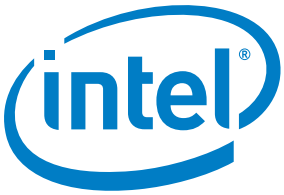

BSP for Microsoft Windows* 7 (WIN*7, WES*7 and POSReady* 7) 32 and 64 bit for Intel® Atom™ Processor E3800 Product Family

Release Notes

May 2015

Intel Confidential

Maintenance Release 3.0
Revision 6.0

Contents

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Revision History

Date	Revision	Description
May 2015	6.0	Updated for Windows 7 Maintenance Release 3
March 2015	5.0	Updated for Windows*7 Maintenance Release 2
September 2014	4.0	Updated for Windows*7 Maintenance Release 1
May 2014	3.0	Added Windows Embedded POSReady 7
March 2014	2.0	Updated USB3 BKM and Know Issues for Gold 2 Release
January 2014	1.0	Updated Release for Windows* 7 Gold 1.0 Release

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1.0 Introduction

1.1 Scope of Document

This document consists Release Notes about Intel developed General Purpose Input/output (GPIO), Inter-Integrated Circuit (I^2C*), Serial Peripheral Interface (SPI), High Speed Universal Asynchronous Receiver/Transmitter (HS-UART), and USB3.0 XHCI driver for Windows* 7 (Win*7), Windows Embedded Standard* 7 (WES7*) and Windows Embedded POSReady* 7. This document also includes information of Window* 7 Inbox drivers that have been validated on Intel® Atom™ E3800 processor.

The driver interfaces, limitations, errata, closed issues, and known issues are also included in this document.

This document is intended for Original Equipment Manufacturers (OEMs) and Original Design Manufacturers (ODMs) that are enabling Win*7 and WES7* drivers with Intel® Atom™ E3800 processor family/Intel® Celeron® Processor N2807/N2930/J1900.

Note: To update the GPIO*, I^2C* and SPI* drivers on structure definition in public driver header file from beta driver to gold driver, recompile your applications with the latest public driver header.

1.2 Systems Requirements

The following Operating Systems are supported:

- Windows* 7 Operating System (32-bit and 64-bit versions)
- Windows Embedded Standard* 7 Operating System (32-bit and 64-bit versions)
- Windows* Embedded POSReady* 7 Operating System (32-bit and 64-bit versions)

Table 1. Terminology

Term	Description
ADMA	Advanced Direct Memory Access
BKM	Best Known Methods
BSOD	Blue Screen of Death (Stop Error)
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
I^2C*	Inter-Integrated Circuit
IOCTLs	Input/Output Controls

Term	Description
HS-UART	High Speed Universal Asynchronous Receiver/Transmitter
LPSS	Low Power Sub-System
ODM	Original Design Manufactures
OEM	Original Equipment Manufactures
MSDN	Microsoft* Developer Network
PIO	Programmed Input/Output
SPI	Serial Peripheral Interface
SUT	System Under Test

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2.0 Release Summary

2.1 Release Details

Driver Version (GPIO, I2C, SPI): 1.1.7.1032

Driver Version (HSUART, SD/eMMC): 1.1.8.1034

Released on May, 2015.

2.2 Release Contents

The contents of this release include:

- Intel® Processor Win*7 IO Drivers 32Bit and 64Bit Driver Installer

  Both "Intel Processor Win*7 IO Drivers 32Bit.msi" and "Intel Processor Win*7 IO Drivers 64Bit.msi" installer will install the following drivers on your system:
  - Intel® Atom™/Celeron®/Pentium® Processor UART Host Controller
  - Intel® Atom™/Celeron®/Pentium® Processor I²C* Controller
  - Intel® Atom™/Celeron®/Pentium® Processor SPI Controller
  - Intel® Atom™/Celeron®/Pentium® Processor GPIO Controller
  - Intel® Atom™/Celeron®/Pentium® Processor Low Power Subsystem Direct Memory Access (DMA) Device
  - Intel® Atom™/Celeron®/Pentium® Processor SD Host Controller
  - Intel® Atom™/Celeron®/Pentium® Processor eMMC* Controller
- Intel® Processor Win*7 IO Drivers – Software Developer Guide
  - Headers Files for GPIO, I²C*, and SPI
  - Software Developers Manual for Win* 7 IO Drivers
- Intel® Processor Win*7 I/O Drivers Release Notes and User's Guide
- Intel® Software License Agreement

2.3 Best Know Configurations

Table 2. Best Known Configurations

Hardware Configuration		
Category	**Description**	**Rev/Type/ Source**
CRB	Bayley Bay Bakersport	FAB 3 REV03 FAB B
SoC	Intel® Atom™ E3800	D0–I : Z8XA
Display	VGA	
Memory	Bayley Bay: 4 GB DDR3 (2x2GB) Bakersport: 2 GB DDR3 (1x2GB with ECC)	
Firmware Configuration		
CRB BIOS	BYTICRB_IA32_R_SPI_0093_39_Sec_Enabled (Stitched with vBIOS v3842)	Intel (CDI#: 558304)
KSC	v03.14	Intel (CDI#: 558304)
Driver/OS Configuration		
Operating System	Windows* 7 SP1 Windows Embedded Standard* 7 SP1 Windows Embedded POSReady 7 SP1	MSDN
Graphics Driver	PC_Version_36_15_0_1097	EMGD
Graphics Driver HotFix	Intel® Embedded Media and Graphics Driver (EMGD) for Bay Trail Embedded SKUs HotFix 36/37.15.0 1127	Intel VIP Kit 107137
GPIO Driver	1.1.7.1032	Intel
I²C* Driver	1.1.7.1032	Intel
SPI Driver	1.1.7.1032	Intel
HS-UART Driver	1.1.7.1032	Intel
SD2 Driver	1.1.8.1034 ***New**	Intel
Chipset INF	10.0.13	Intel
USB 3.0 Driver	3.0.0.34 (32bit and 64bit)	Intel
eMMC* v4.5 Driver	1.1.8.1034 ***New**	Intel
Intel® Sideband Fabric Device (Intel® MBI) Driver Production	1.70.305.16316	Intel VIP Kit 58443
Intel® TXE FEATure FW and tools for Intel® Atom™ Processor E3800 Product Family	1.0.5.1120	Intel VIP Kit 105358

Intel® TXE FEATure FW and tools for Intel® Celeron® Processor N2920 and Intel® Celeron® Processor J1900	1.0.5.1120	Intel VIP Kit 103381

2.4 The Ready Feature

Table 3. The Ready Feature

Area	Feature	Source	Ready*
SIO	General SIO feature	Win*7 Inbox driver	Yes
USB	General USB 2.0 feature	Win*7 Inbox driver	Yes
	General USB 3.0 feature	Intel USB 3.0	Yes
	USB2.0 Boot	Win*7 Inbox driver	Yes
SATA*	General SATA* feature	Win*7 Inbox driver	Yes
PCIe*	General PCIe* feature	Win*7 Inbox driver	Yes
EMGD gfx driver	General graphics feature	Intel	Yes
High Definition Audio	General HD Audio feature	Win*7 Inbox driver	Yes
	HDMI Audio	Integrated in EMGD driver	Yes
Power Management	Power Mgmt S0 and S5	N/A	Yes
	Power Mgmt Sleep S3	Intel	Yes
	Power Mgmt Hibernate S4	Intel	Yes
GPIO Driver*	Direction Setting	Intel	Yes
	Multiplexing Setting		Yes
	Level Value Setting		Yes
	Pin Setting Query		Yes
I^2C* Driver*	Standard Mode (100 Kbps)	Intel	Yes
	Fast Mode (400 Kbps)		Yes
SPI Driver*	SPI Mode 0,1,2,3	Intel	Yes
	Transfer rate from 100Kbps up to 15 Mbps		Yes
HS-UART Driver*	Baud rate support up to 4000000	Intel	Yes
	Data size 5, 6, 7, 8-bit		Yes
	Odd, even, none parity		Yes
	1, 1.5, and 2 stop bits		Yes

Area	Feature	Source	Ready*
	Hardware and No flow control and Software flow control		Yes
DMA Feature* (I^2C*, SPI, HS-UART)	DMA support for I^2C*, SPI and HS-UART	Intel	Yes
SD2 Driver	SD and SDHC cards	Intel	Yes
	Class 2,4,6, and 10		Yes
	1-bit and 4-bit bus mode		Yes
	FAT32, exFAT filesystem		Yes
	ADMA Transfer mode		Yes
	Win*7 OS Boot		Yes
eMMC* Driver	v4.5 Storage		Yes
	Win*7 OS Boot		Yes

NOTES: Refer to the next section for the limitations of the GPIO/I^2C*/SPI/HS-UART/DMA/SD and eMMC* Boot feature

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3.0 Release Notes

3.1 GPIO Driver

GPIO Driver interface is exposed by a series of Input/Output Controls (IOCTLs). A separated "C" header file provides the definition of the IOCTLs and a separated programming guide provides instructions on how to program with the IOCTLs.

Driver Binary Package consists of:

- **iaiogpio.inf**
- **iaiogpio.sys**
- **iaiogpio.cat**

Driver Interface Header consists of: **GPIOPublic.h**

Enabled Features:

- Support GPIO multiplexing setting.
- Support GPIO setting query, query multiplexing information of GPIO pin.
- Support GPIO direction setting, configure selected GPIO pin as input or output pin.
- Support GPIO read pin, read pin's level value when GPIO pin is configured as input pin.
- Support GPIO write pin; configure pin level to high or low when it is configured as output pin.

Limitations:

No Known Limitations

3.2 I²C* Driver

I²C* Driver interface is exposed by a series of IOCTLs. A separated "C" header file provides the definition of the IOCTLs and a separated programming guide provides instructions on how to program with the IOCTLs.

There are total of seven I²C* controllers on the Intel® Atom™ E3800 processor family/Intel® Celeron® Processor N2807/N2930/J1900 which share the same DMA engine. Consequently, the transferring of big data sizes will cause one I²C* controller to occupy the DMA engine for a long duration.

The application can use multiple single transfers or **IOCTL_I2C_EXECUTE_SEQUENCE** interface to transfer big data sizes.

By default, the I²C* driver uses DMA to copy data between peripheral and system memory, but can set the windows* registry to disable the DMA feature and copy data by Programmed Input/Output (PIO) mode. Refer to Best Known Methods (BKM) section to about how set the registry.

Driver Binary Package:

- **iaioi2c.inf**
- **iaioi2c.sys**
- **iaioi2c.cat**

Driver Interface Header: **I2CPublic.h**

Enabled Features:

- Support 7-bit address Mode
- Support Standard Mode (100 Kbps)
- Support Fast Mode (400 Kbps)
- Support polling of I/O data transfer

Limitations:

The maximum single transfer size is limited to 64 Kbytes. Multiple transfers are required for data size of more than 64 KB.

3.3 SPI Driver

The SPI Driver interface is exposed by a series of IOCTLs. A separated "C" header file provides the definition of the IOCTLs and a separated programming guide provides how to program with the IOCTLs.

Driver Binary Package:

- **iaiospi.inf**
- **iaiospi.sys**
- **iaiospi.cat**

Driver Interface Header: **SPIPublic.h**

Enabled Features:

- Support SPI mode 0,1,2,3
- Support transfer rate at the minimum of 100 kbps and at maximum rate 15 Mbps
- Support polling of IO data transfer (Read/Write)
- DMA data transfer

Limitations:

No known limitation

3.4 HS-UART Driver

The HS-UART Driver interface is exposed by standard Windows* Serial Communication interface.

Refer to Serial Communications in Win32 in Microsoft* Developer Network (MSDN) to understand the details:

http://msdn.microsoft.com/en-us/library/ms810467.aspx

The following APIs of serial communication in Win32 are supported in MR1 driver release:

- SetCommMask
- WaitCommEvent
- GetCommMask

Remark: These serial series masks: "`SERIAL_EV_PERR, SERIAL_EV_RX80FULL, SERIAL_EV_EVENT1, SERIAL_EV_EVENT2`" used in above three functions are not supported. Others are supported.

Intel has no plan to support the following APIs of serial communication in Win32:

- **SetupComm**
- **SetCommBreak**
- **ClearCommBreak**
- **EscapeCommFunction** (no support for parameter set to **SETBREAK** and **CLRBREAK**)

Driver Binary Package:

- **iaiouart.inf**
- **iaiouart.sys**
- **iaiouart.cat**

Driver Interface Header:

Refer to MSDN http://msdn.microsoft.com/en-us/library/ms810467.aspx

Enabled Features:

- Support baud rates: 300 – 921600, up to 3686400 by default as specified in the *Bay Trail-I SoC External Design Specification,* Section 27.2.3 Baud Rate Generator. For setting baud rates of 1M, 2M, 3M, and 4M, refer to the BKM section.
- Support data size of 5,6,7, and 8-bit
- Support none, odd and even parity
- Support 1, 1.5, and 2 stop bits
- Support "Hardware" and "No" flow control and software flow control

- Supports Serial Device Control Requests (IOCTLs) defined by Micosoft* for serial controllers in Windows*. See Limitations below for the IOCTLs that will be enabled in Gold release.

Limitations:

- HS-UART driver doesn't support DMA transfer with software flow control. When the application uses the software flow control, the HS-UART will use the PIO mode to copy data between peripheral(s) and system memory.
- Software flow control only supports the maximum baud rate up to 115200. We recommended using hardware flow control for data transfer for high baud rate.
- When 1.5 stop bits are used, the data size can only be supported up to 5 bits.
- IOCTLs are not supported in driver:
  - **IOCTL_SERIAL_XOFF_COUNTER**
  - **IOCTL_SERIAL_LSRMST_INSERT**
  - **IOCTL_SERIAL_SET_BREAK_ON**
  - **IOCTL_SERIAL_SET_BREAK_OFF**

3.5 Low Power Sub-System (LPSS) DMA Driver

The LPSS DMA Driver is not exposed publicly and only the I^2C*, SPI, HS-UART drivers are able to access the DMA driver interface.

3.6 SD2 Storage Driver

The SD2 driver is not exposed publicly and will replace the Windows* Inbox SD2 driver to provide SD2 storage capabilities on this Intel SoC platform.

Apply the following hotfix before driver installation to patch the known data corruption issue:

http://support.microsoft.com/kb/2732471

Driver Binary Package:

- **iaiosd.inf**
- **iaiosd.sys**
- **iaiosd.cat**

Driver Interface Header: None

Enabled Features:

- Support SD and SDHC card specification.
- Support SD card class: 2, 4, 6, 10, and UHS-1.
- Support 1-bit and 4-bit bus mode.
- Support FAT32 and exFAT file system.
- Support Advanced Direct Memory Access (ADMA) transfer mode

Limitation:

SD card read and write performance may be 10- 20% lower in Win*7/WES7* 64 bit due to operating system limitations as the system only sends 64Kb packages.

3.7 eMMC* Storage Driver

The eMMC* storage driver is not exposed publicly and will provide eMMC* storage capabilities on this Intel SoC platform.

Driver Binary Package:

- **iaiosd.inf**
- **iaiosd.sys**
- **iaiosd.cat**

Driver Interface Header: None

Enabled Features:

- Support eMMC* card Specification 4.5
- Support 8-bit SDR & DDR bus mode.
- Support FAT32 and exFAT file system.
- Support ADMA transfer mode

Limitation:

- eMMC* card read and write performance may be 10- 20% lower in Win*7/WES7* 64 bit due to operating system limitations as the system only sends 64 Kb packages.
- Driver don’t support 1-bit and 4-bit bus mode.
- Driver does not support HS200 mode.

3.8 SD and eMMC* Boot Driver

SD and eMMC boot driver is not exposed publicly and it will enable Windows 7 OS to be installed into these storage devices enabled on this Intel SoC platform.

Driver Binary Package:

- **iaiosd.inf**
- **iaiosd.sys**
- **iaiosd.cat**

Driver Interface Header: None

Enabled Features:

Supports Windows* 7, 32 and 64-bit OS installation and boot

Limitation:

- Does not work on Bayley Bay due to platform limitation.

3.9 Errata, Closed Issues, and Known Issues

3.9.1 Errata

Table 4. Errata

Issue #	Description	Impact	Recommendation
4634746	SPI driver failed to read and write on <51 Kbps	Low speed transfer	Use SPI with speed >100 Kbps
4634789	IOTG BIOS does not support USB Legacy boot in xHCI mode.	OS Boot in xHCI mode	Perform OS Boot with USB in EHCI mode.
4634818	System re-enumeration and disconnect on HSIC device due to silicon issue.	File transfer fail on HSCI device when any plug/unplug on USB2.0 bottom port.	Do not plug/unplug on USB2.0 bottom port during file transfer on HSIC device.
4634792	One bit is wrong occasionally in SPI due to Bayley Bay Platform issue	One bit is wrong when perform continuous data transfer in SPI	Use Bakersport Fab A, Fab B, Bayley Bay Fab2 and Bayley bay Fab 3 light green boards.
4634816	System shutdown after BIOS stage when booting up with SD card plug in (Bayley Bay Platform issue)	User failed to boot up the system when connected with the SD card.	Use Bakersport Fab A, Fab B.
4634937	HS-UART COM number increases every time after uninstall/reinstall of UART driver	For those applications using COM ports of HSUART, user need to enable changing input parameter of COM number	Change the HS-UART COM ports in the application whenever the UART driver is reinstalled.
4634826	On top USB2.0 Port (Keyboard or mouse) is unable to wake the system from sleep and hibernate due to the HSIC chipset issue.	User failed to wake the system up by using on top USB2.0 port	Use other USB2.0/USB3.0 port to wake the system from S3 and S4 stage.
4635034	System unable to load into Windows after wake up from hibernate by hitting USBkeyboard and mouse when XHCI mode in BIOS is set to 'Auto' or 'Smart Auto'	User failed to resume the system back from hibernate when XHCI mode is set to "Auto" or smart Auto	Change XHCI mode to "Enable".

3.9.2 Closed Issues

Table 5. Closed Issues

Issue #	Description	Resolution
4634844	High CPU usage when transferring data with high speed through HS-UART	Maintenance Release 1 v1.1.6.1030

4634724	Added UART driver has support for **IOCTL_SERIAL_SET_WAIT_MASK and IOCTL_SERIAL_WAIT_ON_MASK**	Maintenance Release 1 v1.1.6.1030
4634938	HSUART data transfer is incomplete when timeout occurs	Maintenance Release 1 v1.1.6.1030
4635047	I^2C* unable to do read/write after unplugged and plug back to the port when DMA is on.	Maintenance Release 1 v1.1.6.1030
4634842	Intermittent first byte lost when perform I^2C* read on B3-M and B3-D	Maintenance Release 1 v1.1.6.1030

3.9.3 Known Issues

Table 6. Known Issues

Issue #	Description	Impact	Recommendation
4994734	Super Speed USB 3.0 Pendrive Performance Drop in WES* 7	WEC*7 USB3.0 Super Speed thumb drive , for example Lexar* JumpDrive* P10 USB 3.0 Flash Drive 32 GB (up to 265 MB/s read, 245 MB/s write)	Use the standard USB3.0 Pen Drive, for example Corsair Voyager (up to 80 MB/s read, 40 MB/s write).
4994918	[BYT][Win*7][HCK] Several HSUART HCK Device Certification Tests failed [MR1]	HSUART driver will not pass WHCK test and hence no official MSFT certificate granted.	No known functional impact on HSUART. To be fixed in next release.

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