µQseven

User Manual

µQ7-A75-J

Extremely low power/low cost
µQseven® Rel. 2.0 Compliant
Module with NXP
i.MX6 Processor

SECO

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	18th February 2016	First Release	SB

Every effort has been made to ensure the accuracy of this manual. However, SECO S.r.l. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.r.l. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

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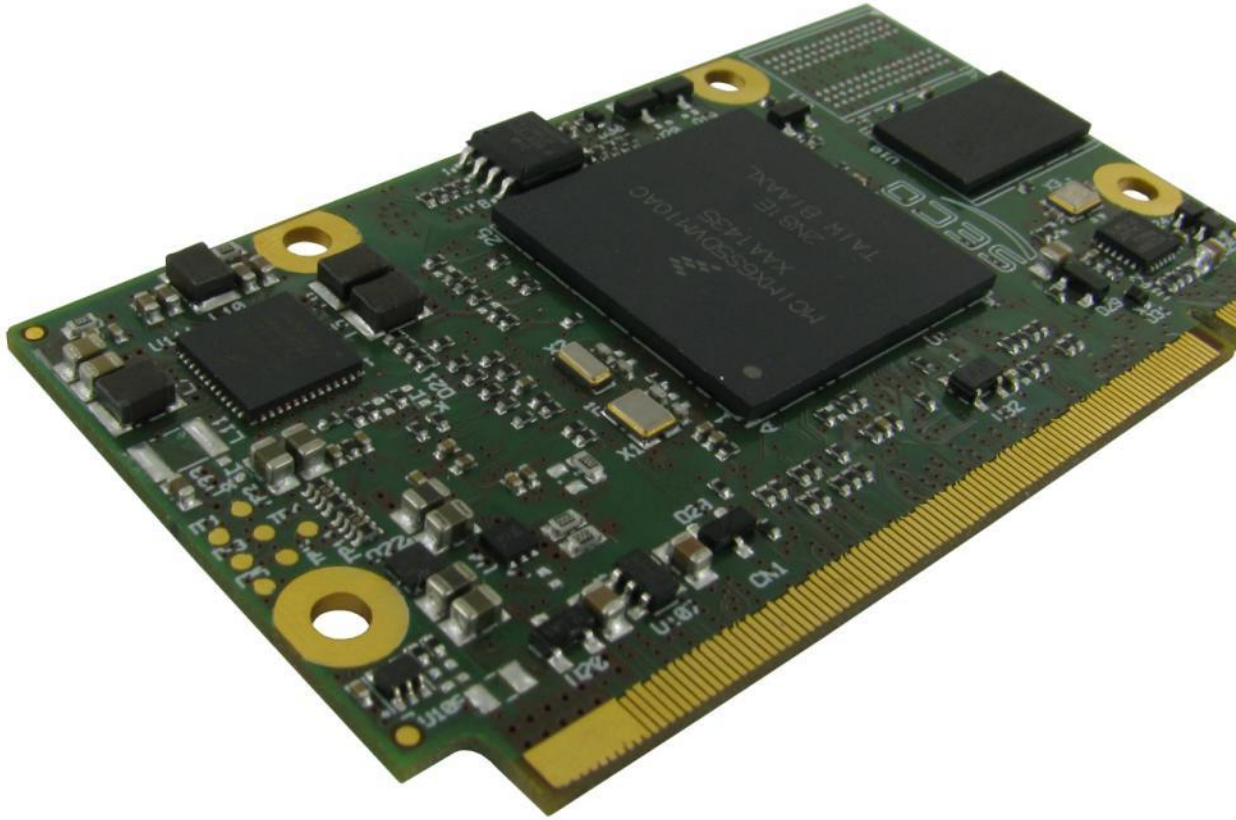
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.r.l. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.r.l. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The µQ7-A75-J module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

1.5 Electrostatic Discharges

The µQ7-A75-J module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling a µQ7-A75-J module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The µQ7-A75-J module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

AC'97	Audio Codec'97, a standard for audio hardware codecs developed by Intel® in 1997
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control.
CSI2	MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host processor
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
DDR3	DDR, 3rd generation
DVI	Digital Visual interface, a type of display video interface
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics

OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port.
PCI-e	Peripheral Component Interface Express
PWM	Pulse Width Modulation
PWR	Power
RMII	Reduced Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer (PHY)
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
USB	Universal Serial Bus
uSDHC	Ultra Secure Digital Host Controller
V_REF	Voltage reference Pin

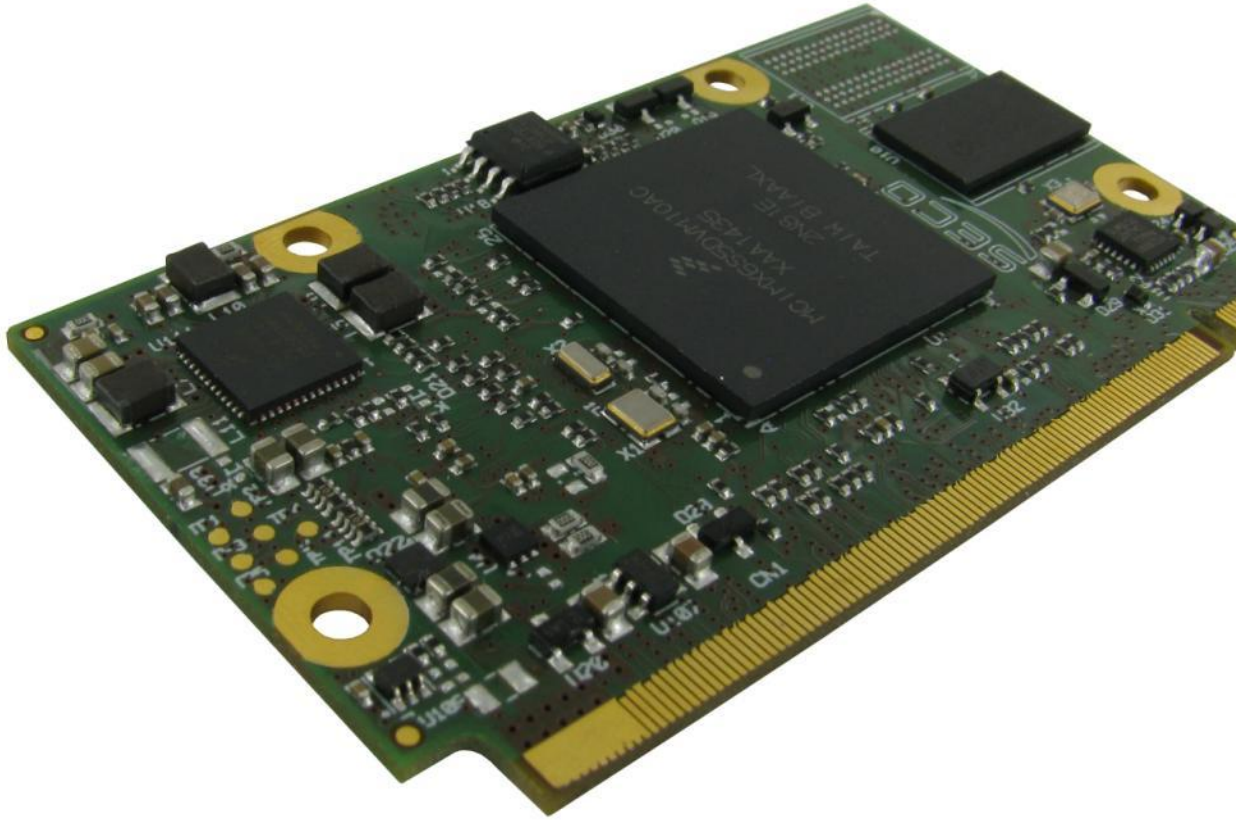
1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
AC'97	http://download.intel.com/support/motherboards/desktop/sb/ac97_r23.pdf
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
CSI	http://www.mipi.org/specifications/camera-interface
DDC	http://www.vesa.org
FasEthernet	http://standards.ieee.org/about/get/802/802.3.html
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
Qseven® Design Guide	http://www.sget.org/uploads/media/Qseven_Design_Guide_2_0.pdf
Qseven® specifications	http://www.sget.org/uploads/media/Qseven-Spec_2.0_SGET.pdf
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
NXP i.MX6 processor	http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors-based-on-arm-cores/i.mx-6-processors:IMX6X_SERIES

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Supported Operating Systems
- Block Diagram



2.1 Introduction

µQ7-A75-J is a CPU module, in µQseven® format, based on embedded NXP i.MX 6Solo and 6Dual Lite, ARM® Cortex®-A9 processors, Single- or Dual-Core, with frequencies up to 1GHz, which are ideal for applications requiring multimedia capabilities.

The board offers a very high level of integration, both for all most common used peripherals in ARM world and for bus interfaces normally used in x86 world, like PCI-Express.

All this comes out in the extremely reduced space offered by µQseven® boards, which offers all functionalities of standard boards in just 40 x 70mm.

This solution allows combining the advantages of a standard, ready-to-use board, like µQseven® boards are, with all advantages offered by ARM application specific processors like NXP i.MX6 processor, in its different versions (Single Core, Dual Core, Quad Core)

Moreover, NXP i.MX6 processors integrate three separated accelerators for Video Processing, Image Processing, 2D and 3D GPUs, giving the processor incredible graphical performances.

The board is completed with up to 1GB DDR3L directly soldered on board (up to 512MB with i.MX 6Solo), and one eMMC Flash Drive, directly accessible like any standard Hard Disk Drive, with up to 8GB of capacity.

The board can support two independent displays using dedicated video interfaces of the module: the first one, is a 24 bit Single/Dual Channel LVDS interface, which can be configured to work as two independent 24 bit Single Channel interfaces. The other display interface is i.MX6's native HDMI interface.

HW video decoding of the most common coding standard (i.e., H.264, MPEG2, MPEG4, DivX, RealVideo and other) is supported. Also MPEG-4, H.263 and H.264 encoding is supported.

Many other features available through the standard Qseven® connector are native for i.MX6 processor: CAN Interface, UART interfaces, 1 x SD/SDIO/MMC interface, PCI-express x1, 2 x PWM Channels, Audio, one USB OTG port, one USB 2.0 host Port.

RMII i.MX6 native interface is internally carried to a Micrel KSZ8091RN Ethernet Transceiver, allowing the implementation of a FastEthernet interface

The µQ7-A75-J module is part of SECO's "Just! Embedded" product line, which are modules totally designed around the features offered by the SOC only, with very few add-ons. This lead to essential, "ready-to-use" and "ready-to-market" products, which allow the reduction of design risks with minimal effort and cost. This allows also to take the most advantage possible from the pin-multiplexing possibilities offered by the i.MX6 processors; indeed, most of the Qseven® standard interfaces, when are not required, can be reprogrammed to offer other functionalities already implemented inside the i.MX6 processor itself.

Optionally, the module can be equipped with a low-power additional RTC, which would replace in working the i.MX6 native RTC (more power consuming).

For external interfacing to standard devices, a carrier board with a 230-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as integration of other peripherals/devices not already included in µQ7-A75-J CPU module.

2.2 Technical Specifications

Processors

NXP i.MX6 Family, based on ARM® CORTEX-A9 processors
- i.MX6S Solo - Single core up to 1GHz
- i.MX6DL Dual Lite - Dual core up to 1GHz per core

Memory

Up to 1GB DDR3L onboard (up to 512MB with i.MX 6Solo)

Graphics

Dedicated 2D Hardware accelerator
Dedicated 3D Hardware accelerator, supports OpenGL® ES2.0 3D
Supports 2 independent displays

Video Interfaces

1 x LVDS Dual Channel or 2 x LVDS Single Channel 18/24 bit interface
HDMI Interface

Video Resolution

LVDS, resolution up to 1920x1200
HDMI, resolution up to 1080p

Mass Storage

Onboard eMMC Drive, up to 8 GB*
SD/MMC/SDIO interface
Internal SPI Flash for booting

PCI Express

1 x PCI-e x1 lane (only PCI-e 1.1 and Gen2 are supported)

** Please consider that for HDD and Flash Disk manufacturers, 1GB = 10^9 Byte. Some OS (like, for example, Windows) intends 1GB = 1024^3 byte, so global capacity shown for Disk Properties will be less than expected. Please also consider that a portion of disk capacity will be used by internal Flash Controller for Disk management, so final capacity will be lower.*

Networking

FastEthernet (10/100 Mbps) interface

USB

1 x USB OTG interface
1 x USB2.0 Host interface

Audio

I2S / AC'97 Audio interface

Other Interfaces

On the card edge connector, many pins can be used as General Purpose I/Os or to implement some (*) of the following extra functionalities:

- Additional SD interface
- Up to 4 UARTs
- CAN interface
- Watchdog(s)
- I2C interfaces
- PWM outputs
- SPI interface
- Additional Audio interface

(*) not all the combinations are allowed simultaneously

Power Management Signals

Power supply voltage: $+5V_{DC}$ ± 5%

Optional Low Power RTC

Operating temperature: 0°C ÷ +60°C **

Dimensions: 40 x70 mm (1.57" x 2.76")

! *** Temperatures indicated are the maximum temperature that the heatspreader / heatsink can reach in any of its parts. This means that it is customer's responsibility to use any passive cooling solution along with an application-dependent cooling system, capable to ensure that the heatspreader / heatsink temperature remains in the range above indicated. Please also check paragraph 4.1*

2.3 Electrical Specifications

According to Qseven® specifications, µQ7-A75-J module needs to be supplied only with an external +5V_{DC} power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from VCC power rail.

2.3.1 Power Consumption

TBM

2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VCC: +5V voltage directly coming from the card edge connector

VCC_5V_SB: +5V stand-by external voltage

VCC_RTC: 3V coin cell voltage coming from the card edge connector for supplying the RTC clock on the i.MX6.

+3P3V_S: +3.3 switched voltage, derived internally.

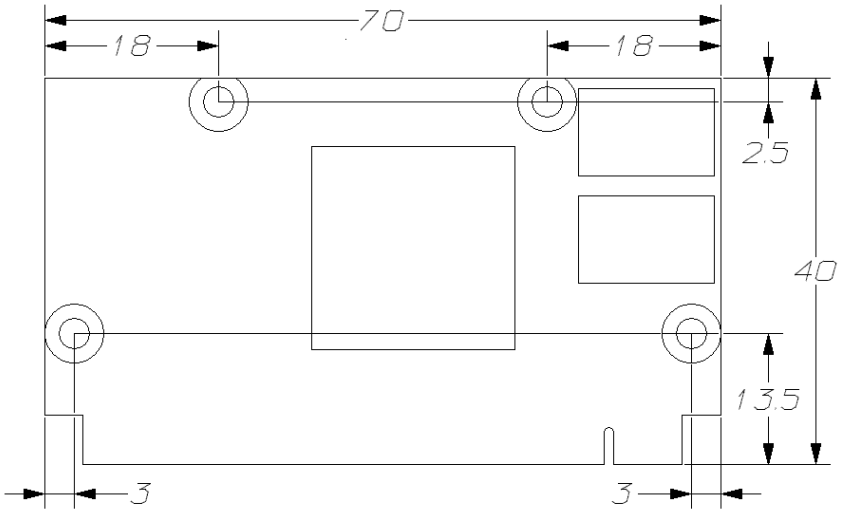
2.4 Mechanical Specifications

According to Qseven® specifications, board dimensions are: 40 x 70 mm (1.57” x 2.76”).

Printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs. Qseven® specification suggests two connector heights, 7.8mm and 7.5mm, but it is also possible to use different connector heights, also remaining compliant to the standard.

When using different connector heights, please consider that, according to Qseven® specifications, components placed on bottom side of µQ7-A75-J will have a maximum height of 2.2mm ± 0.1. Keep this value in mind when choosing the MXM connector’s height, if there is the need to place components on the carrier board in the zone below the Qseven® module.



2.5 Supported Operating Systems

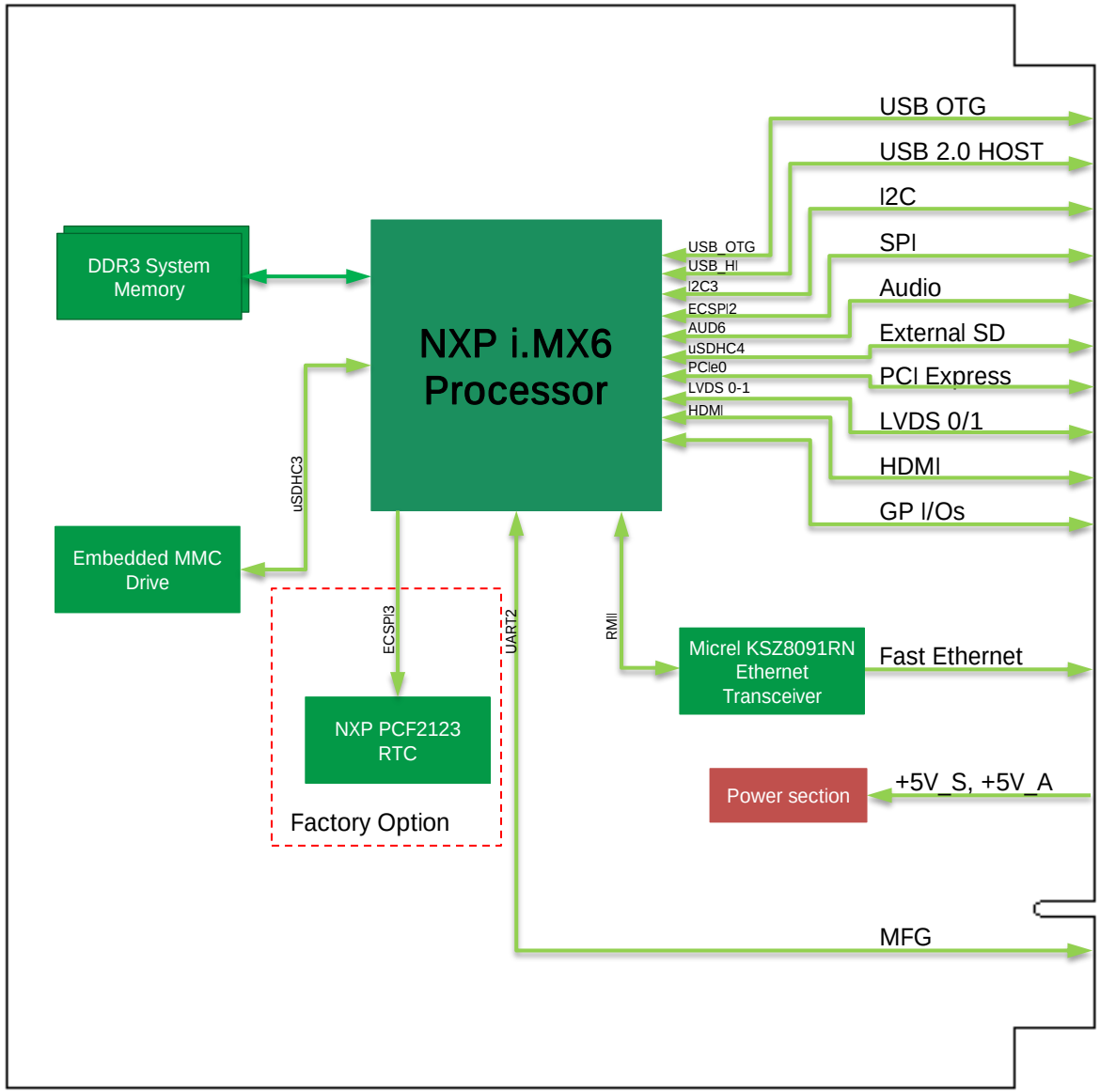
µQ7-A75-J module supports the following operating systems:

- Linux
- Android

SECO will offer the BSP (Board Support Package) for these O.Ss, to reduce at minimum SW development of the board, supplying all the drivers and libraries needed for use both with the Qseven® board and the Carrier Board, assuming that the Carrier Board is designed following SECO Qseven Design Guide, with the same IC’s.

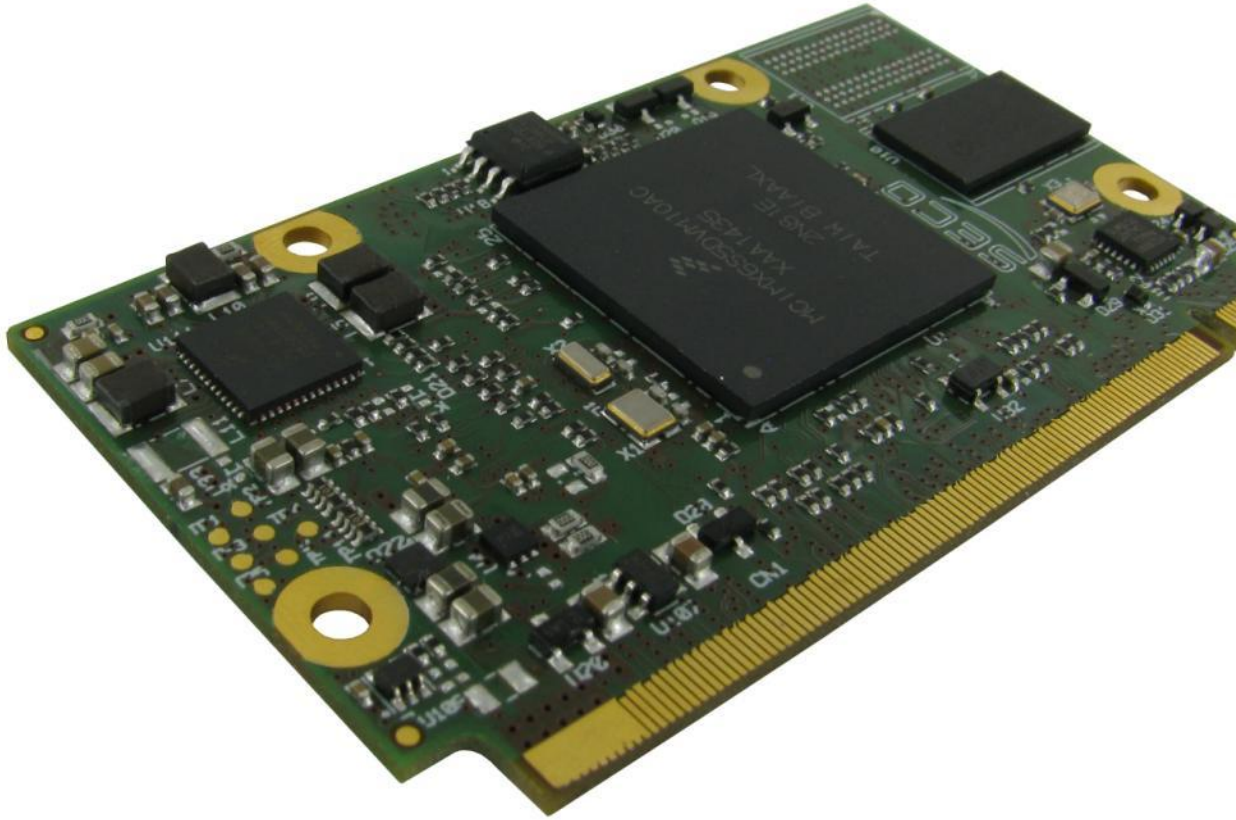
For further details, please visit http://www.seco.com.

2.6 Block Diagram



Chapter 3.
CONNECTORS

- Introduction
- Connectors description



3.1 Introduction

According to Qseven® specifications, all interfaces to the board are available through a single card edge connector.

TOP SIDE

Card edge golden finger, pin 228

Card edge golden finger, pin 2

BOTTOM SIDE

Card edge golden finger, pin 1

Card edge golden finger, pin 229

3.2 Connectors description

3.2.1 Qseven® Connector

According to Qseven® specifications, all interface signals are reported on the card edge connector, which is a 230-pin Card Edge that can be inserted into standard 230 pin MXM connectors, as described in Qseven® specifications.

Not all signals contemplated in Qseven® standard are implemented on MXM connector, due to the functionalities really implemented on µQ7-A75-J module. Therefore, please refer to the following table for a list of effective signals reported on MXM connector.

Furthermore, many signals available on the card edge connector can be used to implement different functionalities, by exploiting the pin-muxing functionalities offered by NXP i.MX6 processors.

For accurate signals description, please consult the following paragraphs. In the first instance, the signals with exclusive functionality will be described thoroughly. After them, it will be given a table with a complete list of all pins with all possible alternative functionalities.

NOTE: Even pins are available on top side of CPU board; odd pins are available on bottom side of CPU board. Please refer to board photos.

Qseven® Golden Finger Connector - CN4

BOTTOM SIDE				TOP SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	1	2	GND	PWR	
	N.A.	N.C.	3	4	N.C.	N.A.	
	N.A.	N.C.	5	6	N.C.	N.A.	
GBE	O	GBE_LINK100#	7	8	GBE_LINK1000#	I/O	Muxed functionalities
GBE	I/O	GBE_MDI1-	9	10	GBE_MDI0-	I/O	GBE
GBE	I/O	GBE_MDI1+	11	12	GBE_MDI0+	I/O	GBE
	N.A.	N.C.	13	14	GBE_ACT#	O	GBE
	REF	GBE_CTREF	15	16	SUS_S5#	O	PWR_MGMT
PWR_MGMT	I	WAKE#	17	18	SUS_S3#	O	PWR_MGMT
Muxed functionalities	O	SUS_STAT#	19	20	PWRBTN#	I	PWR_MGMT
PWR_MGMT	I	SLP_BTN#	21	22	LIDBTN#	I	Muxed functionalities
	PWR	GND	23	24	GND	PWR	
	PWR	GND	25	26	PWGIN	I	PWR_MGMT

Muxed functionalities	I	BATLOW#	27	28	RSTBTN#	I	PWR_MGMT
	N.A.	N.C.	29	30	N.C.	N.A.	
	N.A.	N.C.	31	32	N.C.	N.A.	
Muxed functionalities	O	SATA_ACT#	33	34	GND	PWR	
	N.A.	N.C.	35	36	N.C.	N.A.	
	N.A.	N.C.	37	38	N.C.	N.A.	
	PWR	GND	39	40	GND	PWR	
MISC	I	BOOT_ALT#	41	42	SDIO_CLK	O	SDIO
SDIO	I/O	SDIO_CD#	43	44	GPIO_18	I/O	Muxed functionalities
SDIO	O	SDIO_CMD	45	46	SDIO_WP	I/O	SDIO
SDIO	O	SDIO_PWR#	47	48	SDIO_DAT1	I/O	SDIO
SDIO	I/O	SDIO_DAT0	49	50	SDIO_DAT3	I/O	SDIO
SDIO	I/O	SDIO_DAT2	51	52	SDIO_DAT5	I/O	SDIO
SDIO	I/O	SDIO_DAT4	53	54	SDIO_DAT7	I/O	SDIO
SDIO	I/O	SDIO_DAT6	55	56	USB_DRIVE_VBUS	I	Muxed functionalities
	PWR	GND	57	58	GND	PWR	
AUDIO	O	HDA_SYNC	59	60	SMB_CLK	I/O	MISC
AUDIO	O	HDA_RST#	61	62	SMB_DAT	I/O	MISC
AUDIO	O	HDA_BCLK	63	64	SMB_ALERT#	I/O	Muxed functionalities
AUDIO	I	HDA_SDI	65	66	GP0_I2C_CLK	I/O	MISC
AUDIO	O	HDA_SDO	67	68	GP0_I2C_DAT	I/O	MISC
Muxed functionalities	I	THRM#	69	70	WDTRIG#	I	MISC
Muxed functionalities	O	THRMTRIP#	71	72	WDOUT	O	MISC
	PWR	GND	73	74	GND	PWR	
	N.A.	N.C.	75	76	N.C.	N.A.	
	N.A.	N.C.	77	78	N.C.	N.A.	
Muxed functionalities	O	CSPI1_CLK	79	80	CSPI1_CS0	O	Muxed functionalities
	N.A.	N.C.	81	82	N.C.	N.A.	
	N.A.	N.C.	83	84	N.C.	N.A.	
Muxed functionalities	O	CSPI1_MOSI	85	86	CSPI1_MISO	I	Muxed functionalities

	N.A.	N.C.	87	88	N.C.	N.A.	
	N.A.	N.C.	89	90	N.C.	N.A.	
USB	I	USB_VBUS	91	92	USB_ID	I	USB
USB	I/O	USB_P1-	93	94	USB_P0-	I/O	USB
USB	I/O	USB_P1+	95	96	USB_P0+	I/O	USB
	PWR	GND	97	98	GND	PWR	
LVDS	O	LVDS_A0+	99	100	LVDS_B0+	O	LVDS
LVDS	O	LVDS_A0-	101	102	LVDS_B0-	O	LVDS
LVDS	O	LVDS_A1+	103	104	LVDS_B1+	O	LVDS
LVDS	O	LVDS_A1-	105	106	LVDS_B1-	O	LVDS
LVDS	O	LVDS_A2+	107	108	LVDS_B2+	O	LVDS
LVDS	O	LVDS_A2-	109	110	LVDS_B2-	O	LVDS
LVDS	O	LVDS_PPEN	111	112	LVDS_BLEN	O	LVDS
LVDS	O	LVDS_A3+	113	114	LVDS_B3+	O	LVDS
LVDS	O	LVDS_A3-	115	116	LVDS_B3-	O	LVDS
	PWR	GND	117	118	GND	PWR	
LVDS	O	LVDS_A_CLK+	119	120	LVDS_B_CLK+	O	LVDS
LVDS	O	LVDS_A_CLK-	121	122	LVDS_B_CLK-	O	LVDS
LVDS		LVDS_BLT_CTRL/GP_PWM_OUT0	123	124	HDMI_CEC	I/O	HDMI
Muxed functionalities	I/O	GPIO_6	125	126	GPIO_8	I/O	Muxed functionalities
Muxed functionalities	I/O	GPIO_19	127	128	GPIO_7	I/O	Muxed functionalities
CAN	O	CAN0_TX	129	130	CAN0_RX	I	CAN
HDMI	O	TMDS_CLK+	131	132	CSI_CLK0+	I/O	Muxed functionalities
HDMI	O	TMDS_CLK-	133	134	CSI_CLK0-	I/O	Muxed functionalities
	PWR	GND	135	136	GND	PWR	
HDMI	O	TMDS_TX1+	137	138	CSI_D0+	I/O	Muxed functionalities
HDMI	O	TMDS_TX1-	139	140	CSI_D0-	I/O	Muxed functionalities
	PWR	GND	141	142	GND	PWR	
HDMI	O	TMDS_TX0+	143	144	CSI_D1+	I/O	Muxed functionalities
HDMI	O	TMDS_TX0-	145	146	CSI_D1-	I/O	Muxed functionalities

	PWR	GND	147	148	GND	PWR	
HDMI	O	TMDS_TX2+	149	150	HDMI_CTRL_DAT	I/O	HDMI
HDMI	O	TMDS_TX2-	151	152	HDMI_CTRL_CLK	I/O	HDMI
HDMI	O	HDMI_HPD#	153	154	DP_HPD#	I/O	Muxed functionalities
PCI-E	O	PCIE_CLK_REF+	155	156	PCIE_WAKE#	I/O	Muxed functionalities
PCI-E	O	PCIE_CLK_REF-	157	158	PCIE_RST#	O	PCI-E
	PWR	GND	159	160	GND	PWR	
	N.A.	N.C.	161	162	N.C.	N.A.	
	N.A.	N.C.	163	164	N.C.	N.A.	
	PWR	GND	165	166	GND	PWR	
	N.A.	N.C.	167	168	N.C.	N.A.	
	N.A.	N.C.	169	170	N.C.	N.A.	
UART	O	UART0_TX	171	172	UART0_RTS#	O	UART
	N.A.	N.C.	173	174	N.C.	N.A.	
	N.A.	N.C.	175	176	N.C.	N.A.	
UART	I	UART0_RX	177	178	UART0_CTS#	I	UART
PCI-E	O	PCIE0_TX+	179	180	PCIE0_RX+	I	PCI-E
PCI-E	O	PCIE0_TX-	181	182	PCIE0_RX-	I	PCI-E
	PWR	GND	183	184	GND	PWR	
GPIO	I/O	GPIO0	185	186	GPIO1	I/O	GPIO
GPIO	I/O	GPIO2	187	188	GPIO3	I/O	GPIO
GPIO	I/O	GPIO4	189	190	GPIO5	I/O	GPIO
GPIO	I/O	GPIO6	191	192	GPIO7	I/O	GPIO
	PWR	VCC_RTC	193	194	GP_PWM_OUT2	O	MISC
Muxed functionalities	I	GP_TIMER_IN	195	196	N.C.	N.A.	
	PWR	GND	197	198	GND	PWR	
SPI	O	SPI_MOSI	199	200	SPI_CS0#	O	SPI
SPI	I	SPI_MISO	201	202	SPI_CS1#	O	SPI
SPI	O	SPI_CLK	203	204	N.C.	N.A.	
	PWR	VCC_5V_SB	205	206	VCC_5V_SB	PWR	

	N.A.	N.C.	207	208	MFG_NC2	N.A.	MFG
MFG	N.A.	MFG_NC1	209	210	N.C	N.A.	
	PWR	VCC	211	212	VCC	PWR	
	PWR	VCC	213	214	VCC	PWR	
	PWR	VCC	215	216	VCC	PWR	
	PWR	VCC	217	218	VCC	PWR	
	PWR	VCC	219	220	VCC	PWR	
	PWR	VCC	221	222	VCC	PWR	
	PWR	VCC	223	224	VCC	PWR	
	PWR	VCC	225	226	VCC	PWR	
	PWR	VCC	227	228	VCC	PWR	
	PWR	VCC	229	230	VCC	PWR	

3.2.1.1 PCI Express interface signals

The µQ7-A75-J module can offer one PCI Express lane, which is directly managed by i.MX6 processor (all versions).

PCI express Gen 2.0 (5Gbps) is supported. Of the previous generation, only PCI express 1.1 is supported.

Here following the signals involved in PCI express management

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE_CLK_REF+/ PCIE_CLK_REF-: PCI Express Reference Clock for lane #0, Differential Pair

PCIE_RST#: Reset Signal that is sent from Qseven® Module to any PCI-e device available on the carrier board. It is a 3.3V active-low signal with a 10kΩ pull-up resistor; it can be used directly to drive externally a single RESET Signal. In case there is the need to supply Reset signal to multiple devices, it is recommended to provide for a buffer on the carrier board.

3.2.1.2 UART interface signals

According to the Qseven® Rel. 2.0 specifications, µQ7-A75-J module offers one UART interface, directly managed by i.MX6 processor (all versions), more exactly by UART port #3.

Here following the signals related to UART interface:

UART0_TX: UART Interface, Serial data Transmit (output) line, +3P3V_S electrical level

UART0_RX: UART Interface, Serial data Receive (input) line, +3P3V_S electrical level with 10kΩ pull-up

UART0_RTS#: UART Interface, Handshake signal, Request to Send (output) line, +3P3V_S electrical level

UART0_CTS#: UART Interface, Handshake signal, Clear to Send (Input) line, +3P3V_S electrical level with 10kΩ pull-up.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If there isn't any explicit need of interfacing directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

All of the above mentioned signals can also be used for different functionalities; please refer to the pin muxing table for more details.

3.2.1.3 FastEthernet signals

FastEthernet interface is realized, on µQ7-A75-J module, using a Micrel® KSZ8091 Gigabit Ethernet transceiver, which is interfaced to NXP i.MX6 processor through RMII interface.

Here following the signals involved in Fast Ethernet management

GBE_MDI0+/GBE_MDI0-: Media Dependent Interface (MDI) Transmit differential pair

GBE_MDI1+/GBE_MDI1-: Media Dependent Interface (MDI) Receive differential pair

GBE_ACT#: Ethernet controller activity indicator. Active Low Output signal, electrical level +3P3V_S with a 4k7Ω pull-up resistor

GBE_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, electrical level +3P3V_S with a 10kΩ pull-up resistor.

3.2.1.4 USB interface signals

NXP i.MX6 processor offers four different USB 2.0 controllers.

USB 2.0 controller Core #0 is capable of OTG (On-The-Go) capabilities, capable to work in High Speed (HS), Full Speed (FS) and Low Speed (LS) in Host mode, and HS/FS in peripheral mode. It is carried out directly to the golden finger connector

USB 2.0 controller Core #1 can work only in Host mode, and can work in HS, FS and LS.

i.MX6 processor's USB controller cores #2 and #3 are not used by the module.

Here following the signals related to USB interfaces.

USB_P0+/USB_P0-: Universal Serial Bus Port #0 differential pair (directly managed by i.MX6 USB Host Controller core #1).

USB_P1+/USB_P1-: Universal Serial Bus Port #1 differential pair (directly managed by i.MX6 USB OTG port).

USB_ID: USB ID Input, electrical level +3P3V_S, 10kΩ pull-up. This signal must be driven as an open collector signal by external circuitry placed on the carrier board. It must be tied to GND when USB Port #1 has to be set to work in Host mode. When not driven, USB Port#1 will work in Client mode.

USB_VBUS: USB Client Connect Pin, electrical level +3P3V_S, 10kΩ pull-up. When USB Port #1 is set to work in Client mode, then this signal shall be used to inform the USB controller when an external USB Host is connected (signal High) or disconnected (Signal Low).

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

3.2.1.5 SDI/O interface signals

The NXP i.MX6 processors offer many different SDIO interfaces, that can be used independently one from the other to implement different mass storages (internal eMMC, internal SD Card, external SDI/O interface).

Each of the uSDHC controllers complies with:

- SD Host Controller Standard Specification version 3.0
- MMC System Specification version 4.2/4.3/4.4/4.41
- SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- SDIO Card Specification version 3.0

SDI/O port #4 is externally accessible through golden edge finger connector, and can work in 1-bit, 4-bit and 8-bit modes (8-bit mode for MMC support).

Signals involved with SDI/O interface are the following:

SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +3P3V_S with 10kΩ pull-up resistor. This signal must be externally pulled low to signal that a SDIO/MMC Card is present.

SDIO_CLK: Clock Line (output), 52MHz maximum frequency for MMC High Speed Mode, 50 MHz maximum frequency for SD/SDIO High Speed Mode

SDIO_CMD: Command/Response line. Bidirectional signal, electrical level +3P3V_S, used to send command from Host (i.MX6 processor) to the connected card, and to send the response from the card to the Host.

SDIO_PWR#: SDIO Power Enable output, active low signal, electrical level +3P3V_S. It is used to enable the power line supplying SD/SDIO/MMC devices.

SDIO_WP: Write Protect bidirectional signal, electrical level +3P3V_S. It is used to communicate the status of Write Protect switch on external SD/MMC card.

SDIO_DAT[0÷7]: SDIO data bus. SDIO_DAT0 signal is used for all communication modes. SDIO_DAT[1÷3] signals are required for 4-bit SD/SDIO/MMC communication modes. SDIO_DAT[4÷7] are used only for 8-bit MMC communication mode.

All of the above mentioned signals can also be used for different functionalities; please refer to the pin muxing table for more details.

3.2.1.6 Audio interface signals

µQ7-A75-J module supports AC'97 or I2S audio format, thanks to native support offered by the processor to this audio codec standard.

Here following the signals related to AC'97/I2S Audio interface:

HDA_SYNC: AC'97 Serial Bus Synchronization or I2S Word Select Signal. Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_RST#: AC'97/I2S Codec Reset. Active Low signal Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_BCLK: AC'97 24MHz Serial Bit Clock or I2S Serial Data Clock signal. Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_SDO: AC'97/I2S Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_SDI: AC'97/I2S Serial Data In signal. Input to the module from the Carrier board, electrical level +3.3V_S.

All these signals have to be connected, on the Carrier Board, to an AC'97 or I2S Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.1.7 LVDS Flat Panel signals

Embedded into NXP i.MX6 processor there is an LVDS Display Bridge, connected to the Image Processing Unit (IPU), that makes externally available two LVDS channels, each one consisting of 1 clock pair and four data pairs.

It is possible to configure LVDS output so that it can be used as:

- One single channel (18 or 24 bit) output, max resolution supported 1366 x 768 @ 60fps
- One dual channel (18 or 24 bit) output, max resolution supported 1600 x 1200 @ 60fps
- Two identical single channel outputs, max resolution supported 1366 x 768 @ 60fps
- Two independent single channel outputs, max resolution supported 1366 x 768 @ 60fps on each channel

All of these possibilities come by opportunely configuring the O.S. installed on the module.

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Channel #0 differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Channel #0 differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Channel #0 differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Channel #0 differential data pair #3.

LVDS_A_CLK+/LVDS_A_CLK-: LVDS Channel #0 differential Clock.

LVDS_B0+/LVDS_B0-: LVDS Channel #1 differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Channel #1 differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Channel #1 differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Channel #1 differential data pair #3.

LVDS_B_CLK+/LVDS_B_CLK-: LVDS Channel #1 differential Clock

LVDS_PPEN: +3.3V_S electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display. This pin can also be used as a Generic I/O pin, please check pin muxing table.

LVDS_BLEN: +3.3V_S electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display. This pin can also be used as a Generic I/O pin, please check pin muxing table.

LVDS_BLT_CTRL/GP_PWM_OUT0: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. This pin can also be used differently, please check the pin-muxing table.

3.2.1.8 HDMI interface signals

Besides LVDS interface, NXP i.MX6 processor also has an embedded HDMI Tx module, which provides a HDMI standard interface for HDMI1.4a compliant displays.

Signals involved in HDMI management are the following:

TMDS_CLK+/TMDS_CLK-: TMDS differential Clock.

TMDS_TX0+/TMDS_TX0-: TMDS differential pair #0

TMDS_TX1+/TMDS_TX1-: TMDS differential pair #1

TMDS_TX2+/TMDS_TX2-: TMDS differential pair #2

HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, electrical level +3P3V_S with a 4k7Ω pull-up resistor.

HDMI_CTRL_CLK: DDC Clock line for HDMI panel. Bidirectional signal, electrical level +3P3V_S with a 4k7Ω pull-up resistor. Please be aware that this signal can also be used differently, please check the pin-muxing table.

HDMI_CEC: HDMI Consumer Electronics Control (CEC) Line. Bidirectional signal, electrical level +3.3V_S. Please be aware that this signal can also be used differently, please check the pin-muxing table.

HDMI_HPD#: Hot Plug Detect Input signal. +3.3V_S electrical level signal with 100kΩ pull-down resistor

Since HDMI Tx module is embedded in the i.MX6 processors it is not necessary to implement voltage level shifter for TMDS differential pairs on the Carrier board. It is still necessary, however, to implement voltage level shifters on Control data/Clock signals, as well as for Hot Plug Detect signal.

3.2.1.9 SPI interface signals

i.MX6 processors offer up to four Enhanced Configurable Serial Peripheral Interfaces (eCSPIS), which can be used for connection of EEPROMs and Serial Flash devices, which can also be used for serial boot.

SPI interface can support speed up to 20MHz.

Signals involved with SPI management are the following (they are supported by i.MX6 processor's ECSPI2 controller):

SPI_MOSI: SPI Master Out Slave In, Output from Qseven® module to SPI devices embedded on the Carrier Board.

SPI_MISO: SPI Master In Slave Out, Input to Qseven® module from SPI devices embedded on the Carrier Board.

SPI_CLK: SPI Clock Output to carrier board's SPI embedded devices.

SPI_CS0#: SPI primary Chip select, active low output signal.

SPI_CS1#: SPI secondary Chip select, active low output signal. This signal must be used only in case there are two SPI devices on the carrier board, and the first chip select signal (SPI_CS0#) has already been used. It must not be used in case there is only one SPI device.

All of the above mentioned signals can also be used for different functionalities, please refer to the pin muxing table for more details.

3.2.1.10 CAN interface signals

Since i.MX6 processor includes a Flexible Controller Area Network (FlexCAN), the µQ7-A75-J module can also offer a CAN interface.

This interface is compliant to CAN specifications rel. 2.0 part B.

CAN0_TX: CAN Transmit Output for CAN Bus Channel 0. +3P3V_S electrical voltage level signal.

CAN0_RX: CAN Receive Input for CAN Bus Channel 0. +3P3V_S electrical voltage level signal.

Please consider that it is not possible to connect Qseven® CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

All of the above mentioned signals can also be used for different functionalities; please refer to the pin muxing table for more details.

3.2.1.11 Power Management signals

According to Qseven® specifications, on the golden edge finger connector there is a set of signals that are used to manage the power rails and power states. The signals involved are:

PWGIN: Power Good Input, +5V_S tolerant active high signal. It must be driven on the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

PWRBTN#: Power Button Input, active low +3.3VSB electrical voltage signal, with 10kΩ pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

RSTBTN#: Reset Button Input, active low +3P3V_S electrical voltage signal. This signal can be connected to a momentary push-button: a pulse to GND of this signal will reset the Qseven® module.

SUS_S3#: S3 status output, active low +3.3VSB electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S4#: S4 status output, active low +3.3VSB electrical voltage signal. This signal is used, on the carrier board, to shut off the power supply to all the devices that must become inactive only during S4 (Suspend to Disk) power state.

WAKE#: Wake Input, active low +3.3VSB electrical voltage signal with 10kΩ pull-up resistor and series Schottky diode. This signal can be driven low, on the carrier board, to report that a Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used. Please be aware that this signal can also be used differently, please check the pin-muxing table.

SLP_BTN#: Sleep button Input, active low +3.3VSB electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board. Please be aware that this signal can also be used differently, please check the pin-muxing table.

3.2.1.12 Miscellaneous signals

Here following, a list of signals that complete the standard features of µQ7-A75-J module.

SMB_CLK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3P3V_S with a 4k7Ω pull-up resistor. It is managed by i.MX6 processor's I2C1 controller.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3P3V_S with a 4k7Ω pull-up resistor. It is managed by i.MX6 processor's I2C1 controller.

GP0_I2C_CLK: general purpose I2C Bus clock line. Bidirectional signal, electrical level +3P3V_S with a 4k7Ω pull-up resistor. It is managed by i.MX6 processor's I2C3 controller.

GP0_I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3P3V_S with a 4k7Ω pull-up resistor. It is managed by i.MX6 processor's I2C3 controller.

WDTRIG#: Watchdog Trigger Input. It is an active low signal, +3P3V_S voltage, with 10kΩ pull-up resistor. This signal can be used to reset and restart, via Hardware, the internal Watchdog Timer (which is usually managed via Software using µQ7-A75-J dedicated API - Application Program Interface - libraries).

WDOUT: Watchdog event indicator Output. It is an active high signal, +3.3V_S voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW.

BOOT_ALT#: Boot Alternate Input, active low +3P3V_S voltage signal with 10kΩ pull-up resistor. When this signal is driven low, then i.MX6 processors starts to work in peripheral mode, i.e. it begins to wait for inputs from an external Host connected to the system. This is used usually when it is necessary to program the module.

All of the above mentioned signals (except for BOOT_ALT#) can also be used for different functionalities; please refer to the pin muxing table for more details.

3.2.1.13 Manufacturing signals

According to Qseven® Standard specifications, rel. 2.0, on pins designed as MFG_NC1 and MFG_NC2 are carried the NXP i.MX6 Internal UART #2 signals TX and RX, which can be used for debug purposes

3.2.2 Multiplexed signals

As stated more times in the previous paragraphs, most of the signals available on the Qseven® Card Edge Connector can be reprogrammed to implement different functionalities, according to the i.MX6 pin-multiplexing possibilities.

For this reason, in the following table is shown a complete list of all the multiplexing possibilities offered by this module.

The signals are grouped in logical ports, where each logical port represents one of the standard functionalities (if applicable) of the Qseven modules. Please be aware that sometimes the multiplexing can lead to conflicts (i.e., the same functionality is available on 2 or more logical ports). This situation is evidenced in the last column of the following table.

When the i.MX6 Signal is marked in bold italic (like ***WAKE#***), it means that the standard function is managed through SECO BSP, it is not native of the i.MX6 processor.

Port #	MXM Pin	MXM Pin Name	Qseven® function group	i.MX6 Pad name	i.MX6 Signal for standard function	i.MX6 Alternative Signal					Also used in Port #
1	191	SERIRQ/GPIO6	GPIO	NANDF_CS1	GPIO6_IO14						
	192	LPC_LDRQ#/GPIO7		NANDF_CS2	GPIO6_IO15						
2	17	WAKE#	Power Management	CSI0_DAT13	***WAKE#***	UART4_RX_DATA				GPIO5_IO31	
	22	LID_BTN#		CSI0_DAT17	---	UART4_CTS_B				GPIO6_IO03	
	27	BATLOW#		CSI0_DAT16	---	UART4_RTS_B				GPIO6_IO02	
	64	SMB_ALERT#		CSI0_DAT12	---	UART4_TX_DATA				GPIO5_IO30	
3	19	SUS_STAT#	Power Management	CSI0_DAT14	---	UART5_TX_DATA				GPIO6_IO00	
	21	SLP_BTN#		CSI0_DAT15	***SLP_BTN#***	UART5_RX_DATA				GPIO6_IO01	
	44	SDIO_LED		CSI0_DAT18	---	UART5_RTS_B				GPIO6_IO04	
	56	USB_DRIVE_VBUS		CSI0_DAT19	---	UART5_CTS_B				GPIO6_IO05	
4	8	GBE_LINK1000#	Various	SD2_CLK	---	SD2_CLK				GPIO1_IO10	
	33	SATA_ACT#		SD2_DAT1	---	SD2_DATA1	AUD4_TXFS			GPIO1_IO14	25
	61	HDA_RST#/AC97_RST#/I2S_RST#		SD2_CMD	***AUD_RST#***	SD2_CMD				GPIO1_IO11	7
	70	WDTRIG#		SD2_DAT2	***WDT_TRIG_OUT***	SD2_DATA2	AUD4_TXD			GPIO1_IO13	26
	125	GP2_I2C_DAT/LVDS_DID_DAT		SD2_DAT3	---	SD2_DATA3	AUD4_TXC			GPIO1_IO12	
	195	FAN_TACHOIN/GP_TIMER_IN		SD2_DAT0	---	SD2_DATA0	AUD4_RXD			GPIO1_IO15	

Port #	MXM Pin	MXM Pin Name	Qseven® function group	i.MX6 Pad name	i.MX6 Signal for standard function	i.MX6 Alternative Signal					Also used in Port #
5	42	SDIO_CLK#	4-bit SDIO	SD4_CLK	SD4_CLK					GPIO7_IO10	
	43	SDIO_CD#		NANDF_D6	***SDIO_CD#***					GPIO2_IO06	
	45	SDIO_CMD		SD4_CMD	SD4_CMD					GPIO7_IO09	
	46	SDIO_WP		CSI0_DATA_EN	SDIO_WP					GPIO5_IO20	
	47	SDIO_PWR#		NANDF_D5	***SDIO_PWR#***					GPIO2_IO05	
	48	SDIO_DAT1		SD4_DAT1	SD4_DATA1	PWM3_OUT				GPIO2_IO09	
	49	SDIO_DAT0		SD4_DAT0	SD4_DATA0					GPIO2_IO08	
	50	SDIO_DAT3		SD4_DAT3	SD4_DATA3					GPIO2_IO11	
	51	SDIO_DAT2		SD1_DAT2	SD4_DATA2					GPIO2_IO10	
6	52	SDIO_DAT5	8-bit SDIO	SD4_DAT5	SD4_DATA5		UART2_RTS_B			GPIO2_IO13	
	53	SDIO_DAT4		SD4_DAT4	SD4_DATA4		UART2_RX_DATA			GPIO2_IO12	
	54	SDIO_DAT7		SD4_DAT7	SD4_DATA7		UART2_TX_DATA			GPIO2_IO15	
	55	SDIO_DAT6		SD4_DAT6	SD4_DATA6		UART2_CTS_B			GPIO2_IO14	
7	59	HDA_SYNC/AC97_SYNC/I2S_WS	AC'97 / I2S Audio	DI0_PIN3	AUD6_TXFS					GPIO4_IO19	
	61	HDA_RST#/AC97_RST#/I2S_RST#		SD2_CMD	***AUD_RST#***	SD2_CMD				GPIO1_IO11	4
	63	HDA_BCLK/AC97_BCLK/I2S_CLK		DI0_PIN15	AUD6_TXC					GPIO4_IO17	
	65	HDA_SDI/AC97_SDI/I2S_SDI		DI0_PIN4	AUD6_RXD					GPIO4_IO20	
	67	HDA_SDO/AC97_SDO/I2S_SDO		DI0_PIN2	AUD6_TXD					GPIO4_IO18	
8	60	SMB_CLK/GP1_I2C_CLK	SM Bus	CSI0_DAT9	I2C1_SCL					GPIO5_IO27	
	62	SMB_DAT/GP1_I2C_DAT		CSI0_DAT8	I2C1_SDA					GPIO5_IO26	
9	66	GP0_I2C_CLK	I2C	GPIO_5	I2C3_SCL					GPIO1_IO05	
	68	GP0_I2C_DAT		GPIO_6	I2C3_SDA					GPIO1_IO06	
10	69	THRM#	Thermal	KEY_ROW4	---	FLEXCAN2_RX	UART5_CTS_B			GPIO4_IO15	
	71	THRMTRIP#		KEY_COL4	---	FLEXCAN2_TX	UART5_RTS_B			GPIO4_IO14	
11	79	USB_6_7_OC#	USB Over Current	KEY_COL0	---	AUD5_TXC		UART4_TX_DATA	ECSPI1_SCLK	GPIO4_IO06	
	80	USB_4_5_OC#		KEY_ROW1	---	AUD5_RXD	UART5_RX_DATA		ECSPI1_SS0	GPIO4_IO09	
	85	USB_2_3_OC#		KEY_ROW0	---	AUD5_TXD		UART4_RX_DATA	ECSPI1_MOSI	GPIO4_IO07	
	86	USB_0_1_OC#		KEY_COL1	---	AUD5_TXFS	UART5_TX_DATA		ECSPI1_MISO	GPIO4_IO08	22

Port #	MXM Pin	MXM Pin Name	Qseven® function group	i.MX6 Pad name	i.MX6 Signal for standard function	i.MX6 Alternative Signal					Also used in Port #
12	129	CAN0_TX	CAN Bus	CSI0_DAT10		UART1_TX_DATA				GPIO5_IO28	
				KEY_COL2	FLEXCAN1_TX					GPIO4_IO10	
	130	CAN0_RX		CSI0_DAT11		UART1_RX_DATA				GPIO5_IO29	
				KEY_ROW2	FLEXCAN1_RX					GPIO4_IO11	
13	152	HDMI_CTRL_CLK	Hot Plug	KEY_COL3	HDMI_TX_DDC_SCL	SPDIF_IN				GPIO4_IO12	20
	154	DP_HPD#		GPIO_17	---	SPDIF_OUT				GPIO7_IO12	
14	171	UART0_TX	UART	EIM_D24	UART3_TX_DATA					GPIO3_IO24	
	172	UART0_RTS#		EIM_D31	UART3_RTS_B					GPIO3_IO31	
	177	UART0_RX		EIM_D25	UART3_RX_DATA					GPIO3_IO25	
	178	UART0_CTS#		EIM_D30	UART3_CTS_B					GPIO3_IO30	
15	185	LPC_AD0/GPIO0	GPIO	SD1_DAT0	GPIO1_IO16	SD1_DATA0					
	186	LPC_AD1/GPIO1		SD1_DAT1	GPIO1_IO17	SD1_DATA1	PWM3_OUT				
	187	LPC_AD2/GPIO2		SD1_DAT2	GPIO1_IO19	SD1_DATA2					
	188	LPC_AD3/GPIO3		SD1_DAT3	GPIO1_IO21	SD1_DATA3					
	189	LPC_CLK/GPIO4		SD1_CLK	GPIO1_IO20	SD1_CLK					
	190	LPC_FRAME#/GPIO5		SD1_CMD	GPIO1_IO18	SD1_CMD	PWM4_OUT				
16	194	SPKR/GP_PWM_OUT2	SPKR	DISP0_DAT9	PWM2_OUT		WDOG2_B			GPIO4_IO30	
17	199	SPI_MOSI	SPI	DISP0_DAT16	ECSPI2_MOSI					GPIO5_IO10	
	200	SPI_CS0#		DISP0_DAT18	ECSPI2_SS0					GPIO5_IO12	
	201	SPI_MISO		DISP0_DAT17	ECSPI2_MISO					GPIO5_IO11	
	202	SPI_CS1#		DISP0_DAT15	ECSPI2_SS1					GPIO5_IO09	
	203	SPI_SCK		DISP0_DAT19	ECSPI2_SCLK					GPIO5_IO13	
18	127	GP2_I2C_CLK/LVDS_DID_CLK	---	GPIO_19	---	CCM_CLKO1				GPIO4_IO05	
	132	RSVD (Differential Pair)		CSI_CLK0_DP	---	CSI_CLK0_P					
	134	RSVD (Differential Pair)		CSI_CLK0_DN	---	CSI_CLK0_N					
	138	DP_AUX+		CSI_D0_DP	---	CSI_DATA0_P					
	140	DP_AUX-		CSI_D0_DN	---	CSI_DATA0_N					
	144	RSVD (Differential Pair)		CSI_D1_DP	---	CSI_DATA1_P					
	146	RSVD (Differential Pair)		CSI_D1_DN	---	CSI_DATA1_N					

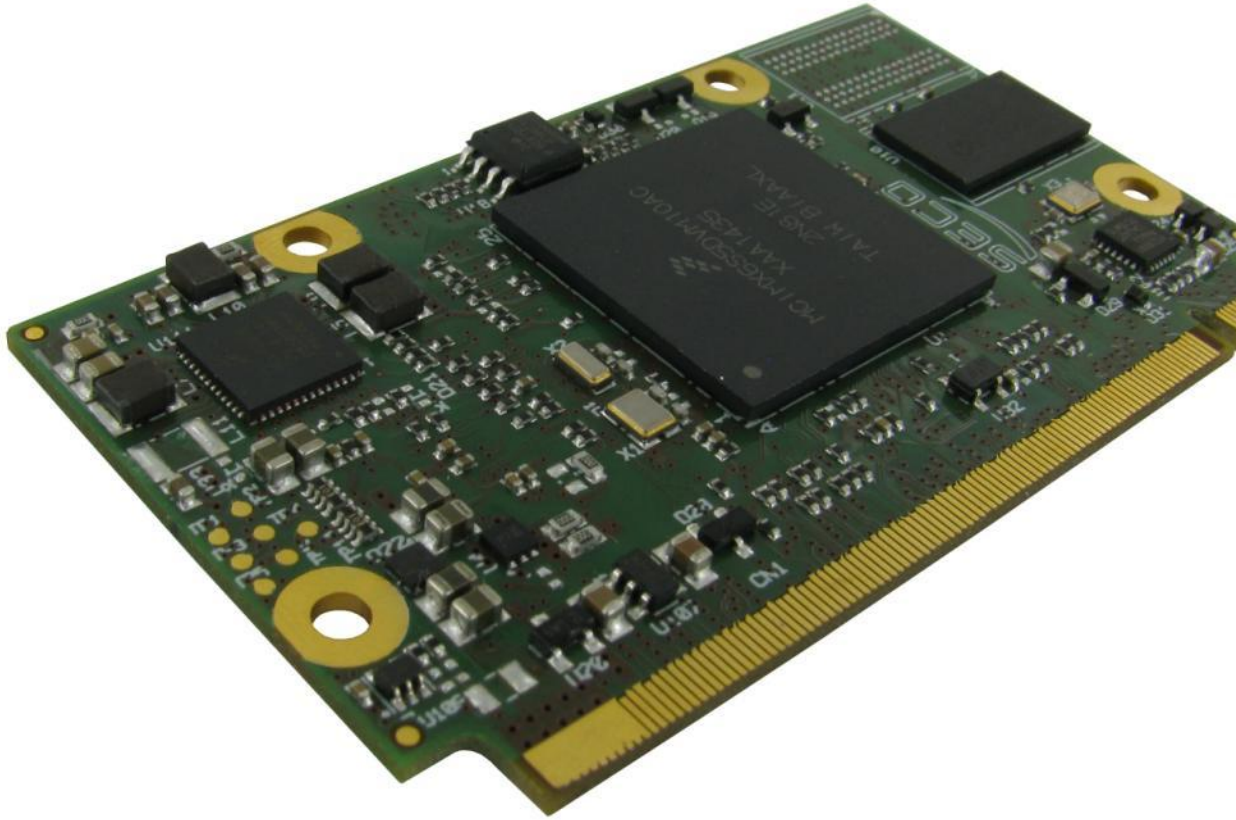
Port #	MXM Pin	MXM Pin Name	Qseven® function group	i.MX6 Pad name	i.MX6 Signal for standard function	i.MX6 Alternative Signal					Also used in Port #
19	155	PCIE_CLK_REF+	PCIe	CLK1_P	PCIE_CLK_REF+						
	156	PCIE_WAKE#		CSI0_DAT13	---					GPIO5_IO31	
	157	PCIE_CLK_REF-		CLK1_N	PCIE_CLK_REF-						
	179	PCIE0_TX+		PCIE_TXP	PCIE_TX_P						
	180	PCIE0_RX+		PCIE_RXP	PCIE_RX_P						
	181	PCIE0_TX-		PCIE_TXM	PCIE_TX_N						
	182	PCIE0_RX-		PCIE_RXM	PCIE_RX_N						
20	124	GP_1-Wire_Bus	HDMI	EIM_A25	HDMI_TX_CEC_LINE					GPIO5_IO02	
	131	DP_LANE3+/TMDS_CLK+		HDMI_CLKP	HDMI_TX_CLK_P						
	133	DP_LANE3-/TMDS_CLK-		HDMI_CLKM	HDMI_TX_CLK_N						
	137	DP_LANE1+/TMDS_LANE1+		HDMI_D1P	HDMI_TX_DATA1_P						
	139	DP_LANE1-/TMDS_LANE1-		HDMI_D1M	HDMI_TX_DATA1_N						
	143	DP_LANE2+/TMDS_LANE0+		HDMI_D0P	HDMI_TX_DATA0_P						
	145	DP_LANE2-/TMDS_LANE0-		HDMI_D0M	HDMI_TX_DATA0_N						
	149	DP_LANE0+/TMDS_LANE2+		HDMI_D2P	HDMI_TX_DATA2_N						
	150	HDMI_CTRL_DAT		KEY_ROW3	HDMI_TX_DDC_SDA		I2C2_SDA			GPIO4_IO13	
	151	DP_LANE0-/TMDS_LANE2-		HDMI_D2M	HDMI_TX_DATA2_N						
	152	HDMI_CTRL_CLK		KEY_COL3	HDMI_TX_DDC_SCL	SPDIF_IN	I2C2_SCL			GPIO4_IO12	13
	153	DP_HDMI_HPD#		HDMI_HPD	HDMI_TX_HPD						

Port #	MXM Pin	MXM Pin Name	Qseven® function group	i.MX6 Pad name	i.MX6 Signal for standard function	i.MX6 Alternative Signal					Also used in Port #
21	99	eDP0_TX0+/LVDS_A0+	LVDS Dual Channel 24 bit	LVDS0_TX0_P	LVDS0_DATA0_P						
	100	eDP1_TX0+/LVDS_B0+		LVDS1_TX0_P	LVDS1_DATA0_P						
	101	eDP0_TX0-/LVDS_A0-		LVDS0_TX0_N	LVDS0_DATA0_N						
	102	eDP1_TX0-/LVDS_B0-		LVDS1_TX0_N	LVDS1_DATA0_N						
	103	eDP0_TX1+/LVDS_A1+		LVDS0_TX1_P	LVDS0_DATA1_P						
	104	eDP1_TX1+/LVDS_B1+		LVDS1_TX1_P	LVDS1_DATA1_P						
	105	eDP0_TX1-/LVDS_A1-		LVDS0_TX1_N	LVDS0_DATA1_N						
	106	eDP1_TX1-/LVDS_B1-		LVDS1_TX1_N	LVDS1_DATA1_N						
	107	eDP0_TX2+/LVDS_A2+		LVDS0_TX2_P	LVDS0_DATA2_P						
	108	eDP1_TX2+/LVDS_B2+		LVDS1_TX2_P	LVDS1_DATA2_P						
	109	eDP0_TX2-/LVDS_A2-		LVDS0_TX2_N	LVDS0_DATA2_N						
	110	eDP1_TX2-/LVDS_B2-		LVDS1_TX2_N	LVDS1_DATA2_N						
	111	LVDS_PPEN		GPIO_4	***LVDS_PPEN***					GPIO1_IO04	
	112	LVDS_BLEN		NANDF_CS0	***LVDS_BLEN***					GPIO6_IO11	
	113	eDP0_TX3+/LVDS_A3+		LVDS0_TX3_P	LVDS0_DATA3_P						
	114	eDP1_TX3+/LVDS_B3+		LVDS1_TX3_P	LVDS1_DATA3_P						
	115	eDP0_TX3-/LVDS_A3-		LVDS0_TX3_N	LVDS0_DATA3_N						
	116	eDP1_TX3-/LVDS_B3-		LVDS1_TX3_N	LVDS1_DATA3_N						
	119	eDP0_AUX+/LVDS_A_CLK+		LVDS0_CLK_P	LVDS0_CLK_P						
	120	eDP1_AUX+/LVDS_B_CLK+		LVDS1_CLK_P	LVDS1_CLK_P						
	121	eDP0_AUX-/LVDS_A_CLK-		LVDS0_CLK_N	LVDS0_CLK_N						
	122	eDP1_AUX-/LVDS_B_CLK-		LVDS1_CLK_N	LVDS1_CLK_N						
	123	LVDS_BLT_CTRL/GP_PWM_OUT0		GPIO_9	PWM1_OUT	WDOG1_B				GPIO1_IO09	
22	126	eDP0_HPD#/LVDS_BLC_DAT	---	GPIO_8	---	FLEXCAN1_RX	I2C4_SDA			GPIO1_IO08	
	128	eDP1_HPD#/LVDS_BLC_CLK		GPIO_7	---	FLEXCAN1_TX	I2C4_SCL			GPIO1_IO07	

Port #	MXM Pin	MXM Pin Name	Qseven® function group	i.MX6 Pad name	i.MX6 Signal for standard function	i.MX6 Alternative Signal					Also used in Port #
23	91	USB_VBUS	USB	DISP0_DAT14	***USB_VBUS***						
	92	USB_ID		GPIO_1	USB_OTG_ID						
	93	USBP1-		USB_OTG_DN	USB_OTG_DN						
	94	USBP0-		USB_H1_DN	USB_H1_DN						
	95	USBP1+		USB_OTG_DP	USB_OTG_DP						
	96	USBP0+		USB_H1_DP	USB_H1_DP						
24	7	GBE_LINK100#	Ethernet 10/100 BT	Not coming from i.MX6 processor but from KSZ8091RN	GBE_LINK_100						
	9	GBE_MDI1-			RX_M						
	10	GBE_MDI0-			TX_M						
	11	GBE_MDI1+			RX_P						
	12	GBE_MDI0+			TX_P						
	13	GBE_LINK#			GBE_LINK_10						
	14	GBE_ACT#			GBE_ACT#						
24	29	SATA0_TX+	SATA	---	---						
	31	SATA0_TX-		---	---						
	33	SATA_ACT#		SD2_DAT1	---	SD2_DATA1	AUD4_TXFS			GPIO1_IO14	4
	35	SATA0_RX+		---	---						
	37	SATA0_RX-		---	---						
25	70	WDTRIG#	WATCHDOG	SD2_DAT2	WDT_TRIG_OUT	SD2_DAT2	AUD4_TXD			GPIO1_IO13	4
	72	WDOUT		DISP0_DAT8	WDOG1_B	PWM1_OUT				GPIO4_IO29	

Chapter 4.
Appendices

- Thermal Design



4.1 Thermal Design

Highly integrated modules, like the µQ7-A75-J module, offer the user excellent performance in a very reduced space, therefore allowing the system's minimization. On the other hand, the miniaturizing of IC's and the increase of clock frequencies of the processors lead to the generation of a big amount of heat that must be dissipated to prevent critical operating conditions, system hang-off or failures.

It is extremely important to note that, for this reason, a critical design parameter always to be kept in very high consideration is the thermal design and analysis of the final assembled system, with the application software running.

Qseven® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the Qseven® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsinks in some situation can represent the cooling solution. Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide µQ7-A75-J specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
QA75-DISS-1-C-PK	µQ7-A75-J Heat Spreader (Passive), Packaged
QA75-DISS-2-C-PK	µQ7-A75-J HeatSink (Passive), Packaged

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