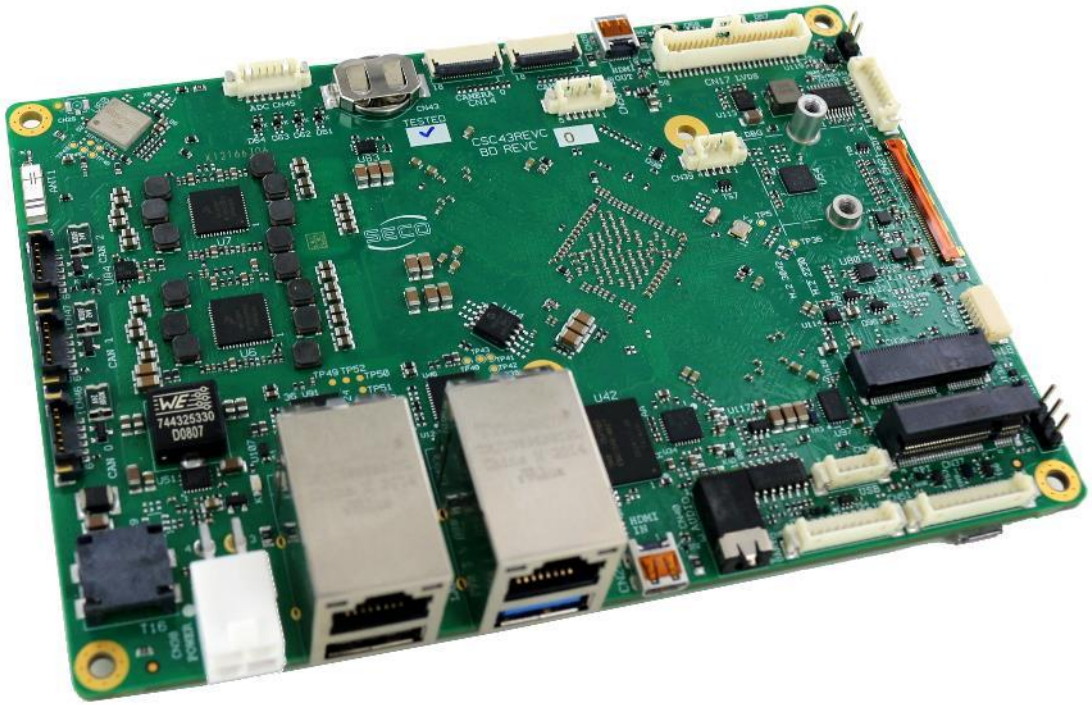
SBC

User Manual



SBC-C43

Single Board Computer
with NXP i.MX 8 Applications Processors
in 3.5” form factor

HDMI®
HIGH-DEFINITION MULTIMEDIA INTERFACE

www.seco.com

REVISION HISTORY

Revision	Date	Note	Ref
1.0	17th November 2020	First Official Release.	AR
2.0	25th November 2021	Aligned to PCB Rev.C: - LVDS pinout changed (par. 3.3.2) - M.2 Key E connector pinout updated (par. 3.3.8) - M.2 Key E I2C bus level to +3.3V updated (par. 3.3.8) - Minor corrections to M.2 signals description - Changed parts: JP2, CN45, CN18 (picture and descriptions) - Added CN56 (picture and description) - Added Trademark Notice (par. 1.8.1)	SO
2.1	7th December 2021	Added Safety Policy Corrected LVDS CN# error introduced in Rev. 2.0	SO

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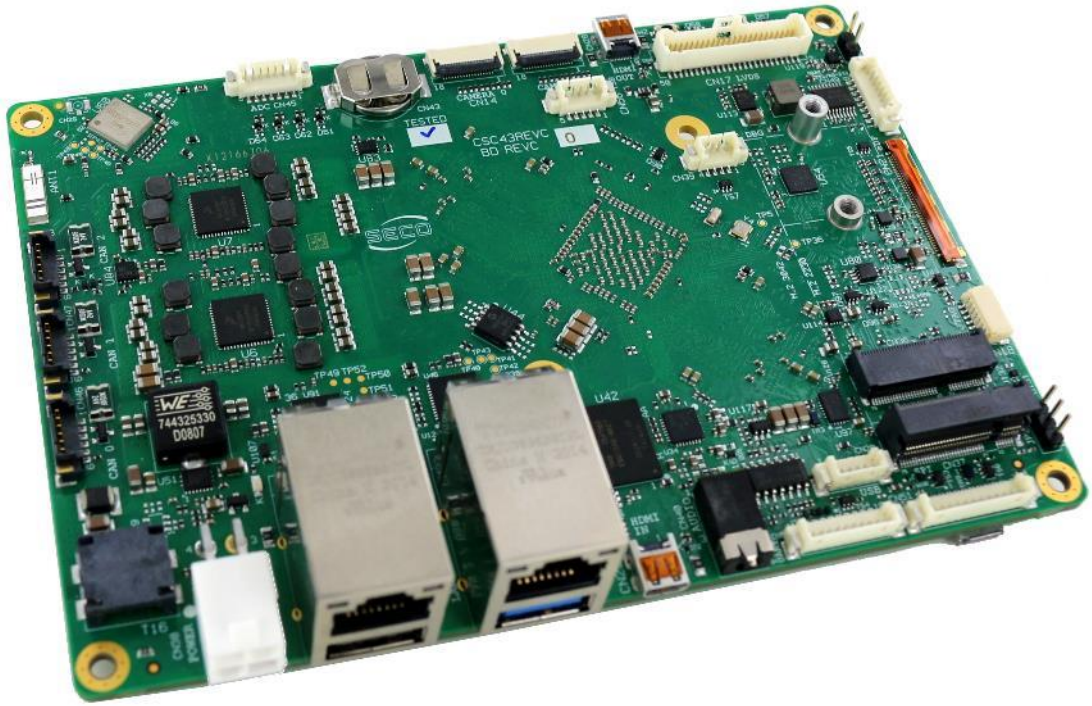
Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorized by the supplier.

The authorization is released after completing the specific form available on the web-site https://www.seco.com/it/support/online-rma.html (RMA Online). The RMA authorization number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionalities and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210
- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by an RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operative system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request an RMA number, please visit SECO's web-site. On the home page, please select "CONTACT US" then "Online RMA" and follow the procedure described.

An RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The SBC-C43 board uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic discharges

The SBC-C43 board, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

Whenever handling an SBC-C43 board, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The SBC-C43 board is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Policy

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, the SBC-C57 Module shall be:

- used exclusively with limited power sources, which cannot exceed 100W even in fault conditions;
- used along with CPU Heat-spreader/heatsinks designed according to the thermal characteristics indicated in the par. 2.2 and to the mechanical characteristics indicated in par. 2.4.
- installed inside an enclosure compliant to all applicable requirements of the above-mentioned standard;
- installed in a way that prevents the access to the board from children

The manufacturer which includes an SBC-C57 module in his end-user product shall:

- verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition.
- provide an instructional safeguard against thermal injuries, according to clause 9.4.2 of the above mentioned standard. This instructional safeguard must be placed both on end-user product's User Manual and on the product itself (Danger Label, it must be placed near the CPU or its heatsink).

The board shall be powered by a Power Supply Unit separately approved and classified ES1/PS2 according to the requirements of IEC EN 62368-1.

1.8 Terminology and definitions

API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control
CSI2	MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host processor
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
eDP	embedded Display Port
GbE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
GPU	Graphics Processing Unit
HDMI®	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
LVDS	Low Voltage Differential Signaling, a standard for transferring data at very high speed using inexpensive twisted pairs copper cables, usually used for video applications
LPDDR4	Low-Power Double Data Rate Synchronous Dynamic Random Access Memory, 4th generation
MAC	Medium Access Controller, the hardware implementing the Data Link Layer of ISO/OSI-7 model for communication systems
Mbps	Megabits per second
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface of SD. The eMMC are the embedded version of the MMC. They are devices that incorporate both the memory controller and the flash memories on a single BGA chip
N.A.	Not Applicable
N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics
OS	Operating System

OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port
PCI-e	Peripheral Component Interface Express
PHY	Abbreviation of Physical, it is the device implementing the Physical Layer of ISO/OSI-7 model for communication systems
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
RGMII	Reduced Gigabit Media Independent Interface, a particular interface defining the communication between an Ethernet MAC and a PHY
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which contemplates a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
USB	Universal Serial Bus
uSDHC	Ultra Secure Digital Host Controller
V_REF	Voltage reference Pin

1.8.1 Trademark Notice

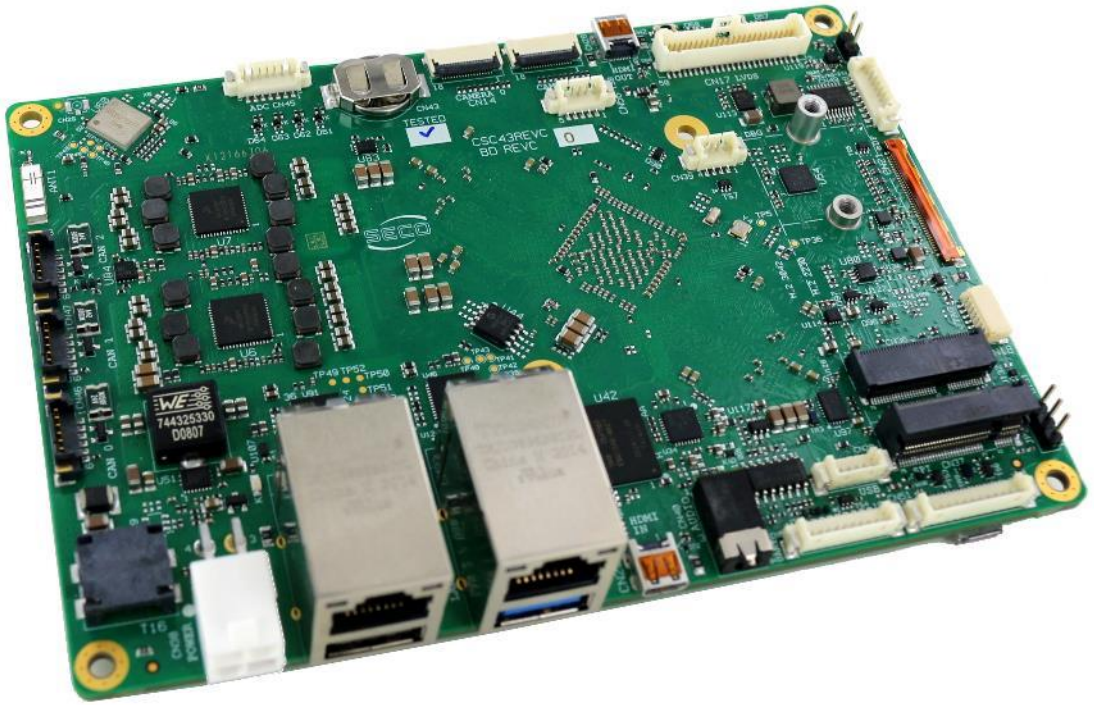
1.9 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	https://uefi.org/specifications
CAN Bus	http://esd.cs.ucr.edu/webres/can20.pdf
CSI	http://www.mipi.org/specifications/camera-interface
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
FastEthernet	http://standards.ieee.org/about/get/802/802.3.html
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HDMI®	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ug/snla187/snla187.pdf
M.2 Specifications	https://pcisig.com/specifications/pciexpress/M.2_Specification/
MMC/eMMC	https://www.jedec.org/committees/jc-64
NXP i.MX8 processor	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-8-processors/i-mx-8-family-arm-cortex-a53-cortex-a72-virtualization-vision-3d-graphics-4k-video:i.MX8
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
SD Card Association	https://www.sdcard.org
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
USB 2.0 and USB OTG	https://www.usb.org/sites/default/files/usb_20_20190524.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical specifications
- Electrical specifications
- Mechanical specifications
- Block diagram



2.1 Introduction

SBC-C43 is a Single Board Computer, measuring just 102 x 146 mm (4,02" x 5,75") based on embedded NXP i.MX 8 Family, featuring multicore processing (Single or Dual ARM Cortex®-A72 cores + Quad ARM Cortex®-A53 cores + Dual general purpose Cortex®-M4 processor).

Graphics features of the board are managed directly by NXP i.MX8 processor, which integrate 2x Graphics accelerators Vivante GC7000 / XVSX or GC7000 Lite / XVSX (QuadMax and QuadPlus) GPUs, supporting OpenGL® ES 1.1 / 2.0 / 3.0 / 3.1, Open CL 1.2 OpenGL 3.x, DirectX 11. This family of processors integrate one embedded VPU, which allows HW acceleration for video decoding of H.265 (4K30), H.264 (1080p60) and encoding of H.264 (1080p30).

The board is completed with up to 8GB LPDDR4 directly soldered on board, and one eMMC Flash Drive, directly accessible like any standard Drive, with up to 64GB of capacity. Mass storage capabilities are completed by a microSD Card slot. External SSD modules can expand mass storage capabilities through M.2 Key B Slot with S-ATA interface (factory option with PCIe x1 for plugging M.2 Modem modules)

The processor offers two RGMII interfaces which, through dedicated Ethernet Transceivers, allows the implementation of two Gigabit Ethernet interfaces.

The communication / networking capabilities of the board are completed by an M.2 Key B Slot, which allows plugging M.2 Modem modules with USB or PCI-e interface, an M.2 Key E Slot, which allows plugging M.2 WiFi + BT modules with USB or PCI-e interface and by an optional WiFi a/b/g/n/ac + BT LE 4.2 combo embedded module, with ceramic SMT antennas on-board.

The M.2 Key B Slot can rely on an on-board microSIM slot.

The SBC-C43 offers an USB 3.0 Standard Type-A connector (combo with RJ-45 GbE connector), one USB 2.0 standard Type-A connector (combo with RJ-45 GbE connector), an internal USB 2.0 header and one USB 2.0 with OTG functionalities on micro-AB socket.

The audio functionalities of this board are realised by an I2S audio codec, which manages Line out and Mic In interfaces on a combo TRRS audio jack.

The standard functionalities of this board are then completed by 3x UART interfaces (RS-232, RS-485/RS-422, TTL level), an I2C interface, four A/D inputs, an SPI interface, 6x GPIOs and three CAN Bus interfaces.

The board is available both in commercial and in industrial temperature range.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics. Not all combinations of these features are offered simultaneously; please visit SECO's website for a description of standard configuration modules offered. Configurations different from the standard offered must be evaluated singularly; please contact a SECO's sales representative / distributor for this.

2.2 Technical specifications

Processors

NXP i.MX 8 Family of processors, based on ARM® Cortex®-A72 Core + ARM® Cortex®-A53 Core + Cortex®-M4F core platform:

- i.MX 8 QuadMax: Dual A72-core, Quad A53-core, Dual M4F-core
- i.MX 8 QuadPlus: Single A72-core, Quad A53-core, Dual M4F-core

Memory

64-bit soldered down LPDDR4-1600 memory, up to 8GB total

Graphics

2x Graphics accelerators Vivante GC7000/XVSX or GC7000Lite/XVSX (QuadMax and QuadPlus)
1x embedded VPU, supporting H.265(4K30) and H.264(1080p60) decoding and H.264 (1080p30) encoding
Supports 3 independent video outputs (total combined resolution 4K)

Video Interfaces

OUTPUTS:
HDMI Tx interface
Optional eDP 1.4 interface
Optional Single/Dual-Channel 18-/24- bit LVDS interface
INPUTS:
HDMI Rx interface
2x 4-lanes MIPI-CSI Camera interfaces

Video Resolution

HDMI: up to UltraHD (4K)
LVDS, eDP: up to 1080p

Mass Storage

eMMC 5.1 Drive soldered on-board, up to 64GB
1x S-ATA interface available on M.2 Socket 2 Key B Slot
microSD Card Slot
4MB QuadSPI Flash NAND (boot device only)

Networking

2x Gigabit Ethernet interfaces
Combo WiFi 802.11 a/b/g/n/ac + BT LE 4.2 module
M.2 Socket 2 Key B Slot for M.2 Modems
M.2 Socket1 Key E Slot for WiFi + BT external modules

USB

1 x USB 3.0 Host port on Type-A socket
1x USB 2.0 OTG port on micro-AB socket
1x USB 2.0 Host port on external Type-A socket
1x USB 2.0 Host port on internal connector
2 x USB 2.0 ports available on M.2 Key B and Key E slots

PCI-e

2x PCI-e x1 ports, available on M.2 Socket 1 Key E and on M.2 Socket 2 Key B

Audio

I2S Audio Codec
HP + MIC combo TRRS audio connector

Serial Ports

1 x UART TTL
1 X RS-232 / UART TTL configurable
1 x RS-485 / RS-422 / UART TTL configurable
3x CAN interfaces

Other interfaces

4x Analog Inputs
6x GPIOs
SPI interface
I2C interface
Embedded additional RTC circuitry for lowest power consumption
SIM dedicated slot

Power supply voltage: $+12V_{DC}$ ± 10%

Operating temperature**: 0°C ÷ +60°C (commercial version)
-40°C ÷ +85°C (industrial version)

Dimensions: 146 x 102 mm (5,75" x 4,02")

Supported Operating Systems:

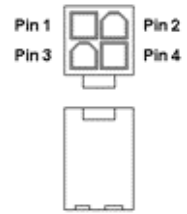
Wind River Linux
Yocto
Android

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated.*

Please also check paragraph 4.1

2.3 Electrical specifications

SBC-C43 needs to be supplied only with an external $12V_{DC}$ ± 10% power supply, with a minimal 60W power rating (SBC-C43 power consumption by itself is around 18W, more power is required for the possible attached devices).



Power In Connector – CN38			
Pin	Signal	Pin	Signal
1	GND	3	VIN_SYS
2	GND	4	VIN_SYS

This voltage can be supplied through a Right-angle connector type Molex Mini-Fit Jr, p/n 39-30-0040 or equivalent, with the pinout indicated in the table below.

2.3.1 Power requirement

When powering SBC-C43 with a PSU with characteristics greater or equal to the one described in paragraph 2.3, please consider thoroughly the use scenario of the board (i.e., which peripherals will be connected)

Since all the power must be supplied by a single external PSU, it must be cumulated the power consumption of the board itself with that of all external devices.

This way it is possible to calculate preliminarily if a 60W PSU can be sufficient for the cumulated power requirements or a more powerful PSU is required.

2.3.2 RTC Battery

The SBC-C43 board can be equipped with an optional low-power Real Time Clock embedded on the module (which is a NXP PCF2123).

If the board is not equipped with the optional rechargeable battery, then it will be available a soldered horizontal 3V coin cell lithium battery to supply the RTC.

The battery used is a not-rechargeable CR1225 Lithium coin-cell battery, with a nominal capacity of 48mAh, to supply such an RTC. The battery must be plugged on the onboard battery holder CN43.

In case of exhaustion, the battery should only be replaced with devices of the same type. Always check the orientation before inserting and make sure that they are aligned correctly and are not damaged or leaking.

Never allow the batteries to become short-circuited during handling.

! CAUTION: handling batteries incorrectly or replacing with not-approved devices may present a risk of fire or explosion.

Batteries supplied with SBC-C43 are compliant to requirements of European Directive 2006/66/EC regarding batteries and accumulators. When putting out of order SBC-C43, remove the batteries from the board in order to collect and dispose them according to the requirement of the same European Directive above mentioned. Even when replacing the batteries, the disposal has to be made according to these requirements.

2.3.3 Power consumption

Using the following setup, the current consumption has been measured on +12VDC V_{IN} power line.

- CPU: i.MX8 QuadMax
- 8GB LPDDR4
- 16GB eMMC onboard
- HDMI FHD display connected (no additional peripherals)

Status	Average Value		Peak Value	
Idle	6.63W	0.55A	6.71W	0.56A
OS Boot	--	--	10.7W	0.891A
Video reproduction 1080p 60fps	8.02W	0.668A	8.51W	0.708A
Stress Test 1	8.36W	0.696A	9.29W	0.774A
Stress Test 2	11.89W	0.99A	13.43W	1.119A
Stress Test 3	13.06W	1.087A	15.03W	1.251A
Stress Test 4	17.37W	1.446A	18.1W	1.507A

2.3.4 Power rails naming convention

In all the tables contained in this manual, Power rails are named with the following meaning:

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

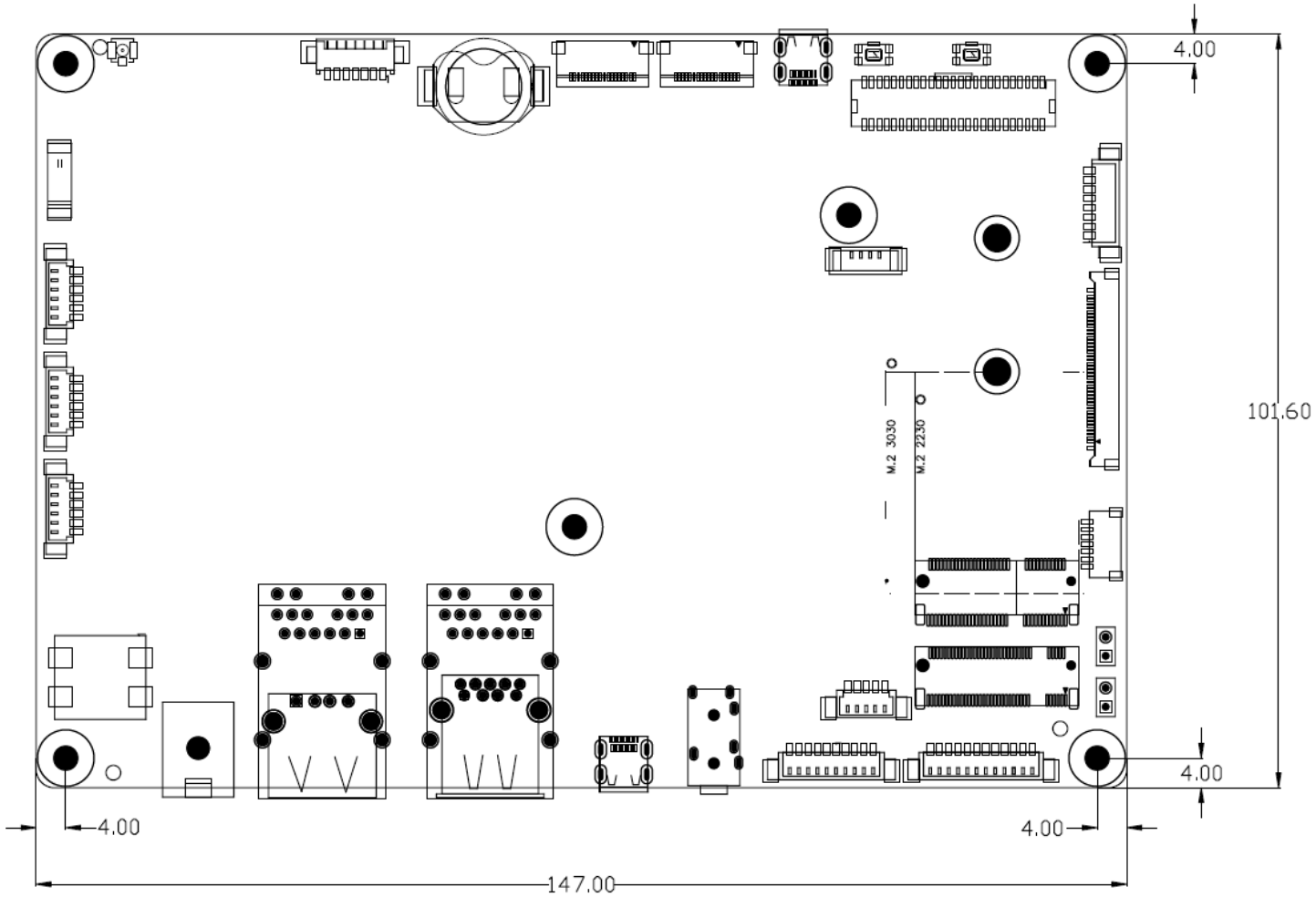
_U: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_U

Other suffixes are used for application specific power rails, which are derived from same voltage value of voltage switched rails, if it is not differently stated (for example, $+5V_{HDMI}$ is derived from +5V_RUN, and so on).

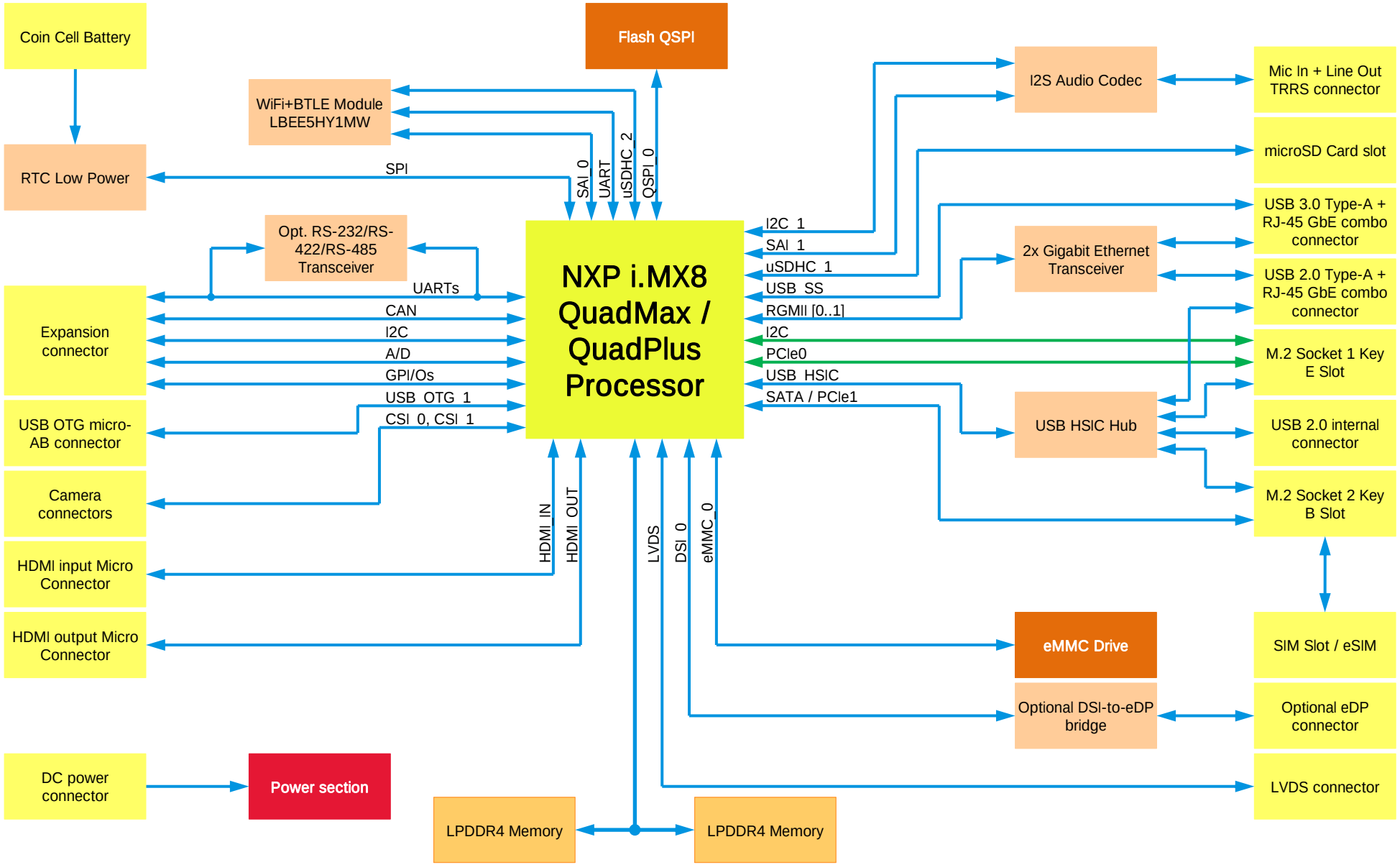
2.4 Mechanical specifications

Board dimensions are 146 x 102 mm (5,75” x 4,02”).

The printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

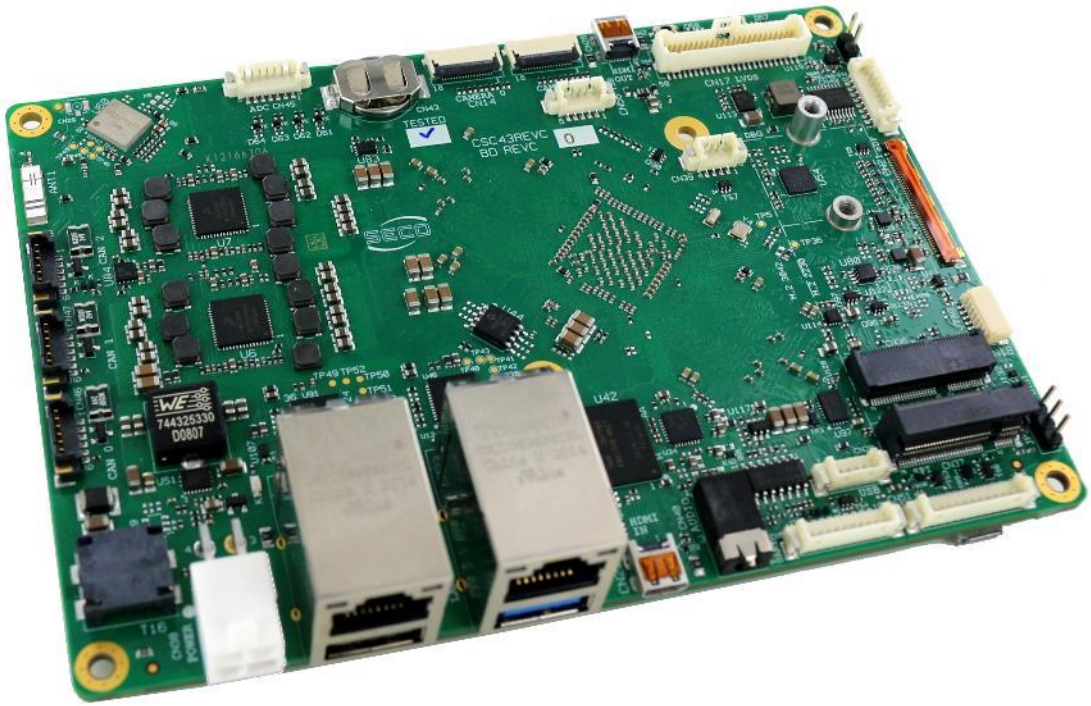


2.5 Block diagram



Chapter 3.
CONNECTORS

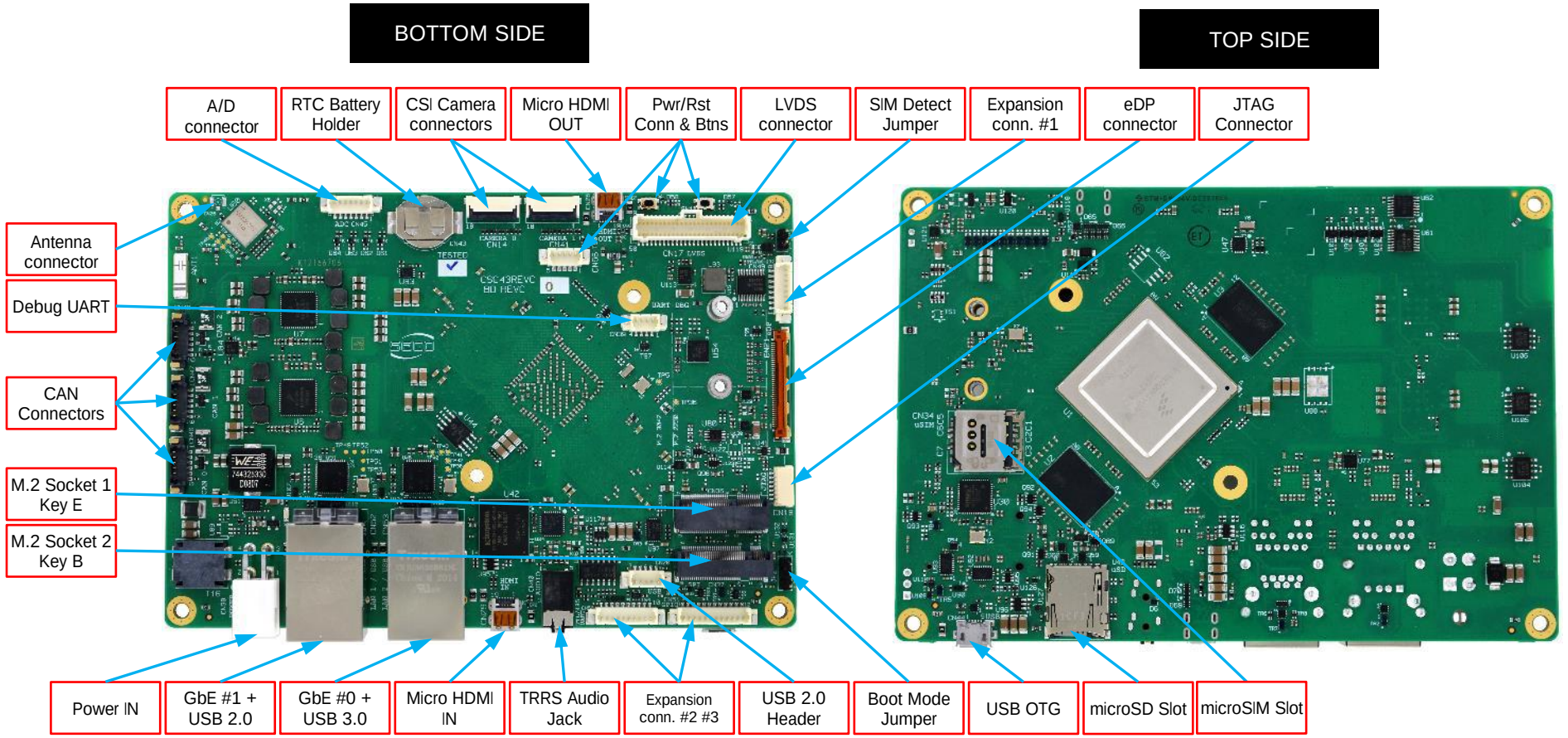
- Introduction
- Connectors overview
- Connectors description



3.1 Introduction

On SBC-C43 board, there are several connectors located on the upper plane. Standard connectors are placed on the same side of PCB, so that it is possible to place them on a panel of an eventual enclosure.

> ! Please be aware that, depending on the configuration purchased, the appearance of the board can be significantly different from the following pictures.



3.2 Connectors overview

Name	Description	Name	Description
CN14	MIPI-CSI #0 Camera Connector	CN43	RTC Battery Holder
CN17	LVDS Connector	CN44	USB 2.0 OTG micro-AB Connector
CN18	JTAG Connector	CN45	A/D Header
CN20	USB 2.0 internal header	CN46	CAN Bus #0 Connector
CN21	eDP Connector	CN47	CAN Bus #1 Connector
CN26	External Antenna u.FL Connector	CN48	CAN Bus #2 Connector
CN28	HDMI output Micro Connector (Type D)	CN49	Expansion connector #1
CN29	HDMI input Micro Connector (Type D)	CN50	Expansion connector #2
CN34	microSIM card Slot	CN51	Expansion connector #3
CN36	M.2 Socket 1 Key E Slot	CN52	Combo GbE #1 + USB 2.0 Type-A connector
CN37	M.2 Socket 2 Key B Slot	CN53	Combo GbE #0 + USB 3.0 Type-A connector
CN38	Power In Connector	CN56	Power and Reset Connector
CN39	Debug UART Connector	U43	microSD Slot
CN40	TRRS Audio Jack	SW1	Reset Button
CN41	MIPI-CSI #1 Camera Connector	SW2	Power Button

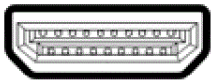
3.2.1 Jumper List

Name	Description	Name	Description
JP1	SIM Detect	JP2	Boot Mode

3.3 Connectors description

3.3.1 HDMI Connectors

HDMI Out Connector – CN28			
Pin	**Signal**	**Pin**	**Signal**
1	HPD	2	----
3	HDMI_TX2+	4	GND
5	HDMI_TX2-	6	HDMI_TX1+
7	GND	8	HDMI_TX1-
9	HDMI_TX0+	10	GND
11	HDMI_TX0-	12	HMDI_CLK+
13	GND	14	HDMI_CLK-
15	CEC	16	GND
17	SCL	18	SDA
19	$+5V_{HDMI}$		



NXP i.MX8 family of processor has an embedded HDMI technology Tx module, which provides an HDMI interface for compliant displays.

For this reason, on SBC-C43 board there is the possibility of connecting one HDMI display, using a certified HDMI Micro Connector (Type D), CN28, type FCI p/n 10118242-001RLF.

Signals involved in HDMI Tx management are the following:

HMDI_CLK+/HMDI_CLK-: TMDS differential Clock.

HDMI_TX0+/ HDMI_TX0-: TMDS differential pair #0

HDMI_TX1+/ HDMI_TX1-: TMDS differential pair #1

HDMI_TX2+/ HDMI_TX2-: TMDS differential pair #2

SDA: DDC Data line for HDMI panel. Bidirectional signal, electrical level $+5V_{HDMI}$ with a 2kΩ pull-up resistor.

SCL: DDC Clock line for HDMI panel. Output signal, electrical level $+5V_{HDMI}$ with a 2kΩ pull-up resistor.

CEC: HDMI Consumer Electronics Control (CEC) Line. Bidirectional signal, electrical level +3.3V_RUN with a 27kΩ pull-up resistor.

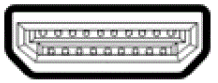
HPD: Hot Plug Detect Input signal. +3.3V_RUN electrical level signal with 1MΩ pull-down resistor.

$+5V_{HDMI}$: Power voltage reference for HDMI, directly derived from +5V_RUN.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

Always use HDMI-certified cables for the connection between the board and the HDMI display; a Standard HDMI Cable can be used for 720p resolution, while a High-Speed HDMI Cable is recommended for higher resolutions.

HDMI In Connector – CN29			
Pin	**Signal**	**Pin**	**Signal**
1	HPD	2	----
3	HDMI_RX2+	4	GND
5	HDMI_RX2-	6	HDMI_RX1+
7	GND	8	HDMI_RX1-
9	HDMI_RX0+	10	GND
11	HDMI_RX0-	12	HMDI_CLK+
13	GND	14	HDMI_CLK-
15	CEC	16	GND
17	SCL	18	SDA
19	$+5V_{SINK}$		



NXP i.MX8 family of processor also embeds an HDMI technology Rx module, which provides acquisition of HDMI compliant sources.

For this reason, on SBC-C43 board there is the possibility of connecting one HDMI source, using a certified HDMI Micro Connector (Type D), CN28, type FCI p/n 10118242-001RLF. This is a factory option and is not available on all configurations.

Signals involved in HDMI Rx management are the following:

HMDI_CLK+/HMDI_CLK-: TMDS differential Clock.

HDMI_RX0+/ HDMI_RX0-: TMDS differential pair #0

HDMI_RX1+/ HDMI_RX1-: TMDS differential pair #1

HDMI_RX2+/ HDMI_RX2-: TMDS differential pair #2

SDA: DDC Data line for HDMI panel. Bidirectional signal, electrical level $+5V_{SINK}$ with a 2kΩ pull-up resistor.

SCL: DDC Clock line for HDMI panel. Output signal, electrical level $+5V_{SINK}$ with a 2kΩ pull-up resistor.

CEC: HDMI Consumer Electronics Control (CEC) Line. Bidirectional signal, electrical level +3.3V_RUN with a 27kΩ pull-up resistor.

HPD: Hot Plug Detect Input signal. +3.3V_RUN electrical level signal with 1MΩ pull-down resistor.

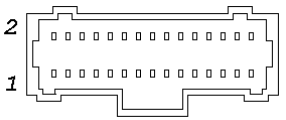
$+5V_{SINK}$: HDMI Input 5V Voltage reference.

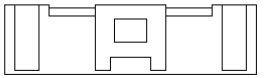
For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

Always use HDMI-certified cables for the connection between the board and the HDMI display; a Standard HDMI Cable can be used for 720p resolution, while a High-Speed HDMI Cable is recommended for higher resolutions.

3.3.2 LVDS Connector

LVDS connector – CN17			
Pin	Signal	Pin	Signal
1	LVDS_VCC_LCD_SW	2	LVDS_VCC_BKL_SW
3	LVDS_VCC_LCD_SW	4	LVDS_VCC_BKL_SW
5	LVDS_VCC_LCD_SW	6	LVDS_VCC_BKL_SW
7	3.3V_RUN	8	GND
9	GND	10	LVDS_A0+
11	LVDS_A1+	12	LVDS_A0-
13	LVDS_A1-	14	GND
15	GND	16	LVDS_A2+
17	LVDS_A3+	18	LVDS_A2-
19	LVDS_A3-	20	GND
21	GND	22	LVDS_A_CLK+
23	LVDS_B0+	24	LVDS_A_CLK-
25	LVDS_B0-	26	GND
27	GND	28	LVDS_B1+
29	LVDS_B2+	30	LVDS_B1-
31	LVDS_B2-	32	GND
33	GND	34	LVDS_B3+
35	LVDS_B_CLK+	36	LVDS_B3-
37	LVDS_B_CLK-	38	GND
39	GND	40	GND
41	BLT_EN	42	BLT_CTRL
43	LVDS_BLT_ANA	44	LVDS_PPEN
45	TOUCH_SCL	46	TOUCH_RST
47	TOUCH_SDA	48	TOUCH_INT#
49	TOUCH_SDA	50	TOUCH_SCL





In addition to HDMI, SBC-C43 board can be interfaced to LCD displays using its LVDS interface, which allows the connection of displays with a colour depth of 18 or 24 bit, single or dual channel.

For the connection, a connector type HR A1014WV-S-2X25P or equivalent (2 x 25p, male, straight, P1, low profile, polarized) is provided, with the pin-out shown in the table below.

Mating connector: HR A1014H -2X25P with HR A1014-T female crimp terminals.

Alternative mating connector, MOLEX 501189-5010 with crimp terminals series 501334.

On the same connectors, are also implemented signals for direct driving of display's backlight: voltages (LVDS_VCC_LCD_SW and LVDS_VCC_BKL_SW) and control signals (LCD Panel enable signal LVDS_PPEN, Backlight enable signal BLT_EN, digital and analog Backlight Brightness Control signal, respectively BLT_CTRL and LVDS_BLT_ANA).

The LCD software-driven voltage, i.e. signal LVDS_VCC_LCD_SW, can be factory regulated to be connected to +5V_ALW or +3.3V_ALW, while backlight software-driven voltage, i.e. signal LVDS_VCC_BKL_SW, can be factory regulated to be connected to +5V_ALW or +12V_ALW

These are factory configurations, please take care of specifying which is the configuration needed for EDP_VCC_LCD_SW and EDP_VCC_BKL_SW voltage rail.

There are also signals necessary for driving I2C touchscreens (I2C signals, reset and interrupt request signals).

When building a cable for connection of LVDS displays, please take care of twist as tight as possible differential pairs' signal wires, in order to reduce EMI interferences. Shielded cables are also recommended.

Here following the signals related to LVDS management:

LVDS_A0+ / LVDS_A0-: LVDS Channel #0 differential data pair #0.

LVDS_A1+ / LVDS_A1-: LVDS Channel #0 differential data pair #1.

LVDS_A2+ / LVDS_A2-: LVDS Channel #0 differential data pair #2.

LVDS_A3+ / LVDS_A3-: LVDS Channel #0 differential data pair #3.

LVDS_A_CLK+ / LVDS_A_CLK-: LVDS Channel #0 differential Clock.

LVDS_B0+ / LVDS_B0-: LVDS Channel #1 differential data pair #0.

LVDS_B1+ / LVDS_B1-: LVDS Channel #1 differential data pair #1.

LVDS_B2+ / LVDS_B2-: LVDS Channel #1 differential data pair #2.

LVDS_B3+ / LVDS_B3-: LVDS Channel #1 differential data pair #3.

LVDS_B_CLK+ / LVDS_B_CLK-: LVDS Channel #1 differential Clock.

BLT_EN: VCC_LCD electrical level Output with a 10kΩ pull-up resistor, Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected displays.

LVDS_PPEN: VCC_LCD electrical level Output with a 10kΩ pull-up resistor, Panel Power Enable signal. It can be used to turn On/Off the connected display.

BLT_CTRL: this signal can be used to adjust the backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations (VCC_LCD electrical level).

LVDS_BLT_ANA: Analog dimming for LVDS panel backlight, electrical level ranging from 0V up to VCC_LCD

TOUCH_SCL: I2C Bus clock line on pin 45 and 50. Bidirectional signal, electrical level VDD_3V3 with a 2K2Ω pull-up resistor. It is managed by the processor's LVDS0_I2C1_SCL.

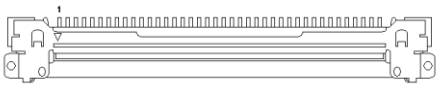
TOUCH_SDA: I2C Bus data line on pin 47 and 49. Bidirectional signal, electrical level VDD_3V3 with a 2K2Ω pull-up resistor. It is managed by the processor's LVDS0_I2C1_SDA.

TOUCH_RST: VDD_3V3 electrical level output, active high signal with a 10kΩ pull-down resistor. This signal can be used to drive a reset of an eventual external Touch Screen connected to the dedicated I2C interface.

TOUCH_INT#: VDD_3V3 electrical level input, active low signal with a 10kΩ pull-up resistor. This signal can be used to serve the interrupt request of an eventual external Touch Screen connected to the dedicated I2C interface.

3.3.3 eDP Connector

eDP connector – CN21			
Pin	**Signal**	**Pin**	**Signal**
1	---	21	EDP_VCC_LCD_SW
2	EDP_VCC_BKL_SW	22	EDP_VCC_LCD_SW
3	EDP_VCC_BKL_SW	23	EDP_VCC_LCD_SW
4	EDP_VCC_BKL_SW	24	GND
5	EDP_VCC_BKL_SW	25	eDP_AUX_N
6	---	26	eDP_AUX_P
7	---	27	GND
8	eDP_BKL_CTRL	28	eDP_ML0P
9	eDP_BKL_ON	29	eDP_ML0N
10	GND	30	GND
11	GND	31	eDP_ML1P
12	GND	32	eDP_ML1N
13	GND	33	GND
14	eDP_HPD	34	eDP_ML2P
15	GND	35	eDP_ML2N
16	GND	36	GND
17	GND	37	eDP_ML3P
18	GND	38	eDP_ML3N
19	---	39	GND
20	EDP_VCC_LCD_SW	40	---



SBC-C43 offers an optional dedicated embedded Display Port interface.

This interface is realized through Texas Instrument SN65DSI86 MIPI® DSI to eDP™ bridge, connected from one channel of the four-lane MIPI display serial interface to eDP interface of the VESA connector.

For the connection of this kind of displays, on-board there is a VESA® certified connectors for embedded Display Port interface, type STARCONN p/n 300E40-0110RA-G3 or equivalent (microcoaxial cable connector, 0.5mm pitch, 40 positions).

On this connector, EDP_VCC_BKL_SW and EDP_VCC_LCD_SW are the software-enabled voltage rails that can be used to supply the LCD and related Backlight Unit.

The LCD software-driven voltage, i.e. signal EDP_VCC_LCD_SW, can be factory regulated to be connected to +5V_ALW or +3.3V_ALW, while backlight software-driven voltage, i.e. signal EDP_VCC_BKL_SW, can be factory regulated to be connected to +5V_ALW or +12V_ALW

These are factory configurations, please take care of specifying which is the configuration needed for EDP_VCC_LCD_SW and EDP_VCC_BKL_SW voltage rail.

Here following the signals involved in eDP management:

eDP_ML0P/eDP_ML0N : embedded DP differential data pair #0.

eDP_ML1P/eDP_ML1N : embedded DP differential data pair #1.

eDP_ML2P/eDP_ML2N : embedded DP differential data pair #2.

eDP_ML3P/eDP_ML3N : embedded DP differential data pair #3.

eDP_AUXN/eDP_AUXP: embedded DP auxiliary channel differential data pair.

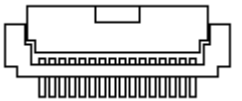
eDP_HPD: embedded DP Hot Plug Detect. +3.3V_RUN electrical level signal.

eDP_BKL_CTRL: this signal can be used to adjust the backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations , electrical level +3.3V_RUN.

eDP_BKL_ON: Backlight enable signal, electrical level +3.3V_RUN.

3.3.4 CSI Camera Connectors

SBC-C43 with NXP iMX8 Processor includes an Image Processing Subsystem, that can be used for video applications, like video-preview, video recording and frame grabbing. It is possible to access to the two embedded video input ports through as many FFC/FPC optional connectors, type OMRON p/n XF2M-1815-1A which are able to accept 18 poles 0.5mm pitch FFC cables.



CSI Camera Connector #0 – CN14

Pin	Signal	Pin	Signal
1	CSI_P0_DN3	10	CSI_P0_DN0
2	CSI_P0_DP3	11	CSI_P0_DP0
3	CSI_P0_DN2	12	GND
4	CSI_P0_DP2	13	MIPI_CSI0_PWDN
5	CSI_P0_DN1	14	MIPI_CSI0_MCKL_OUT
6	CSI_P0_DP1	15	MIPI_CSI0_I2C0_SCL
7	CSI_P0_CKN	16	MIPI_CSI0_I2C0_SDA
8	CSI_P0_CKP	17	MIPI_CSI0_RST_B
9	GND	18	+3.3V_RUN

CSI Camera Connector #1 – CN41

Pin	Signal	Pin	Signal
1	CSI_P1_DN3	10	CSI_P1_DN0
2	CSI_P1_DP3	11	CSI_P1_DP0
3	CSI_P1_DN2	12	GND
4	CSI_P1_DP2	13	MIPI_CSI1_PWDN
5	CSI_P1_DN1	14	MIPI_CSI1_MCKL_OUT
6	CSI_P1_DP1	15	MIPI_CSI1_I2C0_SCL
7	CSI_P1_CKN	16	MIPI_CSI1_I2C0_SDA
8	CSI_P1_CKP	17	MIPI_CSI1_RST_B
9	GND	18	+3.3V_RUN

All CSI differential pairs are managed by i.MX8 CSI Host Controller's Camera Input Ports #0 and #1 which are exposed respectively on CN14 and C41.

Signals description equivalent for Port #0 and Port #1:

CSI_Px_DP0 / CSI_Px_DN0: CSI2 Camera serial input, Receiving Input Differential pair #0.

CSI_Px_DP1 / CSI_Px_DN1: CSI2 Camera serial input, Receiving Input Differential pair #1.

CSI_Px_DP2 / CSI_Px_DN2: CSI2 Camera serial input, Receiving Input Differential pair #2.

CSI_Px_DP3 / CSI_Px_DN3: CSI2 Camera serial input, Receiving Input Differential pair #3.

CSI_Px_CKP / CSI_Px_CKN: CSI Camera, Clock input differential pair.

MIPI_CSIx_PWDN: External camera module Power down signal. It is an active high signal with electrical level +1.8V_RUN.

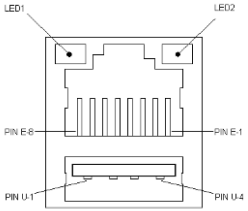
MIPI_CSIx_MCKL_OUT: Master Clock, it is managed by CSI Host Controller. It is suggested, however, to use camera modules with onboard crystal / oscillator, and avoid using this signal. Indeed, it could cause problems for EMI compliance requirements.

MIPI_CSIx_I2C0_SCL: general purpose I2C Bus clock line. Output signal, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

MIPI_CSIx_I2C0_SDA: general purpose I2C Bus data line. Bidirectional signal, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

MIPI_CSIx_RST_B: External camera module reset signal output, it is an active low signal.

3.3.5 Gigabit Ethernet + USB Connectors



On SBC-C43 board it is possible to have up to two Gigabit Ethernet connectors, managed using as many DP83867CR GbE Transceivers.

Each one of these optional connections is available on a combo connector, where the GbE interface is coupled to an USB interface.

More specifically, on connector CN52, type TRXCOM p/n TRJU3836B81N, with 2kV decoupling capacitors, it is available GbE LAN port #1 along with USB 2.0 downstream port #3, managed by the USB HSIC Hub.

Combo GbE #1 + USB 2.0 connector – CN52	
Pin	**Signal**
U1	$+5V_{USB3}$
U2	USB_P3-
U3	USB_P3+
U4	GND
E1	ETH1_MDI0+
E2	ETH1_MDI0-
E3	ETH1_MDI1+
E4	ETH1_MDI2+
E5	ETH1_MDI2-
E6	ETH1_MDI1-
E7	ETH1_MDI3+
E8	ETH1_MDI3-

Signals description:

USB_P3+/USB_P3-: USB Port #3 differential pair; it is managed by Microchip USB4604 Hub controller's Downstream Port #3.

$+5V_{USB3}$ voltage is derived from +5V_ALW power rail using a 600mA power switch.

ETH1_MDI0+/ETH1_MDI0-: Ethernet Controller Media Dependent Interface (MDI) I/O differential pair #0. It is the first differential pair in Gigabit Ethernet mode, and the Transmit differential pair in 10/100 Mbps modes.

ETH1_MDI1+/ ETH1_MDI1-: Ethernet Controller Media Dependent Interface (MDI) I/O differential pair #1. It is the second differential pair in Gigabit Ethernet mode, and the Receive differential pair in 10/100 Mbps modes.

ETH1_MDI2+/ ETH1_MDI2-: Ethernet Controller Media Dependent Interface (MDI) I/O differential pair #2. It is the third differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

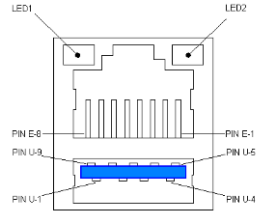
ETH1_MDI3+/ ETH1_MDI3-: Ethernet Controller Media Dependent Interface (MDI) I/O differential pair #3. It is the fourth differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

On the connector there are also two LEDs for each port. Left LED is bicolor (Orange / Green) and shows 10/100 or 1000 connection: orange means 100Mbps connection, green means 1000Mpbs connection, when the LED is Off then 10Mpbs or no connection is available. The right LED is Yellow and shows ACTIVITY presence.

This interface is compatible both with Gigabit Ethernet (1000Mbps) and with Fast Ethernet (10/100Mbps) Networks. It will configure automatically to work with the existing network.

Please be aware that they will work in Gigabit mode only in case that they are connected to Gigabit Ethernet switches/hubs/routers. For the connection, cables category Cat5e or better are required. Cables category Cat6 are recommended for noise reduction and EMC compatibility issues, especially when the length of the cable is significant.

Instead on connector CN53, type TRXCOM p/n TRJU3636B81NL, with 2kV decoupling capacitors, it is available GbE LAN port #0 along with USB 3.0 port #3, directly managed by the i.MX8 processor.



Combo GbE #0 + USB 3.0 connector – CN53	
Pin	**Signal**
U1	$+5V_{USB}$
U2	USB_H1-
U3	USB_H1+
U4	GND
U5	USB_SSRX1-
U6	USB_SSRX1+
U7	GND
U8	USB_SSTX1-
U9	USB_SSTX1+
E1	ETH0_MDI0+
E2	ETH0_MDI0-
E3	ETH0_MDI1+
E4	ETH0_MDI2+
E5	ETH0_MDI2-
E6	ETH0_MDI1-
E7	ETH0_MDI3+
E8	ETH0_MDI3-

Signals description:

USB_H1+/USB_H1-: USB 2.0 Host Port #1 differential pair;

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair;

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair;

+5VUSB voltage is derived from +5V_ALW power rail using a 1A power switch.

Common mode chokes are placed on all USB differential pairs for EMI compliance. For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

ETH0_MDI0+/ETH1_MDI0-: Ethernet Controller Media Dependent Interface (MDI) I/O differential pair #0. It is the first differential pair in Gigabit Ethernet mode, and the Transmit differential pair in 10/100 Mbps modes.

ETH0_MDI1+/ ETH1_MDI1-: Ethernet Controller Media Dependent Interface (MDI) I/O differential pair #1. It is the second differential pair in Gigabit Ethernet mode, and the Receive differential pair in 10/100 Mbps modes.

ETH0_MDI2+/ ETH1_MDI2-: Ethernet Controller Media Dependent Interface (MDI) I/O differential pair #2. It is the third differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

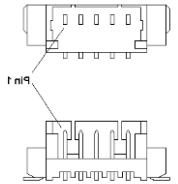
ETH0_MDI3+/ ETH1_MDI3-: Ethernet Controller Media Dependent Interface (MDI) I/O differential pair #3. It is the fourth differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

On the connector there are also two LEDs for each port. Left LED is bicolor (Orange / Green) and shows 10/100 or 1000 connection: orange means 100Mbps connection, green means 1000Mpbs connection, when the LED is Off then 10Mpbs or no connection is available. The right LED is Yellow and shows ACTIVITY presence.

This interface is compatible both with Gigabit Ethernet (1000Mbps) and with Fast Ethernet (10/100Mbps) Networks. It will configure automatically to work with the existing network.

Please be aware that they will work in Gigabit mode only in case that they are connected to Gigabit Ethernet switches/hubs/routers. For the connection, cables category Cat5e or better are required. Cables category Cat6 are recommended for noise reduction and EMC compatibility issues, especially when the length of the cable is significant.

3.3.6 USB Connectors



On SBC-C43 board there are two USB ports directly available on external connectors.

The USB downstream port #4 managed by the USB HSIC Hub is available on a 5-pin p1.27mm connector type Molex p/n 53398-0571 or equivalent, with pinout shown in the table on the left.

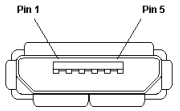
USB 2.0 Internal Header – CN20	
Pin	**Signal**
1	$+5V_{USB4}$
2	USB_P4-
3	USB_P4+
4	GND
5	SHLD (GND)

Mating connector: MOLEX 51021-0500 receptacle with 50079-8000 female crimp terminals.

Signal Description of this port:

USB_P4+/USB_P4-: USB Port #4 differential pair; it is managed by Microchip USB4604 Hub controller's Downstream Port #4.

$+5V_{USB4}$ voltage is derived from +5V_ALW power rail using a 600mA power switch.



In addition, there is an USB OTG Port, managed directly by the i.MX8 processor, which is carried to a standard micro-AB connector, described in the table on the left.

USB micro-AB connector – CN44	
Pin	**Signal**
1	USB_VBUS
2	USB_OTG_D-
3	USB_OTG_D+
4	USB_ID
5	SHLD (GND)

Depending on the needed use of the system, it is necessary to connect micro-A or micro-B USB cables to connector CN44

A micro-A USB cable has to be used when the system has to work in Host mode. In this case, USB_VBUS is a power output of SBC-C43 Board for the connected device.

When a micro-B USB cable is used, its USB_ID pin is floating; this way, the board acknowledges that it must configure itself to work as a Client. In this case, USB_VBUS is an input of the carrier board from the external Host.

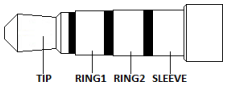
Signal description of this port:

USB_OTG_D+/USB_OTG_D-: USB OTG Port #1 differential pair.

USB_VBUS: USB voltage rail. It is an input for USB port working in Client mode, an output for Host mode.

USB_ID: Client/Host identification signal. This signal is high when the USB port works in client mode, is low when works in Host mode.

3.3.7 TRSS Audio jack



On SBC-C43 board, audio functionalities are controlled by an I2S Audio Codec type TLV320AIC3204IRHBR.

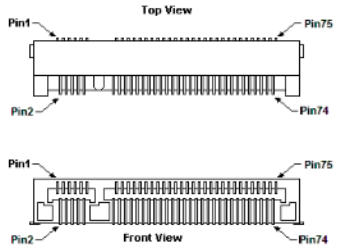
It is possible to have Stereo Line Out and Mic In Audio functionalities, all of them on a single TRRS Combo Audio Jack, i.e. a single jack which offer both stereo Line Out and Mic In functionalities.

TRRS Audio jack- CN40	
Pin	**Signal**
TIP	Headphone Out Left Channel
RING1	Headphone Out Right Channel
RING2	GND
SLEEVE	MIC_IN

Such TRRS Combo Audio jack can be used with any 4-poles 3.5mm diameter audio jack, with pinout compatible with the most recent Headsets, shown in the table on the left.

3.3.8 M.2 2230 Socket 1 Key E Connectivity Slot

It is possible to increase the connectivity of the SBC-C43 board by using M.2 Socket 1 Key E connectivity slot.



M.2 Connectivity Slot (Socket 1 Key E type 2230) – CN36

Pin	Signal	Pin	Signal
1	GND	2	+3.3V_RUN
3	USB_P2+	4	+3.3V_RUN
5	USB_P2-	6	---
7	GND	8	---
9	---	10	---
11	---	12	---
13	---	14	---
15	---	16	---
17	---	18	M2_KEYE_PRST#
19	---	20	---
21	---	22	---
23	---	32	---
33	GND	34	---
35	PCIE1_TX0+	36	---
37	PCIE1_TX0-	38	---
39	GND	40	---
41	PCIE1_RX0+	42	---
43	PCIE1_RX0-	44	---
45	GND	46	---
47	PCIE_KEYE_CLK+	48	---

The connector used for the M.2 Connectivity slot is CN36, which is a standard 75 pin M.2 Key E connector, type LOTES p/n APCI0076-P001A, H=4.2mm, with the pinout shown in the table on the left.

On the SBC-C43 board there is also a Threaded Spacer which allows the placement of M.2 Socket 1 Key E connectivity modules in 2230 size.

Signals Description

USB_P2+ / USB_P2-: USB Port #2 differential pair; it is managed by Microchip USB4604 Hub controller's Downstream Port #2.

M2_KEYE_PRST#: M.2 Key E input for detection when a module is inserted in the slot. Active low signal, electrical level +3.3V_RUN with a 100KΩ pull-up resistor.

PCIE1_TX+/PCIE1_TX-: PCI Express lane #1, Transmitting Output Differential pair

PCIE1_RX+/PCIE1_RX-: PCI Express lane #1, Receiving Input Differential pair

PCIE_KEYE_CLK+ / PCIE_KEYE_CLK-: Dedicated PCI Express Reference Clock

PCIE_CTL1_RST1#: Reset Signal that is sent from the SoC to all PCI-e devices available on the board. It is a +3.3V_RUN active-low signal with 100kΩ pull-down.

PCIE_CTL1_CLK_REQ: PCI-e Clock Request Input. Active low signal, electrical level +3.3V_RUN with a 47KΩ pull-up resistor. This signal shall be driven low by any module inserted in the connectivity slot, in order to ensure that the SoC makes available the reference clock.

PCIE_CTL1_WAKE: Board's Wake Input, it must be externally driven by the module inserted in the slot when it requires waking up the system. Active low signal, electrical level +3.3V_RUN with a 47KΩ pull-up resistor

M2_KEYE_W_DIS1# / M2_KEYE_W_DIS2#: M.2 Key E Wireless module functionality disable signal #1 and #2, active low outputs.

M2_KEYE_I2C_SDA: I2C Bus data line. Bidirectional signal, electrical level +3.3V_RUN with a 2K2Ω pull-up resistor.

M2_KEYE_I2C_SCL: I2C Bus clock line. Electrical level +3.3V_RUN with a 2K2Ω pull-up resistor.

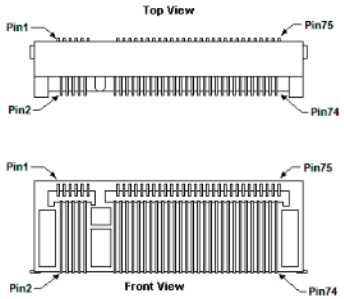
49	PCIE_KEYE_CLK-	50	---
51	GND	52	PCIE_CTL1_RST#
53	PCIE_CTL1_CLK_REQ	54	M2_KEYE_W_DIS2#
55	PCIE_CTL1_WAKE	56	M2_KEYE_W_DIS1#
57	GND	58	M2_KEYE_I2C_SDA
59	---	60	M2_KEYE_I2C_SCL
61	---	62	M2_KEYE_I2C_ALERT#
63	GND	64	---
65	---	66	---
67	---	68	---
69	GND	70	---
71	---	72	+3.3V_RUN
73	---	74	+3.3V_RUN
75	GND		

M2_KEYE_I2C_ALERT#: I2C Bus Alert. Input signal, electrical level +3.3V_RUN with a 2K2Ω pull-up resistor.

3.3.9 M.2 SSD/WWAN Slot: Socket 2 Key B

The mass storage capabilities of the SBC-C43 board are completed by an M.2 SSD Slot, which allow plugging M.2 Socket 2 Key B Solid State Drives.

M.2 SSD/WWAN Slot (Socket 2 Key B type 3042/2260- CN37)			
Pin	**Signal**	**Pin**	**Signal**
1	CONFIG3	2	+3.3V_RUN
3	GND	4	+3.3V_RUN
5	GND	6	M2_KEYB_PWROFF#
7	USB_P1-	8	M2_KEYB_W_DIS1#
9	USB_P1+	10	---
11	GND	20	---
21	CONF0	22	---
23	---	24	---
25	---	26	M2_KEYB_W_DIS2#
27	GND	28	---
29	PCIE0_RX1-	30	UIM_RESET
31	PCIE0_RX1+	32	UIM_CLK
33	GND	34	UIM_DATA
35	PCIE0_TX1-	36	UIM_PWR
37	PCIE0_TX1+	38	---
39	GND	40	---
41	PCIE0_RX0- / SATA0_RX+	42	---
43	PCIE0_RX0+ / SATA0_RX-	44	---
45	GND	46	---
47	PCIE0_TX0- / SATA0_TX-	48	---



The same slot can be used alternatively for the connection of Connectivity modules, using PCI-e x2 interface or USB 2.0 interface (USB interface is always available, while SATA interface is alternative to PCI-e interface).

The connector used for the M.2 SSD slot is CN37, which is a standard 75 pin M.2 Key B connector, type LOTES p/n APCI0087-P001A, H=8.5mm, with the pinout shown in the table on the left.

On the SBC-C43 board there is also a Threaded Spacer which allows the placement of M.2 Socket 2 Key B SSD modules in 2260 size.

It is possible to place also modules in 2242 / 3042 size, by using a M/F Spacer which allow fixing the M.2 SSD on the spacer already available on the PCB, deemed for the fixing of the M.2 connectivity slot (see par. 3.3.8).

Here following the signals related to the SATA interface:

SATA0_TX+ / SATA0_TX-: Serial ATA Channel #0 Transmit differential pair

SATA0_RX+ / SATA0_RX-: Serial ATA Channel #0 Receive differential pair

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

Here following the signals related to the PCI-e interface:

PCIE0_TX0+ / PCIE0_TX0-: PCI Express port #0 lane #0, Transmitting Output Differential pair

PCIE0_RX0+ / PCIE0_RX0-: PCI Express port #0 lane #0, Receiving Input Differential pair

PCIE0_TX1+ / PCIE0_TX1-: PCI Express port #0 lane #1, Transmitting Output Differential pair

PCIE0_RX1+ / PCIE0_RX1-: PCI Express port #0 lane #1, Receiving Input Differential pair

PCIE_KEYB_CLK+ / PCIE_KEYB_CLK-: Dedicated PCI Express Reference Clock

PCIE_CTL0_RST: Reset Signal that is sent from the SoC to all PCI-e devices available on the board. It is a +3.3V_RUN active-low signal with 100kΩ pull-down.

PCIE_CTL0_CLK_REQ0: PCI Express Clock Request Input, active low signal. This signal shall be driven low by any module inserted in the connectivity slot, in order to ensure that the SoC makes available the reference clock. Electrical level +3.3V_RUN with a 47KΩ pull-up resistor.

49	PCIe0_TX0+ / SATA0_TX+	50	PCIE_CTL0_RST
51	GND	52	PCIE_CTL0_CLK_REQ
53	PCIE_KEYB_CLK-	54	PCIE_CTL0_WAKE
55	PCIE_KEYB_CLK+	56	---
57	GND	58	---
59	---	60	---
61	---	62	---
63	---	64	---
65	---	66	SIM_DETECT
67	---	68	---
69	CONF1	70	+3.3V_RUN
71	GND	72	+3.3V_RUN
73	GND	74	+3.3V_RUN
75	CONF2		

PCIE_CTL0_WAKE: Board's Wake Input, 3.3V_RUN active low signal with 47kΩ pull-up resistor. It must be externally driven by the Connectivity module plugged in the slot when it requires waking up the system.

Here following the signals related to the USB interface:

USB_P1+ / USB_P1-: USB Port #1 differential pair; it is managed by Microchip USB4604 Hub controller's Downstream Port #1.

M2_KEYB_PWROFF#: Power Off signal for plugged modules, usually used in battery-powered systems. Fixed 2k2Ω pull-up @ 1.8V_RUN.

M2_KEYB_W_DIS1# / M2_KEYB_W_DIS2#: M.2 module functionality disable signals #1 and #2, active low outputs.

UIM_RESET: Reset signal line, sent from M.2 WWAN card to the UIM module.

UIM_DATA: Bidirectional Data line between M.2 WWAN card and UIM module.

UIM_CLK: Clock line, output from M.2 WWAN card to the UIM module.

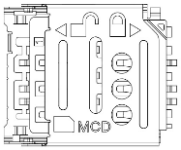
UIM_PWR: Power line for UIM module.

SIM_DETECT: Sim Detect signal coming from module. It can be forced to be low through the insertion of jumper JP1.

CONF0, CONF1, CONF2, CONF3: Configuration inputs, +3.3V_RUN signals with 10kΩ pull-up. These signals are necessary to switch between the S-ATA and the PCI-e signals on the pins 29/31/35/37/41/43/47/49 of connector CN37. The selection is automatic, according to M.2 specifications for Socket2 Add-In Card configuration Table.

3.3.10 microSIM Card Slot

microSIM Card Slot – CN34			
Pin	Signal	Pin	Signal
1	UIM_PWR	5	GND
2	UIM_RST#	6	---
3	UIM_CLK	7	UIM_DATA
4	---	8	---

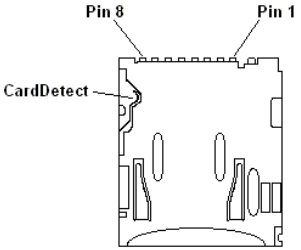


Interfaced to the M.2 slot CN37, there is a microSIM Card Slot, to be used in conjunction with M.2 Socket 2 Key B modems. Here it is possible to insert the microSIM card provided by any telecommunication operator for the connection to their network.

The socket is type MOLEX. p/n 78800-0001or equivalent, with the pinout shown in the table on the left. Signal are described in paragraph 3.3.9.

3.3.11 microSD Slot

µSD Card Slot – U43	
Pin	Signal
1	SDIO_DAT2
2	SDIO_DAT3
3	SDIO_CMD
4	+3.3V_RUN
5	SDIO_CLK
6	GND
7	SDIO_DAT0
8	SDIO_DAT1



The i.MX8 Family of SoCs embeds three Ultra Secured Digital Host controller (uSDHC), able to support SD / SDIO / MMC Cards.

One of them is used for the implementation of the optional onboard eMMC drive, another is used to manage the M.2 Socket 1 Key E Slot (CN36, the other one is used to manage a µSD Card Slot for the use of standard microSD cards, which can be used as Mass Storage and/or Boot Devices.

The connector is a microSD connector, push-push type, H=2mm, p/n TFWF1.

SDIO_CLK: SD Clock Line (output).

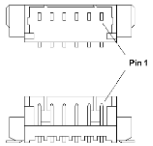
SDIO_CMD: Command/Response bidirectional line.

SDIO_DAT[0÷3]: SD Card data bus. SDIO_DAT0 signal is used for all communication modes. SDIO_DAT[1÷3] signals are required for 4-bit communication mode.

3.3.12 CAN Connectors

On SBC-C43 board there can be three optional CAN Connectors managed using as many TJA1051 CAN trasnceivers.

CAN Bus Connectors are 6-pin single line SMT connector, type MOLEX 53398-0461 or equivalent, with pinout shown in the tables below. Mating connector: MOLEX 51021-0600 receptacle with MOLEX 50079-8000 female crimp terminals.



On these connectors, the pins CANx_L_TERM and CANx_TERM can be used to insert the 120Ohm termination at the end of CAN line. When the termination is needed, then these pins must be connected together.

CAN BUS #0 – CN46	
Pin	**Signal**
1	+12V_ALW
2	CAN0_H
3	GND
4	CAN0_L
5	CAN0_L_TERM
6	CAN0_TERM

CAN BUS #1 – CN47	
Pin	**Signal**
1	+12V_ALW
2	CAN1_H
3	GND
4	CAN1_L
5	CAN1_L_TERM
6	CAN1_TERM

CAN BUS #2 – CN48	
Pin	**Signal**
1	+12V_ALW
2	CAN2_H
3	GND
4	CAN2_L
5	CAN2_L_TERM
6	CAN2_TERM

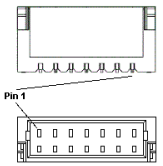
CANx_H: High-Level CAN bus line.

CANx_L: Low-Level CAN bus line.

3.3.13 JTAG Connector

JTAG Connector – CN18	
Pin	**Signal**
1	+3V3_ALW
2	JTAG_TCK
3	JTAG_TMS
4	JTAG_TDI
5	JTAG_TDO
6	JTAG_RST#
7	GND

SBC-C43 board is equipped with a connector reporting the JTAG signals coming from the i.MX8 processor, which can be useful for software debugging and tracing in development phase. This connector is a 7-pin single line SMT connector, type JST SM07B-SRSS-TB or equivalent, with pinout shown on the table to the left. Mating connector: JST SHR-07V-S receptacle or equivalent with JST SSH-003T-P0.2-H female crimp terminals.

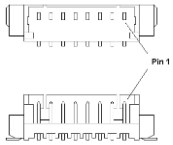


JTAG_RST#: power section reset input, active low signal, electrical level +1V8_RUN with a 10KΩ pull-up resistor

All other JTAG signals are directly connected to i.MX8 pins with same name. Please refer to i.MX8 processor's documentation for a description of the signals and their usage.

3.3.14 Expansion connectors

SBC-C43 board offers multiple interfaces, like RS-232, RS-485, SPI, I2C and so on, which are carried to three expansion connectors.



Expansion Connector #1– CN49

Pin	Signal
1	+3.3V_RUN
2	GND
3	TTL_GPIO_UART2_TX
4	TTL_GPIO_UART2_RX
5	RS232_UART2_TX
6	RS232_UART3_RX
7	RS232_UART3_RTS
8	RS232_UART3_CTS

First expansion connector is CN49, an 8-pin single line SMT connector, type MOLEX 53398-0871 or equivalent, with pinout shown in the table on the left. Mating connector: MOLEX 51021-0800 receptacle with MOLEX 50079-8000 female crimp terminals. This connector carries out processor's UART #1 (4-wires UART) and UART#2 interface (2-wires UART). UART #1 interface can be optionally (factory alternatives) available in RS-232 or TTL interface, while UART #2 interface is always available in TTL interface. Pins available with TTL interface can also be used also as GPIO.

RS232_UART1_TX: Serial Port#3 Transmit data; can be available at RS232 or TTL level (factory alternatives)

RS232_UART1_RX: Serial Port#3 Receive data; can be available at RS232 or TTL level (factory alternatives)

RS232_UART1_RTS: Serial Port#3 Request to Send handshaking signal; can be available at RS232 or TTL level (factory alternatives)

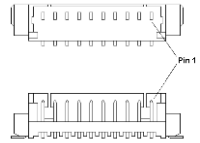
RS232_UART1_CTS: Serial Port#3 Clear to Send handshaking signal; can be available at RS232 or TTL level (factory alternatives)

TTL_GPIO_UART2_TX: GPIO or Serial Port#2 Transmit data (TTL level)

TTL_GPIO_UART2_RX: GPIO or Serial Port#2 Receive data (TTL level)

Expansion Connector #2– CN50

Pin	Signal
1	+3.3V_RUN
2	UART4_TX_485_Y
3	UART4_RX_485_Z
4	RS485_A
5	RS485_B
6	GND
7	M41_I2C0_SDA
8	M41_I2C0_SCL
9	GPIO_0
10	GPIO_1



Second expansion connector is CN50, a 10-pin single line SMT connector, type MOLEX 53398-1071 or equivalent, with pinout shown in the table on the left. Mating connector: MOLEX 51021-1000 receptacle with MOLEX 50079-8000 female crimp terminals.

This connector carries out processor's UART #4 (4-wires UART) interface, M41 core's I2C interface and two GPIOs.

UART #4 interface can be optionally (factory alternatives) available in RS-485 or TTL interface.

Pins available with TTL interface can also be used also as GPIO.

UART4_TX_485_Y / UART4_RX_485_Z: Serial Port#4; can be RS485 differential pairs, RS422 transmit pair or TTL tx/rx pair (factory alternatives)

UART4_RX_485_Z: Serial Port#4 Receive data; can be available at RS485 or TTL level (factory alternatives)

RS485_A / RS485_B: RS485 differential pairs or RS422 transmit pair (factory alternatives)

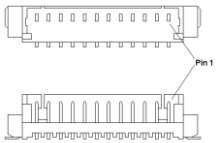
M41_I2C0_SDA: M41 core's I2C Bus data line. Bidirectional signal, electrical level +3.3V_RUN with a 2k2Ω pull-up resistor.

M41_I2C0_SCL: M41 core's I2C Bus clock line. Bidirectional signal, electrical level +3.3V_RUN with a 2k2Ω pull-up

Expansion Connector #3– CN51	
Pin	**Signal**
1	+3.3V_RUN
2	GND
3	SPI3_SCK
4	SPI3_SDO
5	SPI3_SDI
6	SPI3_CS0
7	GPIO_2
8	GPIO_3
9	GPIO_4
10	GPIO_5
11	SCU_UART0_TX
12	SCU_UART0_RX

resistor.

GPIO_[0÷1]: General purpose IO #0 and #1, electrical level +3.3V_RUN



Third expansion connector is CN51, a 12-pin single line SMT connector, type MOLEX 53398-1271 or equivalent, with pinout shown in the table on the left. Mating connector: MOLEX 51021-1200 receptacle with MOLEX 50079-8000 female crimp terminals.

This connector carries out processor's SPI interface #3, four GPIOs and processor's UART #0 interface at TTL level.

SPI3_CS0: SPI chip select, output signal, active high, electrical level +3.3V_RUN.

SPI3_SDI: SPI Master Input Slave Output, input signal, electrical level +3.3V_RUN.

SPI3_SDO: SPI Master Output Slave Input, ouput signal, electrical level +3.3V_RUN.

SPI3_SCK: SPI Serial Clock, electrical level +3.3V_RUN

GPIO_[2÷5]: General purpose IO's, electrical level +3.3V_RUN

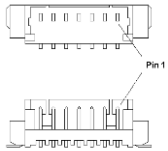
SCU_UART0_TX: Serial Port#0 Transmit data (TTL level)

SCU_UART0_RX: Serial Port#0 Receive data (TTL level)

3.3.15 A/D Header

A/D Header – CN45	
Pin	**Signal**
1	+3.3V_RUN
2	ADC_0
3	ADC_1
4	GND
5	ADC_2
6	ADC_3
7	GND

NXP i.MX8 Processor includes to 12-bit Quad-channel Analog-to-Digital Converter (ADCs), which can be used, on SBC-C43 board, to manage up to 4 analog inputs.



The A/D converter interface is accessible through a 7-pin 1.25mm pitch connector, type MOLEX 53398-0771 or equivalent, with the pinout shown in the table on the left.

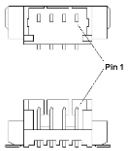
Mating connector: MOLEX 51021-0700 receptacle with MOLEX 50079-8000 female crimp terminals.

ADC_[0÷3]: Analog Inputs, voltage range from -12V to +12V.

3.3.16 Debug UART Connector

Debug UART – CN39	
Pin	**Signal**
1	+3.3V_RUN
2	UART0_RX
3	UART0_TX
4	GND

Onboard, connector CN39 carries out signals related to Debug Serial Port, which is managed by NXP i.MX8 UART3 internal controller, with signals available at TTL level. This interface can be used for the debugging of the processor.



For this purpose, a dedicated 4-pin Connector, Type MOLEX p/n 53398-0471 or equivalent is provided. Mating connector: MOLEX 51021-0400 receptacle with MOLEX 50079-8000 female crimp terminals.

UART0_RX: UART #0 Receive data signal, electrical level +3.3V_RUN

UART0_TX: UART #0 Transmit data signal, electrical level +3.3V_RUN

3.3.17 Power and Reset buttons

SBC-C43 board is equipped with a Reset button (SW1) and a Power button (SW2), type C&K p/n KMR211G LFS.

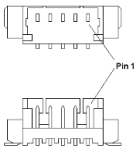
When SW1 Reset button is toggled the board's power section will be reset.
When SW2 Power button is toggled the board will turn on from off and respectively turn off from on.

Please be aware that the push button switches are available only on board in commercial temperature range, since they cannot sustain the full industrial temperature range.

3.3.18 Power and Reset connector

Power and Reset – CN56	
Pin	**Signal**
1	+5V_RUN
2	GND
3	iMX8_ON_OFF
4	GND
5	RST_BTN

Independently by the temperature range of the module purchased, it is always available an additional connector, CN56, to allow use of external power and reset switches, this is a 5-pin Connector, type MOLEX 53398-0571 or equivalent. Mating connector: MOLEX 51021-0500 receptacle with MOLEX 50079-8000 female crimp terminals.



iMX8_ON_OFF: input signal, pulled high internally with debounce function, when toggled the board will turn on from off and respectively turn off from on.
RST_BTN: input signal, pulled high at +1.8V_RUN with a 70kΩ resistor, when toggled the board's power section will be reset.

3.3.19 Boot Mode Selection jumper JP2

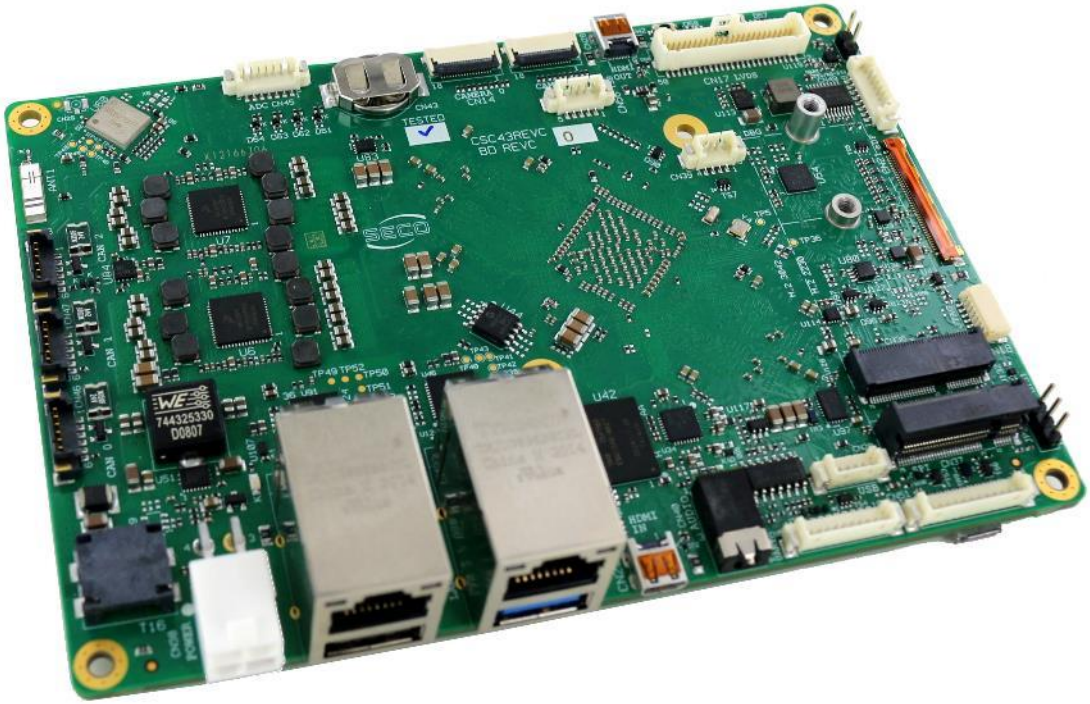
JP2 Jumper	Boot mode
1-2	Serial download
2-3	Internal ROM

The onboard 2-way jumper JP2 can be used to select boot mode for the SBC-C43 module.

When the jumper is inserted in position 1-2, then the processor will search for the USB OTG connection to be established, in order to download a program image to the chip.
When the jumper is inserted in position 2-3, the processor will continue to execute the boot code from the internal boot ROM.

Chapter 4.
APPENDICES

- Thermal Design



4.1 Thermal Design

Highly integrated systems, like the SBC-C43 board, offer the user excellent performance in a much reduced space, therefore allowing the system's minimization. On the other hand, the miniaturizing of IC's and the increase of clock frequencies of the processors lead to the generation of a big amount of heat that must be dissipated to prevent critical operating conditions, system hang-off or failures.

It is extremely important to note that, for this reason, a critical design parameter always to be kept in very high consideration is the thermal design and analysis of the final assembled system. It is necessary to carefully consider the heat generated by the module in the final assembled system and the application.

The customer must always ensure that the heatspreader/heatsink surface temperature remain within the declared operating temperature range at any point of the cooling element.

Please always keep in mind that heavy computational tasks will generate much heat, on all versions of the processor.

Therefore, it is always necessary that the customer studies and develops a specifically tailored cooling solution for the final system by evaluating processor's workload, application environment, system enclosure, air flow and so on.

Warning!

The thermal solutions available with SECO boards are tested in the commercial temperature range (0-60°C), without housing and inside climatic chamber. Therefore, the customer is suggested to study, develop and validate the cooling solution for his system, considering ambient temperature, processor's workload, utilisation scenarios, enclosures, air flow and so on.

In particular, the heatspreader is not intended to be a cooling system by itself, but only as the standard means for transferring heat to cooler, like heatsinks, cold plate, heat pipes and so on.

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