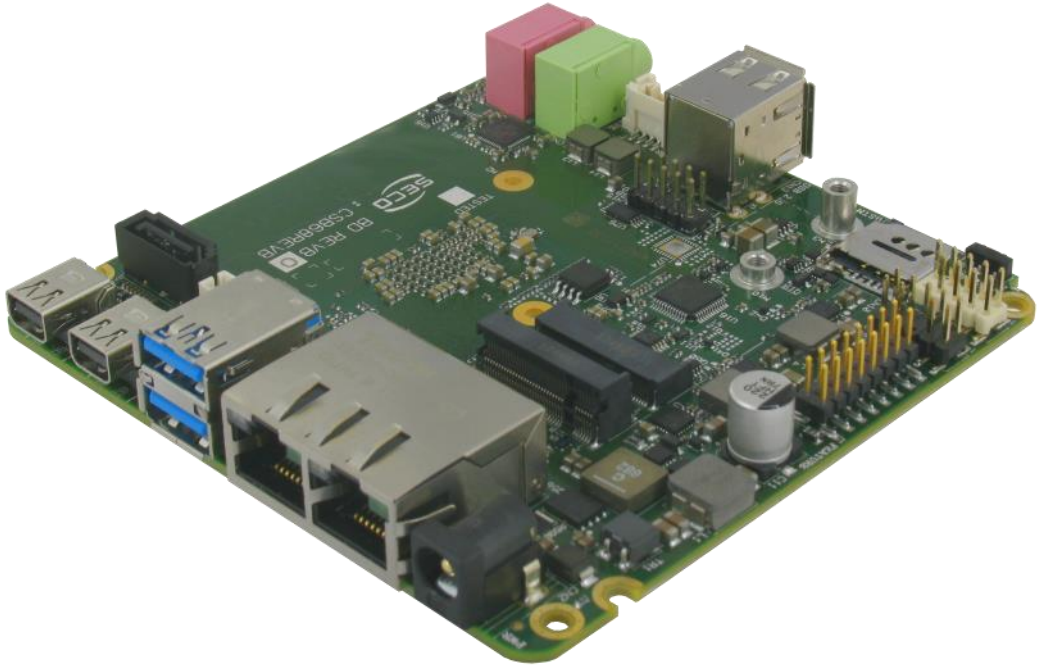
SBC

User Manual



SBC-B68-eNUC

SBC with the Intel® Atom™ X Series, Intel® Celeron® J/N Series and Intel® Pentium® N Series (formerly code name Apollo Lake) SoCs in the embedded NUC™ form factor

SECO

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REVISION HISTORY

Revision	Date	Note	Ref
1.0	27 April 2018	First Official Release.	SB
1.1	26 February 2018	Technical Features updated. Aligned to PCB rev. D Breaker references removed in par. 3.3.4 and 3.3.14 BIOS Section updated eDP-to-LVDS accessory section updated (par. 5.2.3)	SB
1.2	21 May 2019	CN2 P/N corrected CN19 Specification updated and pinout corrected CABKITB68 composition corrected	SB
1.3	21 April 2020	Amplified audio specifications corrected (par. 3.3.5) CN9 pinout corrected (par. 3.3.9) eDP-to-LVDS accessory section updated (par. 5.2.3)	SB

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications withoTut prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

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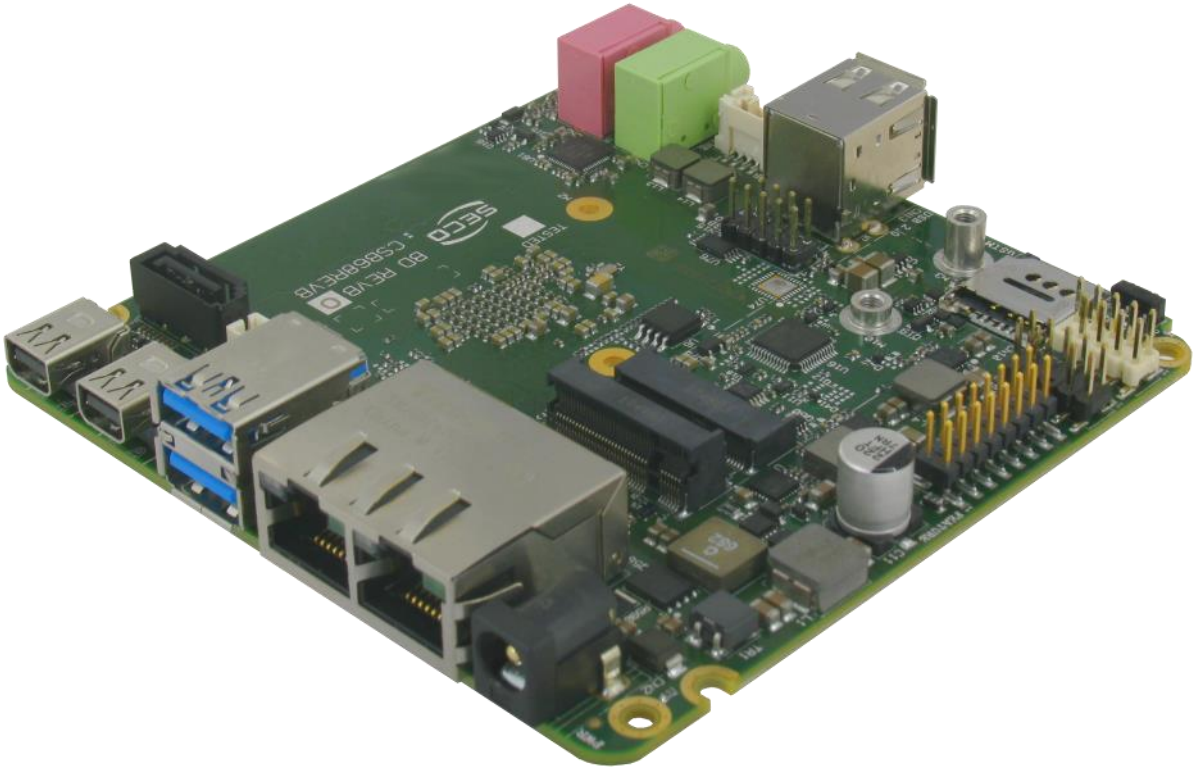
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorized by the supplier.

The authorization is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorization number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above mentioned requirements for the RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionalities and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The SBC-B68-eNUC board uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic discharges

The SBC-B68-eNUC board, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling a SBC-B68-eNUC board, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The SBC-B68-eNUC board is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
DDR3L	DDR, 3rd generation, Low voltage
DP++	Multimode Display Port, a video interface which can support both Display Port displays (directly) and HDMI/DVI displays (by using and external adapter)
eDP	embedded Display Port
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
IoT	Internet of Things
M.2	recent specifications for internal expansion modules, which defines many pinouts and sizes for different purposes. Can include SATA, PCI Express, USB, UART, DP interfaces
Mbps	Megabits per second
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected

OpenCL	Open Computing Language, a software library based on C99 programming language, conceived explicitly to realise parallel computing using Graphics Processing Units (GPU)
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OS	Operating System
PCI-e	Peripheral Component Interface Express
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
PXE	Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS
SATA	Serial Advance Technology Attachment, a differential full duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SIM	Subscriber Identity Module, a card which stores all data of the owner
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TDP	Thermal Design Power, an indication of the amount of heat generated by the processor that must be used for the design of the thermal solution.
TMDS	Transition-Minimized Differential Signaling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
UIM	User Identity Module, an extension of SIM modules.
USB	Universal Serial Bus
V_REF	Voltage reference Pin
xHCI	eXtensible Host Controller Interface, Host controller for USB 3.0 ports, which can also manage USB 2.0 and USB1.1 ports

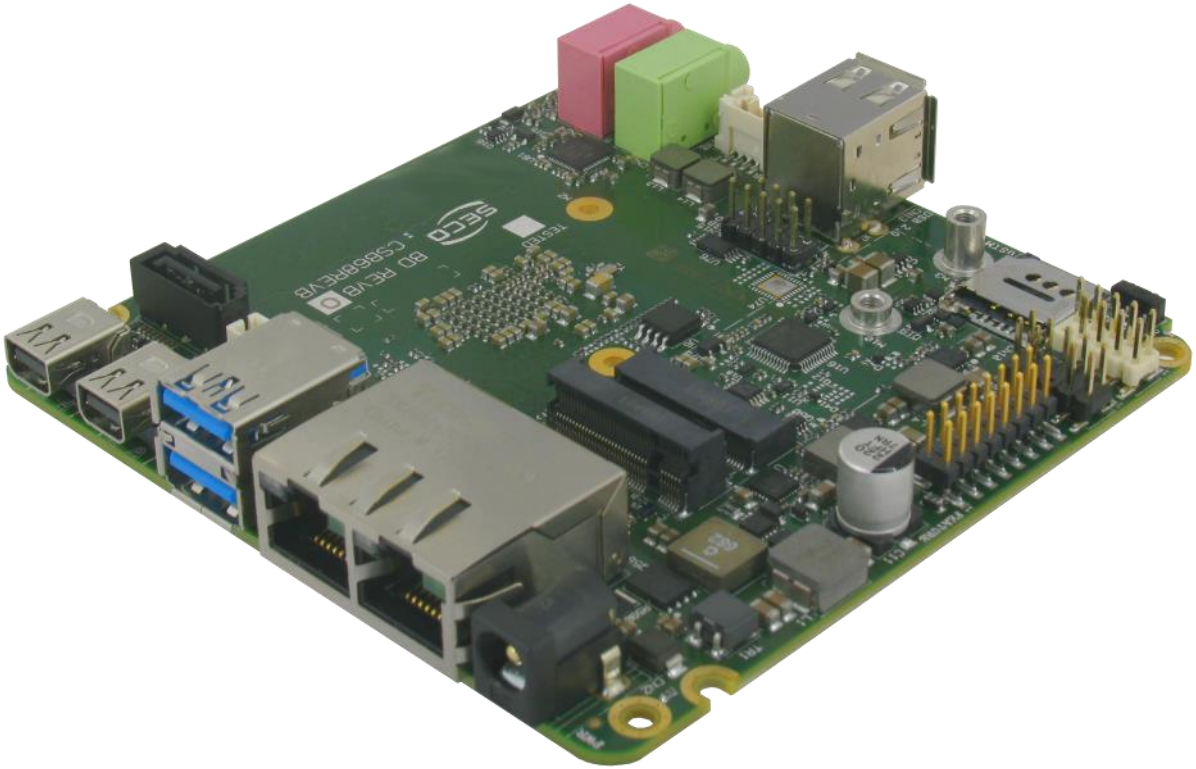
1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
DDC	http://www.vesa.org
embedded NUC™	http://www.sget.org/fileadmin/_migrated/content_uploads/SGET_Specification_embedded_NUC_SFF_V100.pdf
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
Intel® Front Panel I/O connectivity DG	http://www.formfactors.org/developer/specs/A2928604-005.pdf
M.2	http://pcisig.com/specifications
MMC/eMMC	http://www.jedec.org/committees/jc-649
OpenCL	http://www.khronos.org/opencl
OpenGL	http://www.opengl.org
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SD Card Association	https://www.sdcard.org/home
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
UEFI	http://www.uefi.org
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip
Intel® Atom™, Pentium ® and Celeron® Apollo Lake family	http://ark.intel.com/products/codename/80644/Apollo-Lake#@Embedded

Chapter 2.
OVERVIEW

- Introduction
- Technical specifications
- Electrical specifications
- Mechanical specifications
- Block diagram



2.1 Introduction

SBC-B68-eNUC is a Single Board Computer in embedded NUC™ form factor (just 101.6 x 101.6mm) based on the 8th generation Intel® Atom™, Pentium® and Celeron® family of System-on-Chips (SOCs) formerly coded as Apollo Lake, a series of Dual / Quad SOCs with 64-bit instruction set.

These SoCs embed all the features usually obtained by combination of CPU + platform controller hubs, all in one single IC, which allows, therefore, the system minimisation and performance optimisation, which is essential for boards with sizes so reduced as for embedded NUC™ SBCs.

The board is also available in EXTREME configuration, with all the components mounted onboard certified for industrial temperature ranges (this configuration is not available with the Celeron® processors).

The embedded memory controller allows the integration of up to 8GB of LPDDR4 Memory directly soldered onboard, speed up to 2400MT/s.

All SOCs embed an Intel® HD Graphics 500 series controller, which offer high graphical performances, with support for Microsoft® DirectX12, OpenGL 4.3, OpenCL 1.2, OpenGLES 3.0 and HW acceleration for video encoding and decoding of HEVC (H.265), H.264, JPEG/MJPEG. It is also possible the HW video decoding only of VP9, MPEG2, VC-1 and WMV9.

This embedded GPU is able to drive three independent displays, by using the miniDP++ and eDP interfaces. Any combinations of these video interfaces are supported.

Further features, managed directly by the Intel® Atom™, Pentium® and Celeron® family of System-on-Chips (SOCs) SoCs and included in SBC-B68-eNUC board, are two SATA Channels (one used for the common SATA / SSD drives, the other used to implement a M.2 Socket 2 Key B SSD/WWAN slot), microSD interface, eight USB ports (two USB 3.0 and two further USB 2.0 on standard Type-A sockets, one USB 2.0 on M.2 Socket 1 Key E Connectivity slot, one USB 3.0 on M.2 Socket 2 Key B SSD/WWAN slot and two USB 2.0 on internal pin header), HD Audio, two UARTs (which are made available with software-configurable RS-232 / RS-422 / RS-485 interface) and five PCI Express lanes (two PCI express lanes are used for the implementation of two Gigabit Ethernet interfaces, a PCI-e x1 lane is carried out on M.2 Socket 1 Key E Connectivity slot, a PCI-e x2 port is shared on M.2 Socket 2 Key B SSD/WWAN slot)

This board is suitable both for IoT applications, due to its rich connectivity, and for industrial applications, since it can accept supply voltages in the range +18V_{DC} ÷ + 32V_{DC} (recommended voltage range).

The board offers the possibility of expansion by using M.2 modules (both for mass storage and connectivity expansion), which is one of the most recent standards for expansion modules. This guarantees to the SBC-B68-eNUC board a wide possibility of expandability even for the future.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

2.2 Technical specifications

SoC

Intel® Atom™ x7-E3950, Quad Core @1.6GHz (Burst 2.0GHz), 2MB L2 Cache, 12W TDP
Intel® Atom™ x5-E3940, Quad Core @1.6GHz (Burst 1.8GHz), 2MB L2 Cache, 9.5W TDP
Intel® Atom™ x5-E3930, Dual Core @1.3GHz (Burst 1.8GHz), 2MB L2Cache, 6.5W TDP
Intel® Pentium® N4200, Quad Core @1.1GHz (Burst 2.5GHz), 2MB L2 Cache, 6W TDP
Intel® Celeron® N3350, Dual Core @1.1GHz (Burst 2.4GHz), 2MB L2Cache, 6W TDP
Intel® Celeron® J3455, Quad Core @1.5GHz (Burst 2.3GHz), 2MB L2Cache, 10W TDP
Intel® Celeron® J3355, Dual Core @2.0GHz (Burst 2.5 GHz), 2MB L2Cache, 10W TDP

Memory

Quad Channel Soldered Down LPDDR4 memory, up to 8GB

Graphics

Integrated Intel® HD Graphics 500 series controller with up to 18 Execution Units
Three independent display support
HW decoding of HEVC(H.265), H.264, MVC , VP8, VP9, MPEG2, VC-1, WMV9, JPEG/MJPEG formats
HW encoding of HEVC(H.265), H.264, MVC, VP8, VP9 and JPEG/MPEG formats

Video Interfaces

Two DP++ 1.2 interfaces on miniDP connectors (supports HDMI displays through external adapter)
embedded Display Port (eDP) internal connector
LVDS through optional external adapter

Video Resolution

HDMI, eDP:	Up to 3840x2160 (4K)
DP++:	Up to 4096x2160
LVDS:	Up to 1920 x 1200

Mass Storage

Optional eMMC drive onboard
SATA 7p M connector
M.2 SATA SSD slot (Socket 2 Key B Type 3042/2260 *)
microSD Card slot

Networking

2x Gbit LAN / Intel Gigabit Ethernet i21x family controller
M.2 WWAN Slot for Modems (Socket 2 Key B Type 3042/2260 *)
M.2 WLAN Connectivity Slot for WiFi/BT (Socket 1 Key E type 2230)

** SATA SSD + USB 3.0 and WWAN functionalities share the same slot and are therefore mutually exclusive*

USB

2 x USB 3.0 Host ports on Type-A sockets
2 x USB 2.0 Host ports on Type-A sockets
2 x USB 2.0 Host port on internal pin header
1 x USB 3.0 Host port on SSD/WWAN M.2 slot (*)
1 x USB 2.0 Host port on WLAN M.2 Slot

PCI-Express

1 x PCI-e x2 port on M.2 SSD/WWAN Slot
1 x PCI-e x1 port on M.2 WLAN Slot

Audio

HD Audio Codec Cirrus Logic CS4207
Mic In and Line out Audio jacks
Amplified Speaker Output on internal pin header

Serial Ports

2 x RS-232 / RS-422 / RS-485 Serial ports on internal pin Header (software configurable)

Other Interfaces

2 x I2C + 8 x GPI/Os on Feature connector
Button/LED Front Panel Header
CIR (Consumer InfraRed) Sensor
microSIM slot for M.2 WWAN Modem

Power supply:	+18V_{DC} ÷ + 32V_{DC} recommended +15V_{DC} ÷ +36V_{DC} absolute RTC Battery
Operating temperature:	0°C ÷ +60°C** (Commercial temperature) -40°C ÷ +85°C (Industrial version)

Dimensions: 101.6 x 101.6 mm (4" x 4").

Supported Operating Systems:

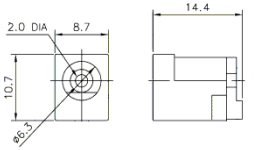
Microsoft® Windows 10 Enterprise (64 bit)
Microsoft® Windows 10 IoT Core
Wind River Linux (64 bit)
Yocto (64 bit)

! *** *Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated.*
Please also check paragraph 5.1

2.3 Electrical specifications

The SBC-B68-eNUC board can be supplied with any voltage in the range +18V_{DC} ÷ +32V_{DC} range (recommended voltage range)

This voltage can be supplied through a standard 6.3mm (internal pin, diameter 2.0 mm) Power Jack (CN1). Internal pin is V_{IN} power line.



Power IN PCB terminal block - CN2	
Pin	**Signal**
1	V_{IN}
2	GND

As an alternative, the board can be equipped with a 2-position Terminal Block with front spring-cage connection type PHOENIX CONTACT p/n 1990973 or equivalent, which can be used for the connection of an external PSU.

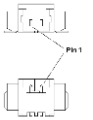
2.3.1 RTC Battery

For the occurrences when the module is not powered with an external power supply, on board there is a cabled coin Lithium Battery to supply, with a 3V voltage, the Real Time Clock embedded inside the Intel® SoC.

Battery used is a cabled CR2032-LD Lithium coin-cell battery, with a nominal capacity of 220mAh.

Battery connector - CN3	
Pin	**Signal**
1	V_{RTC}
2	GND

The battery is not rechargeable, and can be connected to the board using dedicated connector CN5 which is a 2-pin p1.27 mm type MOLEX p/n 53261-0271 or equivalent, with pinout shown in the table on the left.



Mating connector: MOLEX 51021-0200 receptacle with MOLEX 50079-8000 female crimp terminals.

In case of exhaustion, the battery should only be replaced with devices of the same type. Always check the orientation before inserting and make sure that they are aligned correctly and are not damaged or leaking.

Never allow the batteries to become short-circuited during handling.

! CAUTION: handling batteries incorrectly or replacing with not-approved devices may present a risk of fire or explosion.

Batteries supplied with SBC-B68-eNUC are compliant to requirements of European Directive 2006/66/EC regarding batteries and accumulators. When putting out of order SBC-B68-eNUC, remove the batteries from the board in order to collect and dispose them according to the requirement of the same European Directive above mentioned. Even when replacing the batteries, the disposal has to be made according to these requirements.

2.3.2 Power consumption

Using the following setup, and using all possible SoCs offered for SBC-B68-eNUC board, the current consumption (RMS) has been measured on the V_{IN} Voltage line when the board is supplied with a $+19V_{DC}$ voltage through DC power jack CN1. The power consumption has been measured using a Keysight DC Power Analyzer

- O.S. Windows 10 Enterprise 2016 LTSB
- 8GB Soldered Down LPDDR4 memory
- 32GB eMMC onboard
- USB mouse and keyboard connected
- LG 27UD88 4K Ultra-HD monitor connected to module's miniDP through adapter
- Intel Dual Band Wireless-AC 3168 WiFi + BT card connected to M.2 Key-E slot
- Kingston SUV400S37 120GB SSD connected to module
- Bios Release 1.04 RC01

Status	SoC / Configuration				
	x7-E3950	x5-E3940	x3-E3930	N4200	N3350
Idle, power saving configuration	193mA Avg. 28mA Peak	TBM	TBM	TBM	TBM
OS Boot, power saving configuration	320mA Avg. 933mA Peak	TBM	TBM	TBM	TBM
Intel TAT tool running, maximum performance	991mA Avg. 1347mA Peak	TBM	TBM	TBM	TBM
Suspend state (S3)	48.7mA	TBM	TBM	TBM	TBM
Soft-Off State (S4, no deepsleep)	43.4mA	TBM	TBM	TBM	TBM
Soft-Off State (S4, with deepsleep)	22.2mA	TBM	TBM	TBM	TBM

Please consider that the power consumption depends strongly on the utilization scenario.

Please also consider that the SBC-B68-eNUC board can accept a wide voltage range; the efficiency of the DC/DC converters, necessary to generate all the voltages used by the module itself and by the peripherals connected, varies with the rise of the input voltage.

For all these reasons, it is recommended to use PSU with a minimum voltage of 40W for basic functionalities

2.3.3 Power rails naming convention

In all the tables contained in this manual, Power rails are named with the following meaning:

_S: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_S, +5V_S.

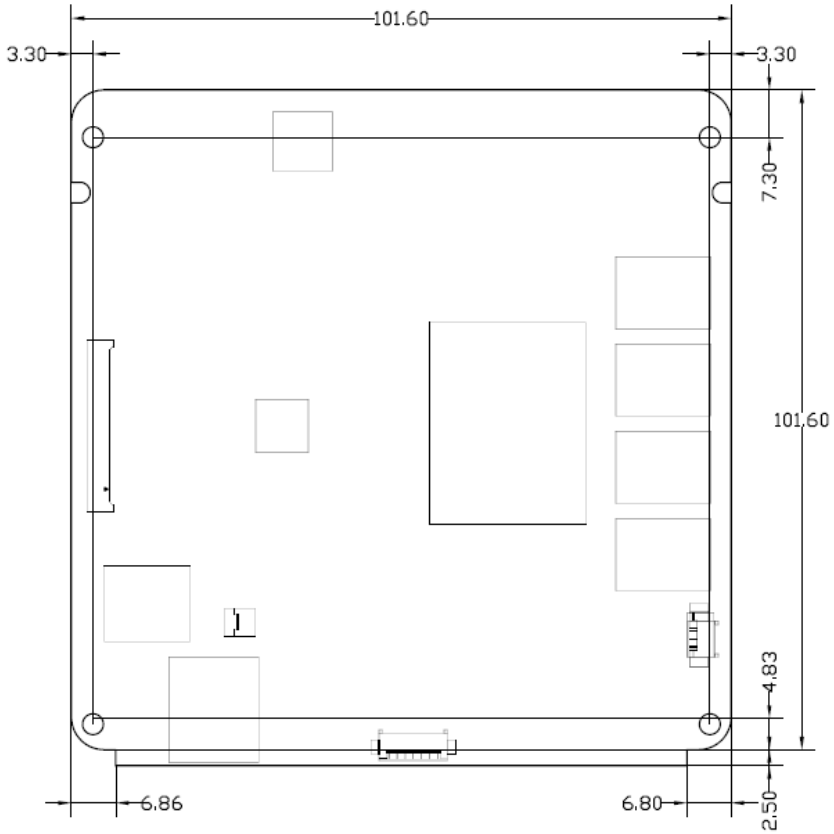
_A: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_A, +3.3V_A.

Other suffixes are used for application specific power rails, which are derived from same voltage value of voltage switched rails, if it is not differently stated (for example, $+5V_{HDMI}$ is derived from +5V_S, and so on).

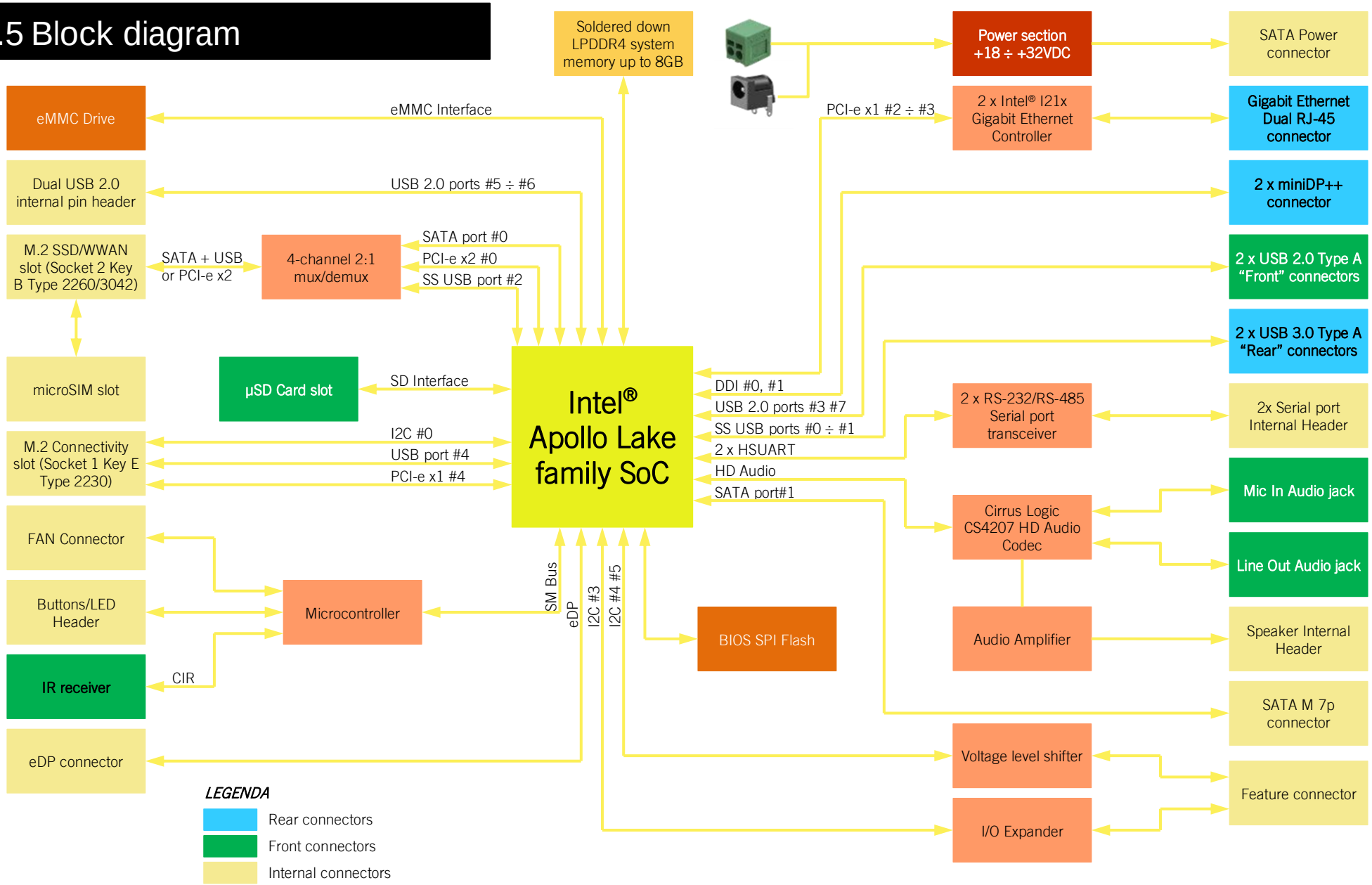
2.4 Mechanical specifications

According to embedded NUC™ form factor, board dimensions are 101.6 x 101.6 mm (4” x 4”).

The printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

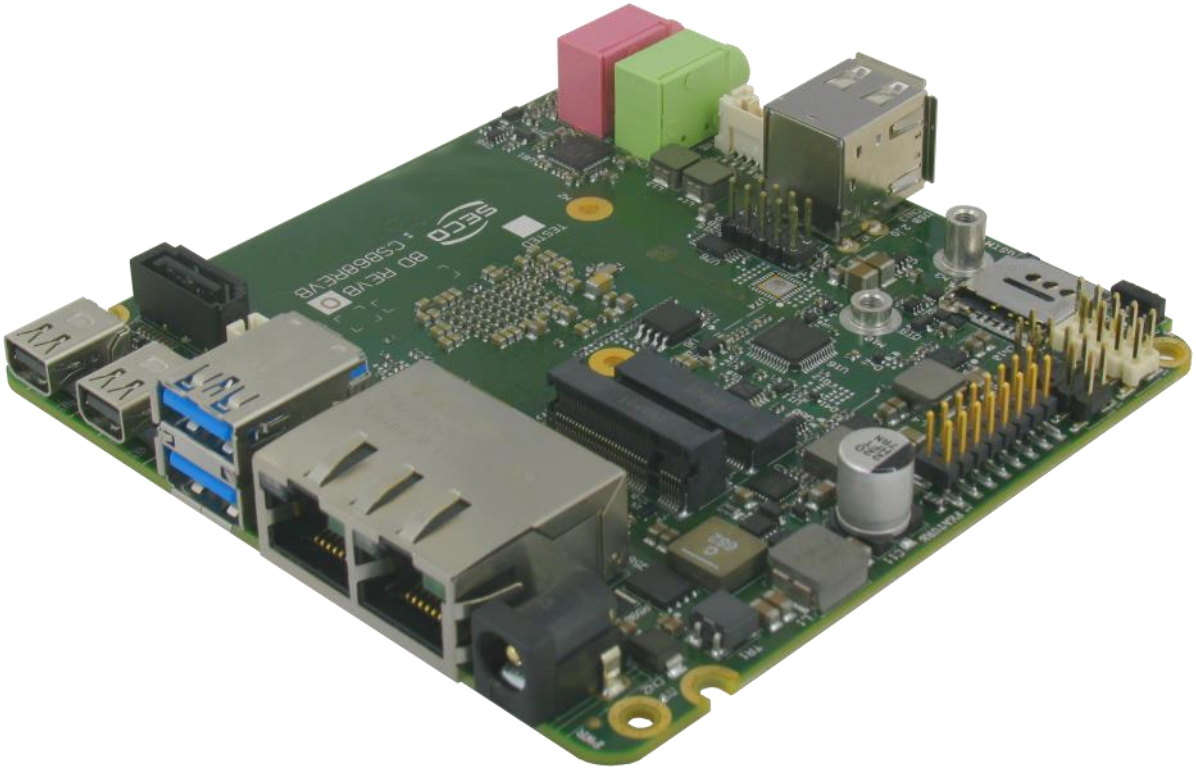


2.5 Block diagram



Chapter 3.
CONNECTORS

- Introduction
- Connectors overview
- Connectors description

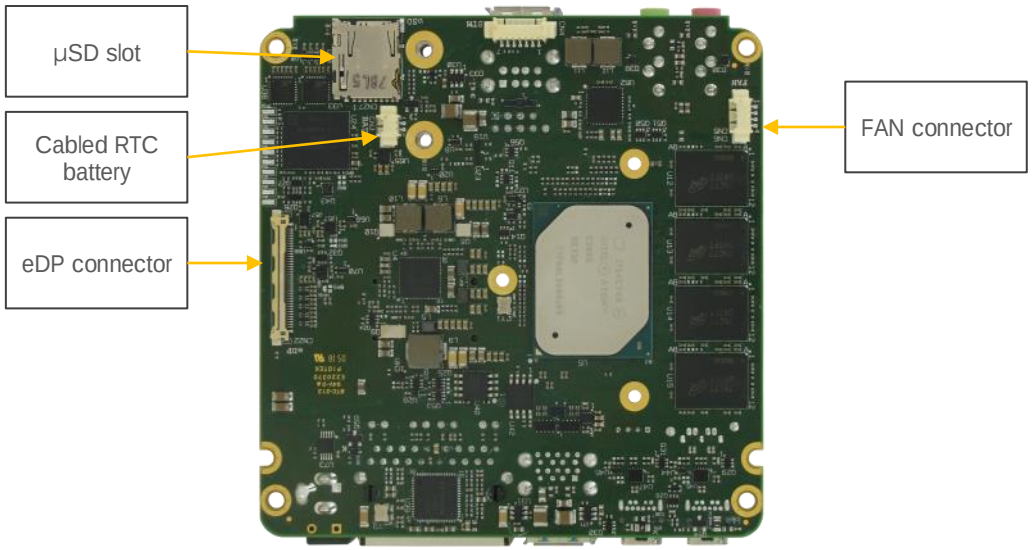


3.1 Introduction

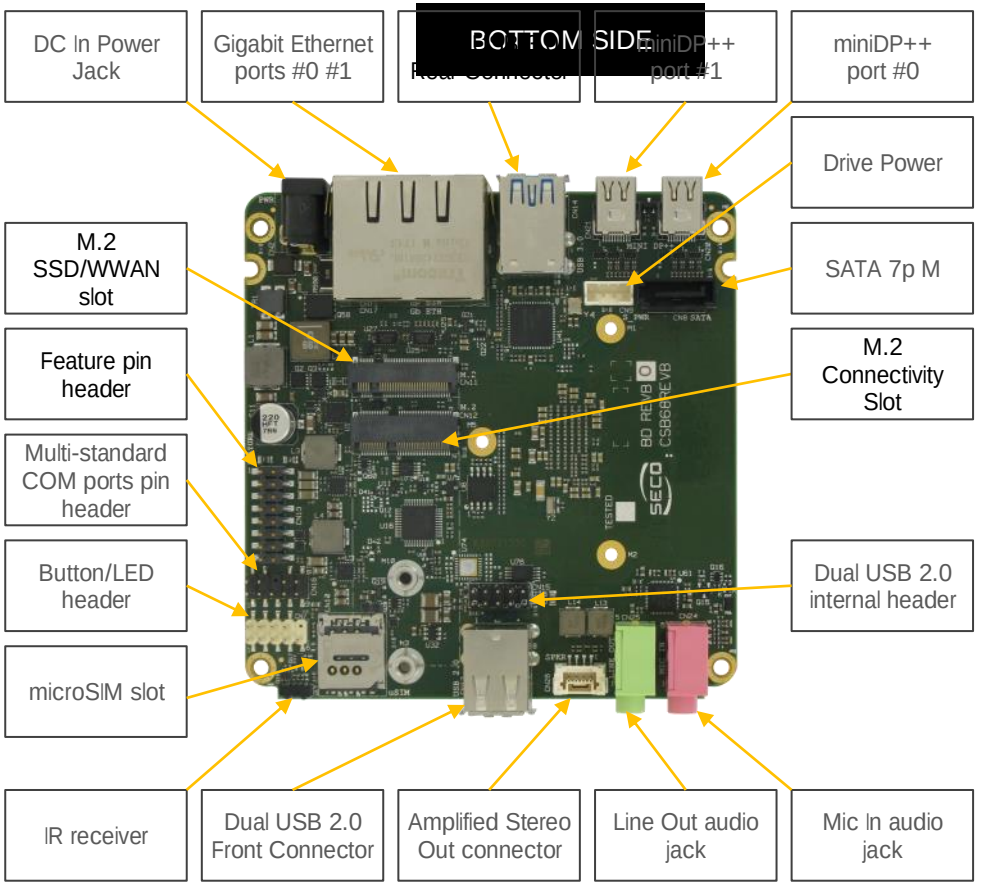
On SBC-B68-eNUC board, there are several connectors located on the upper plane. Standard connectors are placed on the same side of PCB, so that it is possible to place them on a panel of an eventual enclosure.

> **!** Please be aware that, depending on the configuration purchased, the appearance of the board could be slightly different from the following pictures.

TOP SIDE



BOTTOM SIDE



3.2 Connectors overview

Name	Description	Name	Description
CN1	DC IN Power Jack	CN14	Dual USB 3.0 Rear Connector
CN2	DC IN PCB terminal block	CN15	Dual USB 2.0 Internal header
CN3	Cabled RTC Battery	CN16	Multi-standard COM ports internal header
CN4	MFG Connector	CN17	Dual Gigabit Ethernet connector
CN5	Optional FAN Header 3p	CN19	Feature connector
CN6	FAN Header 4p	CN20	miniDP++ #0 connector
CN7	Button/LED Internal Header	CN21	miniDP++ #1 connector
CN8	SATA Port #1 M 7p connector	CN22	eDP internal connector
CN9	HDD Power connector	CN24	Mic Audio Jack
CN10	microSIM Slot	CN25	LineOut Audio Jack
CN11	M.2 SSD/WWAN Slot (Socket 2 Key B Type 2260/3042)	CN26	Amplified Stereo Out connector
CN12	M.2 Connectivity Slot (Socket 1 Key E Type 2230)	CN27	µSD Card Slot
CN13	Dual USB 2.0 Front Connector	U17	IR Receiver

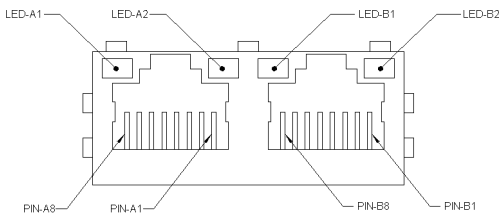
3.3 Connectors description

3.3.1 Ethernet connectors

Dual Gigabit Ethernet Ports #0 / #1 - CN17			
Pin	**Signal**	**Pin**	**Signal**
A1	GBE0_MDI0+	A5	GBE0_MDI2-
A2	GBE0_MDI0-	A6	GBE0_MDI1-
A3	GBE0_MDI1+	A7	GBE0_MDI3+
A4	GBE0_MDI2+	A8	GBE0_MDI3-
B1	GBE1_MDI0+	B5	GBE1_MDI2-
B2	GBE1_MDI0-	B6	GBE1_MDI1-
B3	GBE1_MDI1+	B7	GBE1_MDI3+
B4	GBE1_MDI2+	B8	GBE1_MDI3-

On board, there are two Gigabit Ethernet connections, for the use of two different LANs. Both connections use a dedicated Intel I21x family controller.

Both connections are available on a double port RJ-45 socket type TRXCOM p/n TRJG27420AINL or equivalent, with 2kV decoupling capacitors.



On the connectors there are also two LEDs for each port. Left LED is bicolor (Green /Yellow) and shows 10/100 or 1000 connection: green means 100Mbps connection, yellow means 1000Mpbs connection, when the LED is Off then 10Mpbs or no connection is available. The right LED is Green and shows ACTIVITY presence.

These two interfaces are compatible both with Gigabit Ethernet (1000Mbps) and with Fast Ethernet (10/100Mbps) Networks. They will configure automatically to work with the existing network.

Please be aware that they will work in Gigabit mode only in case that they are connected to Gigabit Ethernet switches/hubs/routers. For the connection, cables category Cat5e or better are required. Cables category Cat6 are recommended for noise reduction and EMC compatibility issues, especially when the length of the cable is significant.

It is also possible to use both Gigabit Ethernet interface simultaneously to perform the link aggregation, useful to increase the throughput of the netwrok connection and to provide also redundancy.

GBEx_MDI0+/GBEx_MDI0-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #0. It is the first differential pair in Gigabit Ethernet mode, and the Transmit differential pair in 10/100 Mbps modes.

GBEx_MDI1+/GBEx_MDI1-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #1. It is the second differential pair in Gigabit Ethernet mode, and the Receive differential pair in 10/100 Mbps modes.

GBEx_MDI2+/GBEx_MDI2-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #2. It is the third differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

GBEx_MDI3+/GBEx_MDI3-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #3. It is the fourth differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

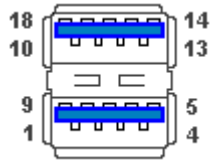
3.3.2 USB ports

The Intel® Apollo Lake family of SoCs used on SBC-B68-eNUC board can manage up to six USB SuperSpeed (i.e., USB 3.0 compliant) ports and eight High Speed (i.e. USB 2.0 compliant) ports. There are only two dedicated High Speed port, the other four ports are shared with the SuperSpeed ports, i.e. they can be used either by USB 2.0 or USB 3.0.

USB 3.0 ports Type-A double receptacle - CN14

Pin	Signal	Pin	Signal
1	$+5V_{USB1}$	10	$+5V_{USB0}$
2	USB_P1-	11	USB_P0-
3	USB_P1+	12	USB_P0+
4	GND	13	GND
5	USB_SSRX1-	14	USB_SSRX0-
6	USB_SSRX1+	15	USB_SSRX0+
7	GND	16	GND
8	USB_SSTX1-	17	USB_SSTX0-
9	USB_SSTX1+	18	USB_SSTX0+

The USB 3.0 ports #0 and #1 are available on a double type-A USB 3.0 receptacle, type Würth Elektronik p/n 692141030100 or equivalent.



Since this connector is a standard type receptacle, it can be connected to all types of USB 1.1 / USB 2.0 / USB 3.0 devices using Standard-A USB 3.0 or USB 2.0 plugs.

For USB 3.0 connections it is mandatory the use of SuperSpeed certified cables, whose SuperSpeed differential pairs are individually shielded inside the global cable's external shielding.

USB 2.0 type A receptacle - CN13

Pin	Signal	Pin	Signal
1	$+5V_{USB7}$	5	$+5V_{USB3}$
2	USB_P7-	6	USB_P3-
3	USB_P7+	7	USB_P3+
4	GND	8	GND

USB 2.0 ports #6 and USB port #3, instead, are carried out on a standard double Type-A receptacle.

Since this connector is a standard type receptacle, it can be connected to all types of USB 1.1 / USB 2.0 devices using Standard-A USB 2.0 cables.

USB 2.0 ports internal pin header - CN15			
Pin	Signal	Pin	Signal
1	$+5V_{USB6}$	2	$+5V_{USB5}$
3	USB_P6-	4	USB_P5-
5	USB_P6+	6	USB_P5+
7	GND	8	GND
		10	---

There are also two additional USB 2.0 ports, which are hosted on a 9-pin p2.54mm pin header, h= 6mm, type NELTRON p/n 2213S-10G-E9 or equivalent, with the pinout shown in the tables on the left (it is a common pinout for USB headers in PC motherboards).

All USB ports' voltages ($+5V_{USBx}$) are derived from +5V_A standby voltages. This means that the ports can be powered also when the OS is in Suspend-to-RAM (S3) state in order to support (if enabled) e the "Wake-Up on USB" functionality.

For the connection of standard devices to this pin headers, it is needed an adapter cable. SECO can optionally provide for such an adapter cable, as a part of the accessory kit p/n CABKITB68 (please check chapter 5.2.1 for further details).

Signal description:

USB_P0+/USB_P0-: USB 2.0 Port #0 differential pair.

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair.

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair.

USB_P1+/USB_P1-: USB 2.0 Port #1 differential pair.

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair.

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair.

USB_P3+/USB_P3-: USB 2.0 Port #3 differential pair.

USB_P5+/USB_P5-: USB 2.0 Port #5 differential pair.

USB_P6+/USB_P6-: USB 2.0 Port #6 differential pair.

USB_P7+/USB_P7-: USB 2.0 Port #7 differential pair.

Common mode chokes are placed on all USB differential pairs for EMI compliance.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

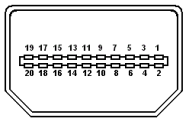
3.3.3 miniDP++ Connectors

miniDP++ Port #0 Connector - CN20			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	DP0_HPD
3	DP0_LANE0+	4	CAD
5	DP0_LANE0-	6	---
7	GND	8	GND
9	DP0_LANE1+	10	DP0_LANE3+
11	DP0_LANE1-	12	DP0_LANE3-
13	GND	14	GND
15	DP0_LANE2+	16	HDMI0_CTRL_CLK/DP0_AUX+
17	DP0_LANE2-	18	HDMI0_CTRL_DAT/DP0_AUX-
19	GND	20	+3.3V_S

miniDP++ Port #1 Connector - CN21			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	DP1_HPD
3	DP1_LANE0+	4	CAD
5	DP1_LANE0-	6	---
7	GND	8	GND
9	DP1_LANE1+	10	DP1_LANE3+
11	DP1_LANE1-	12	DP1_LANE3-
13	GND	14	GND
15	DP1_LANE2+	16	HDMI1_CTRL_CLK/DP1_AUX+
17	DP1_LANE2-	18	HDMI1_CTRL_DAT/DP1_AUX-
19	GND	20	+3.3V_S

The Intel® Apollo Lake family of SoCs offer two Digital Display Interfaces, configurable to work in HDMI/DVI/DP++ modes.

On the SBC-B68-eNUC board, both the Digital Display Interfaces are used to implement multimode Display Port (DP++)interfaces, i.e. they can be used to support DP displays directly and, through an external adapter, also HDMI or DVI displays.



These two interfaces are available on as many miniDP connectors, type Pulse Electronics p/n E9320-001-01 or equivalent, with the pinout shown in the table on the left.

The configuration of this interface in DP or HDMI/DVI mode is automatic, and it is driven by the CAD signal available on pin 4.

When a DP cable is connected, then the CAD signal is not connected; this interface will recognize it, and on pins 16/18 there will be the Display Port Auxiliary channel signals. Instead, when a DP-to-HDMI adapter is mounted, it will drive opportunely the CAD signal, which will make available HDMI_CTRL_CLK and HDMI_CTRL_DAT signals on the same pins.

Further signals involved in DP management are the following:

DPx_LANE0+/DPx_LANE0-: Display Port #x differential pair #0.

DPx_LANE1+/DPx_LANE1-: Display Port #x differential pair #1.

DPx_LANE2+/DPx_LANE2-: Display Port #x differential pair #2.

DPx_LANE3+/DPx_LANE3-: Display Port #x differential pair #3.

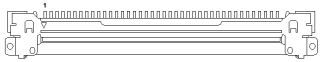
DPx_HPD: Port #x Hot Plug Detect Input signal.

3.3.4 eDP Connector

eDP connector - CN22			
Pin	**Signal**	**Pin**	**Signal**
1	PTN_PWR	21	SW_VDD
2	SW_BACK	22	SW_VDD
3	SW_BACK	23	SW_VDD
4	SW_BACK	24	GND
5	SW_BACK	25	eDP_AUX-
6	PTN_SMB_CLK	26	eDP_AUX+
7	PTN_SMB_DAT	27	GND
8	eDP_BLT_CTRL	28	eDP_TX0+
9	eDP_BACKLIGHT_EN	29	eDP_TX0-
10	GND	30	GND
11	GND	31	eDP_TX1+
12	GND	32	eDP_TX1-
13	GND	33	GND
14	eDP_HPD	34	eDP_TX2+
15	GND	35	eDP_TX2-
16	GND	36	GND
17	GND	37	eDP_TX3+
18	GND	38	eDP_TX3-
19	---	39	GND
20	SW_VDD	40	---

The Intel® Apollo Lake family of SoCs offer a dedicated embedded Display Port interface.

For the connection of this kind of displays, on-board there is a VESA® certified connectors for embedded Display Port interface, type STARCONN p/n 300E40-0110RA-G3 or equivalent (microcoaxial cable connector, 0.5mm pitch, 40 positions).



On this connector, SW_BACK and SW_VDD are the voltage rails that can be used to supply the LCD and related Backlight Unit.

The LCD software-driven voltage, i.e. signal SW_VDD, can be regulated to be connected to +3.3V_A or +5V_A.

Similarly, the backlight software-driven voltage, i.e. signal SW_BACK, can also be regulated to be connected to +5V_A or +12V_A

These are factory configurations, please take care of specifying which is the configuration needed for both SW_VDD and SW_BACK voltage rails.

Here following the signals involved in eDP management:

eDP_TX0+/eDP_TX0-: embedded DP differential data pair #0.

eDP_TX1+/eDP_TX1-: embedded DP differential data pair #1.

eDP_TX2+/eDP_TX2-: embedded DP differential data pair #2.

eDP_TX3+/eDP_TX3-: embedded DP differential data pair #3.

eDP_AUX+/eDP_AUX-: embedded DP auxiliary channel differential data pair.

eDP_HPD: embedded DP Hot Plug Detect. Active high signal with 100kΩ pull-down resistor

eDP_BACKLIGHT_EN: +3.3V_S electrical level Output, 100kΩ pull-down resistor, Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected displays.

eDP_BLT_CTRL: this signal can be used to adjust the backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations (+3.3V_S electrical level, 100kΩ pull-down resistor).

PTN_PWR: 3.3V_S derived voltage for external eDP-to-LVDS bridge adapter (please check par. 5.2.3)

PTN_SMB_CLK: SM Bus control clock line for external eDP-to-LVDS bridge adapter. Output signal, electrical level PTN_PWR with a 2k2Ω pull-up resistor.

PTN_SMB_DAT: SM Bus control data line for external eDP-to-LVDS bridge adapter. Bidirectional signal, electrical level PTN_PWR with a 2k2Ω pull-up resistor.

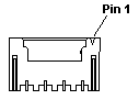
3.3.5 Audio interfaces

In the SBC-B68-eNUC board, audio functionalities are provided by a Cirrus Logic CS4207 High Definition Audio Codec.

Two standard stereo audio jacks are available on-board: the light green (lime) audio jack is the Headphone out (not amplified), while Pink Audio jack is the Mic In.

Amplified Stereo Connector-CN26	
Pin	**Signal**
1	Speaker Right Channel +
2	Speaker Right Channel -
3	Speaker Left Channel -
4	Speaker Left Channel +

Additionally, it is also possible to connect external stereo speakers by using the dedicated connector CN26, which is a connector type JST p/n BM04B-ZESS-TB.



Mating connector: JST ZER-04V-S with SZE-002T-P0.3female crimp terminals.

Speaker audio output is internally amplified, and is able to support:

- 2x 8W outputs on 8Ω speakers;
- 2x 13W outputs on 4Ω speakers.

! Please take care of selecting speakers able to sustain the max power supplied by the audio amplifier

3.3.6 Buttons / LED header

Buttons / LED Header - CN7			
Pin	Signal	Pin	Signal
1	HD_LED_P	2	FP PWR_P/SLP_N
3	HD_LED_N	4	FP PWR_N/SLP_P
5	RST_SW_N	6	PWR_SW_P
7	RST_SW_P	8	PWR_SW_N
9	---		

To allow the integration of a SBC-B68-eNUC based system inside a box PC-like, there is a connector on the board that allows to remote signals for the Power Button (to be used to put the system in a Soft Off State, or awake from it), for the Reset Button, and the signal for optional LED signaling activity on SATA Channel and Power On states.

The pinout of this connector complies with Intel® Front Panel I/O connectivity Design Guide, Switch/LED Front Panel section, chapter 2.2. It is shown in the table on the left.

Connector CN7 is an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E10 or equivalent.

It is possible to buy SECO's dedicated front panel module, which offers standard connections: two standard audio jacks, two pushbuttons (for reset and power on) and two LEDs, for SATA activity and Power status signaling.

This adapter module is also contained inside the dedicated cable kit (CABKITB68) for SBC-B68-eNUC board. Please also check chapter 5.2.1for further details.

Signals Description

HD_LED_P: Hard Disk Activity LED signal's pull-up to +5V_S voltage (510Ω pull-up).

HD_LED_N: Hard Disk Activity LED output signal

RST_SW_N: Reset Button GND

RST_SW_P: Reset button input signal. This signal has to be connected to an external momentary pushbutton (contacts normally open). When the pushbutton is pressed, the pulse of Reset signal will cause the reset of the board.

PWR_SW_P: Power button input signal. This signal has to be connected to an external momentary pushbutton (contacts normally open). Upon the pressure of this pushbutton, the pulse of this signal will let the switched voltage rails turn on or off.

PWR_SW_N: Power button GND

FP PWR_P/SLP_N: Power/Sleep messaging LED terminal 1 with 510Ω pull-up resistor to +5V_A voltage. Connect it to an extremity of a dual-color power LED for power ON/OF, sleep and message waiting signaling. Please refer to Intel® Front Panel I/O connectivity Design Guide, chapter 2.2.4, for LED functionalities and signal meaning.

FP PWR_N/SLP_P: Power/Sleep messaging LED terminal 2 with 510Ω pull-up resistor to +5V_A voltage. Connect it to the other extremity of the dual-color power LED above mentioned.

3.3.7 Multi-standard serial ports

Dual RS-232/RS-422/RS-485 pin header- CN16			
Pin	**Signal RS-232 mode**	**Signal RS-422 mode**	**Signal RS-485 mode**
1	COM1_RxD	COM1_Rx+	
2	COM2_RxD	COM2_Rx+	
3	COM1_TxD	COM1_Tx-	COM1_Data-
4	COM2_TxD	COM2_Tx-	COM2_Data-
5	GND	GND	GND
7	COM1_RTS#	COM1_Tx+	COM1_Data+
8	COM2_RTS#	COM2_Tx+	COM2_Data+
9	COM1_CTS#	COM1_Rx-	
10	COM2_CTS#	COM2_Rx-	

The Intel® Apollo Lake family of SoCs embed three high speed UART controllers, which support COM ports with flow control (RTS# and CTS# signals).

Two of these ports (HSUART #0 and #2) are carried, on SBC-B68-eNUC board to as many multistandard RS-23/RS-422/RS-485 transceivers, allowing the implementation of two multistandard serial ports (from now on respectively named COM1 and COM2).

These ports are available on dedicated connector CN16, which is an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h = 6mm, type NELTRON p/n 2213S-10G-E06 or equivalent.

Signals Description

COM1_RxD/COM2_RxD: COM port #1 / #2 RS-232 Receive data

COM1_TxD/COM2_TxD: COM port #1 / #2x RS-232 Transmit data

COM1_RTS#/COM2_RTS#: COM port #1 / #2 RS-232 Request to Send handshaking signal.

COM1_CTS#/COM2_CTS#: COM port #1 / #2x RS-232 Clear To Send handshaking signal

COM1_RX+/COM1_RX-: COM port #1 RS-422 receive differential pair

COM1_TX+/COM1_TX-: COM port #1 RS-422 Transmit differential pair

COM2_RX+/COM2_RX-: COM port #2 Full Duplex RS-485 (RS-422) Receive differential pair

COM2_TX+/COM2_TX-: COM port #2 Full Duplex RS-485 (RS-422) Transmit differential pair

COM1_Data+/COM1_Data-: COM Port #1 Half Duplex RS-485 Differential Pair

COM2_Data+/COM2_Data-: COM Port #2 Half Duplex RS-485 Differential Pair

The selection of the kind of interface (RS-232, RS-422 or RS-485) can be made via BIOS (please check par.4.3.12).

Please be aware that for proper RS-485 working, the RTS# signals coming out from the Apollo Lake family of SoCs must be used as an handshaking signal, i.e. it is used to control the data flow direction. When RTS# signal is driven low, then the RS-485 port is in receiving mode, when RTS# signal is driven high then the RS-458 port is in transmitting mode.

Please check paragraphs 4.3.12 and 4.4.3.2 for further details on serial ports enabling and console redirection

3.3.8 µSD slot

The SoCs used on SBC-B68-eNUC module offer a SD 3.0 compliant interface, that can be used to implement another mass storages media other than the optional internal eMMC and the two SATA interfaces.

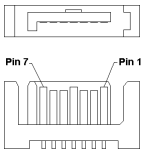
This SD interface is carried to a standard µSD card slot, soldered on top side of the module, push-push type.

3.3.9 S-ATA connectors

S-ATA Connector - CN8	
Pin	**Signal**
1	GND
2	SATA1_Tx+
3	SATA1_Tx-
4	GND
5	SATA1_Rx-
6	SATA1_Rx+
7	GND

The Apollo Lake family of SoCs embeds a SATA Controller, which offers two SATA III, 6.0 Gbps interfaces.

Of these interfaces, one SATA channel is carried out to a standard male S-ATA connector, CN8 (the other SATA channel is available on the M.2 KeyB socket, CN11, please check par. 3.3.10).



Here following the signals related to SATA interface:

SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair

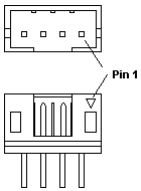
SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

S-ATA Power Connector - CN9	
Pin	**Signal**
1	---
2	GND
3	GND
4	+5V_S

A dedicated power connector, CN9, can be used to give supply to external Hard Disks (or Solid State Disks) connected to the SATA male connector.

The dedicated power connector is a 4-pin male connector, type MOLEX p/n 89400-0420 or equivalent, with pinout shown in the table on the left.



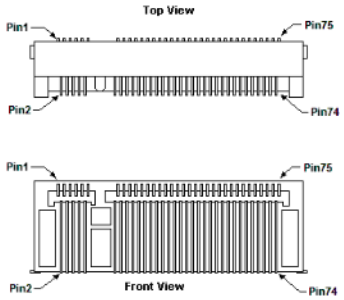
Mating connector: MOLEX 87369-0400 crimp housing with MOLEX 50212 crimp terminals.

An adapter cable for powering SATA disks from this connector is also contained inside the dedicated cable kit (CABKITB68) for SBC-B68-eNUC board. Please also check chapter 5.2.1for further details.

3.3.10 M.2 SSD/WWAN Slot: Socket 2 Key B

M.2 SSD/WWAN Slot (Socket 2 Key B type 3042/2260- CN11)			
Pin	**Signal**	**Pin**	**Signal**
1	CONF3	2	+3.3V_M2
3	GND	4	+3.3V_M2
5	GND	6	FULL_CARD_POWER_OFF#
7	USB_P2-	8	W_DISABLE1#
9	USB_P2+	10	---
11	GND		
		20	---
21	CONF0	22	---
23	WWAN_WAKE#	24	---
25	---	26	W_DISABLE2#
27	GND	28	---
29	PCIe0_Rx1-/USB_SSRX2-	30	UIM_RESET
31	PCIe0_Rx1+/USB_SSRX2+	32	UIM_CLK
33	GND	34	UIM_DATA
35	PCIe0_Tx1-/USB_SSTX2-	36	UIM_PWR
37	PCIe0_Tx1+/USB_SSTX2+	38	---
39	GND	40	---
41	PCIe0_Rx0+/SATA0_RX+	42	---
43	PCIe0_Rx0-/SATA0_RX-	44	---
45	GND	46	---
47	PCIe0_Tx0-/SATA0_TX-	48	---
49	PCIe0_Tx0+/SATA0_TX+	50	PLT_RST#
51	GND	52	PCIe_REQ0#
53	PCIe0_CLK+	54	PCIe_WAKE0#
55	PCIe0_CLK-	56	---
57	GND	58	---

The mass storage capabilities of the SBC-B68-eNUC are completed by an M.2 SSD Slot, which allow plugging M.2 Socket 2 Key B Solid State Drives.



The same slot can be used alternatively for the connection of Connectivity modules , using PCI-e x2 interface or USB 3.0 interface (USB interface is available simultaneously to SATA interface; both of them are alternative to PCI-e interface).

The connector used for the M.2 SSD slot is CN11, which is a standard 75 pin M.2 Key B connector, type LOTES p/n APCI0087-P001A, H=8.5mm, with the pinout shown in the table on the left.

On the SBC-B68-eNUC board there is also a Threaded Spacer which allows the placement of M.2 Socket 2 Key B SSD modules in 2260 size.

It is possible to place also modules in 2242 / 3042 size, by using a M/F Spacer which allow fixing the M.2 SSD on the spacer already available on the PCB, deemed for the fixing of the M.2 connectivity slot (see next paragraph).

Here following the signals related to the SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

Here following the signals related to the PCI-e interface:

PCIe0_Tx0+/PCIe0_Tx0-: PCI Express port #0 lane #0, Transmitting Output Differential pair

PCIe0_Rx0+/PCIe0_Rx0-: PCI Express port #0 lane #0, Receiving Input Differential pair

PCIe0_Tx1+/PCIe0_Tx1-: PCI Express port #0 lane #1, Transmitting Output Differential pair

PCIe0_Rx1+/PCIe0_Rx1-: PCI Express port #0 lane #1, Receiving Input Differential pair

PCIe0_Clock+ / PCIe0_Clock-: PCI Express Reference Clock for port #0, Differential Pair

PLT_RST#: Reset Signal that is sent from the SoC to all PCI-e devices available on the board (i.e. the GbE controllers, the PCI-e based modules plugged in the CN11 slot and the

59	---	60	---
61	---	62	---
63	---	64	---
65	---	66	---
67	---	68	---
69	CONF1	70	+3.3V_M2
71	GND	72	+3.3V_M2
73	GND	74	+3.3V_M2
75	CONF2		

connectivity modules plugged in CN12 slot). It is a 3.3V active-low signal.

PCIe_REQ0#: PCI Express Clock Request Input, active low signal. This signal shall be driven low by any module inserted in the connectivity slot, in order to ensure that the SoC makes available the reference clock.

PCIe_WAKE0#: Board's Wake Input, 3.3V_A active low signal with 10kΩ pull-up resistor. It must be externally driven by the Connectivity module plugged in the slot when it requires waking up the system.

Here following the signals related to the USB interface:

USB_P2+/USB_P2-: USB 2.0 Port #2 differential pair.

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair.

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair.

FULL_CARD_POWER_OFF#: Power Off signal for plugged modules, usually used in battery-powered systems. Fixed 2k2Ω pull-up @ 1.8V_A.

W_DISABLE1#: M.2 module disable signal #1, 3.3V_M2 active low output

W_DISABLE2#: M.2 module disable signal #2, 3.3V_M2 active low output

WWAN_WAKE#: Board's Wake Input, 1.8V_A active low signal with 100kΩ pull-up resistor. It must be externally driven by the Connectivity module plugged in the slot when it requires waking up the system (functionality not yet supported by the BIOS).

UIM_RESET: Reset signal line, sent from M.2 WWAN card to the UIM module.

UIM_DATA: Bidirectional Data line between M.2 WWAN card and UIM module.

UIM_CLK: Clock line, output from M.2 WWAN card to the UIM module.

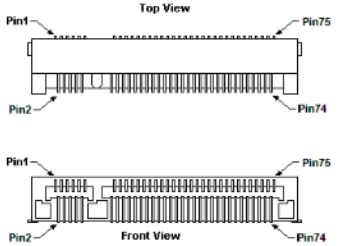
UIM_PWR: Power line for UIM module.

CONF0, CONF1, CONF2, CONF3: Configuration inputs, +3.3V_A signals with 10kΩ pull-up. This signal is necessary to switch between the S-ATA + USB signals and the PCI-e signals on the pins 29/31/35/37/41/43/47/49 of connector CN11. When CONFIG_1 signal is high, then PCI-e x 2 interface is available on connector CN20. When the signal is driven low, then SATA interface will be available. The selection is automatic, according to M.2 specifications for Socket2 Add-In Card configuration Table.

+3.3V_M2: 3.3 voltage for M.2 module, derived from +3.3V_A standby voltage.

3.3.11 M.2 Connectivity Slot: Key E Socket 1

M.2 Connectivity Slot: Socket 1 Key E type 2230 - CN12			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	+3.3V_A
3	USB_P4+	4	+3.3V_A
5	USB_P4-	6	---
7	GND	8	---
9	---	10	---
11	---	12	---
13	---	14	---
15	---	16	---
17	---	18	GND
19	---	20	---
21	---	22	---
23	---		
		32	---
33	GND	34	---
35	PCIe4_Tx+	36	---
37	PCIe4_Tx-	38	---
39	GND	40	---
41	PCIe4_Rx+	42	---
43	PCIe4_Rx-	44	---
45	GND	46	---
47	PCIe4_CLK+	48	---
49	PCIe4_CLK-	50	SUS_CLK
51	GND	52	PLT_RST#
53	PCIe_REQ1#	54	BT_DISABLE#
55	PCIe_WAKE1#	56	WIFI_DISABLE
57	GND	58	M.2_I2C_SDA



It is possible to increase the connectivity of the SBC-B68-eNUC board by using M.2 Socket 1 Key E connectivity slot.

The connector used for the M.2 Connectivity slot is CN12, which is a standard 75 pin M.2 Key E connector, type LOTES p/n APCI0076-P001A, H=4.2mm, with the pinout shown in the table on the left.

On the SBC-B68-eNUC board there is also a Threaded Spacer which allows the placement of M.2 Socket 1 Key E connectivity modules in 2230 size.

Here following the signals related to this connectivity interface:

USB_P4+/USB_P4-: USB 2.0 Port #4 differential pair.

PCIe4_TX+/PCIe4_TX-: PCI Express port #4, Transmitting Output Differential pair

PCIe4_RX+/PCIe4_RX-: PCI Express port #4, Receiving Input Differential pair

PCIe4_Clock+ / PCIe4_Clock-: PCI Express Reference Clock for port #4, Differential Pair

PCIe_WAKE1#: Board's Wake Input, 3.3V_A active low signal. It must be externally driven by the Connectivity module inserted in the slot when it requires waking up the system.

PLT_RST#: Reset Signal that is sent from the SoC to all PCI-e devices available on the board (i.e. the GbE controllers) and on the connectivity module. It is a 3.3V active-low signal.

PCIe_REQ1#: PCI Express Clock Request Input, active low signal. This signal shall be driven low by any module inserted in the connectivity slot, in order to ensure that the SoC makes available the reference clock.

SUS_CLK: 32.768kHz Clock provided by the SBC-B68-eNUC board to the module plugged in the slot CN12. +3.3V_A electrical level.

BT_DISABLE#: Bluetooth module disable, active low signal, +3.3V_A electrical level. This signal can be used to disable Bluetooth functionalities of any connectivity module plugged in CN12 Slot.

WIFI_DISABLE#; WiFi module disable, active low signal, +3.3V_A electrical level. This signal can be used to disable WiFi functionalities of any connectivity module plugged in CN16 Slot.

59	---	60	M.2_I2C_SCL
61	---	62	M.2_ALERT#
63	GND	64	---
65	---	66	---
67	---	68	---
69	GND	70	---
71	---	72	+3.3V_A
73	---	74	+3.3V_A
75	GND		

M.2_I2C_SDA: I2C Bus data line. Bidirectional signal, electrical level +3.3V_A with a 2K2Ω pull-up resistor. It is managed by SoC's I2C controller #0.

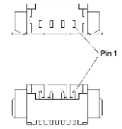
M.2_I2C_SCL: I2C Bus clock line. Bidirectional signal, electrical level +3.3V_A with a 2K2Ω pull-up resistor. It is managed by SoC's I2C controller #0.

M.2_ALERT#: I2C Bus Alert. Input signal, electrical level +3.3V_A with a 10KΩ pull-up resistor. It is managed through a SoC's GPIO.

3.3.12 FAN connectors

FAN Connector - CN6	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN
4	FAN_PWM

Depending on the usage model of SBC-B68-eNUC, for critical applications/environments on SBC-B68-eNUC it is available a 4-pin dedicated connector for an external +5V_{DC} FAN.



The default FAN Connector is a 4-pin single line SMT connector, type MOLEX 53261-0471 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 51021-0400 receptacle with MOLEX 50079-8000 female crimp terminals.

Optional FAN Connector - CN5	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN

Alternatively, as a factory option, the SBC-B68-eNUC module can be equipped with a 3-pin single line SMT connector, type MOLEX 53261-0371 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

Please refer to chapter 5.1 for considerations about thermal dissipation.

FAN_POWER: +5V_A derived power rail for FAN.

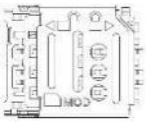
FAN_PWM: PWM output from the embedded microcontroller to the FAN (4-pin connector only).

FAN_TACHO_IN: tachometric input from the FAN to the embedded microcontroller, +3.3V_S electrical level signal with 10kΩ pull-up resistor and Schottky series diode.

3.3.13 microSIM Card Slot

microSIM Card Slot – CN10			
Pin	Signal	Pin	Signal
1	UIM_PWR	5	GND
2	UIM_RST#	6	---
3	UIM_CLK	7	UIM_DATA
4	---	8	---

Interfaced to the M.2 WWAN slot CN11, as already told in paragraph3.3.10, there is a microSIM Card Slot, to be used in conjunction with M.2 Socket 2 Key B modems. Here it is possible to insert the microSIM card provided by any telecommunication operator for the connection to their network.



The socket is type MOLEX. p/n 78800-0001or equivalent, with the pinout shown in the table on the left.

3.3.14 Feature connector

Feature connector – CN19			
Pin	Signal	Pin	Signal
1	+3.3V_A	2	+5V_A
3	GP_I2C4_SCL	4	GP_I2C5_SCL
5	GP_I2C4_SDA	6	GP_I2C5_SDA
7	GND	8	GND
9	GPIO_0	10	GPIO_4
11	GPIO_1	12	GPIO_5
13	GPIO_2	14	GPIO_6
15	GPIO_3	16	GPIO_7

Interfaced to the I2C interface #3 coming from the Intel® Apollo Lake family of SoCs, there is a device, NXP Semiconductors PCAL6408A, which is able to provide 8 General Purpose I/O pins. The device allows for a wide configurability of GPI/O pins, since it can offer programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs. Each I/O must be externally limited to a maximum of 25 mA, for a device total of 200 mA.

The device acts as a slave according to I2C protocol, and can be addressed at address 0100000 binary.

On the same connector are also available I2C ports #4 and #5, coming from the Intel® Apollo Lake family of SoCs.

The dedicated connector CN19 is an internal 16-pin standard male pin header, p 2.54 mm, 8+8 pin, h= 8mm, type TYCO p/n 5-146130-7 or equivalent.

GP_I2C4_SDA: I2C Bus data line. Bidirectional signal, electrical level +3.3V_A with a 2K2Ω pull-up resistor. It is managed by SoC's I2C controller #4.

GP_I2C4_SCL: I2C Bus clock line. Bidirectional signal, electrical level +3.3V_A with a 2K2Ω pull-up resistor. It is managed by SoC's I2C controller #4.

GP_I2C5_SDA: I2C Bus data line. Bidirectional signal, electrical level +3.3V_A with a 2K2Ω pull-up resistor. It is managed by SoC's I2C controller #5.

GP_I2C5_SCL: I2C Bus clock line. Bidirectional signal, electrical level +3.3V_A with a 2K2Ω pull-up resistor. It is managed by SoC's I2C controller #5.

GPIO_[0..7]: I/O Expander's Port P I/O# [0..7]. On these I/Os are placed also two 4-channel Diode Arrays, type DRTR5V0U4LP16, for ESD protection

It is possible to select the voltage reference level of these GPI/Os, which can be adjusted to be referred to +3.3V_A or to +5V_A voltage. This is a factory configuration, please take care of specifying which is the configuration needed.

3.3.15 Optional IR Receiver

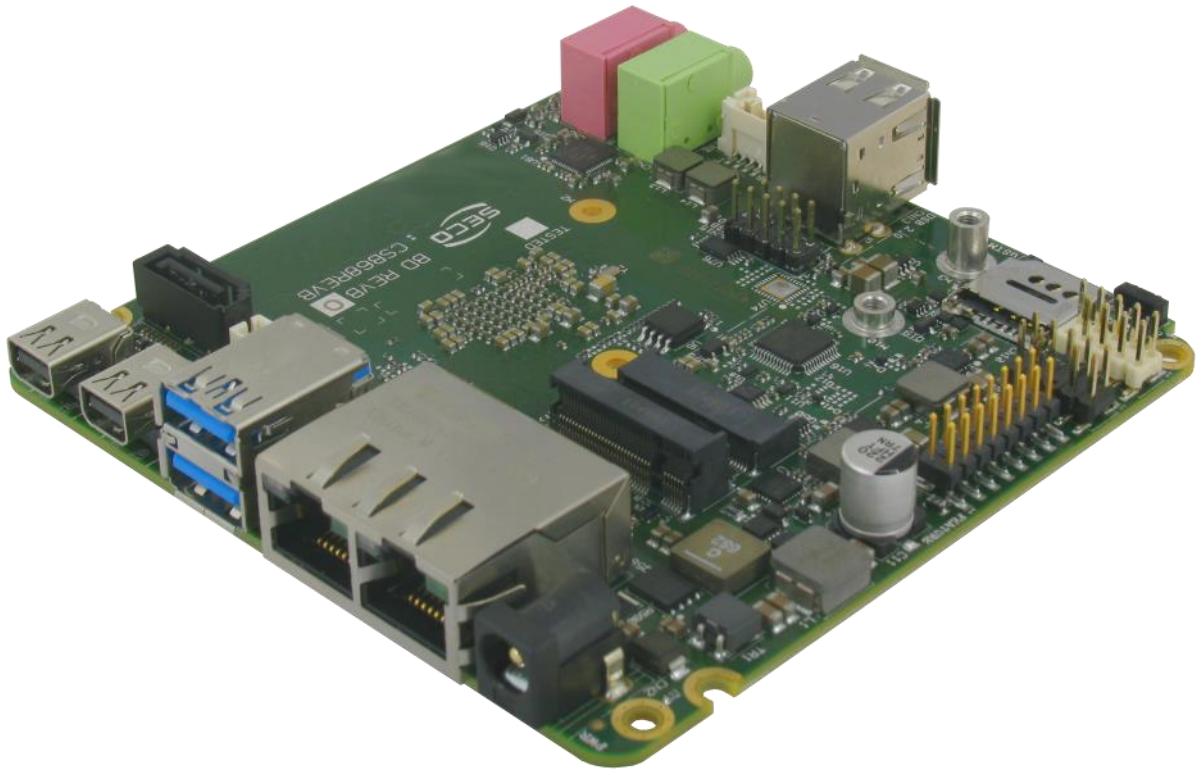
The SBC-B68-eNUC board can mount an optional IR receiver, which allows using a remote control when the board is placed in an enclosure (like, i.e., on Set Top Boxes).

The Infrared Receiver is SMD Type, p/n TSOP75238TR, and works with 38kHz carrier frequency.

The IR port is managed by the embedded microcontroller.

Chapter 4.
BIOS SETUP

- Aptio setup Utility
- Main setup menu
- Advanced menu
- Chipset menu
- Security menu
- Boot menu
- Save & Exit menu



4.1 Aptio setup Utility

Basic setup of the board can be done using American Megatrends, Inc. “Aptio Setup Utility”, that is stored inside an onboard SPI Serial Flash.

It is possible to access to Aptio Setup Utility by pressing the <ESC> key after System power up, during POST phase.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
+ / -	+ and - keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows displaying the General Help screen.
<F2>	Previous Values
<F3>	<F3> key allows loading Optimised Defaults for the board. After pressing <F3> BIOS Setup utility will request for a confirmation, before loading such default values. By pressing <ESC> key, this function will be aborted
<F4>	<F4> key allows save any changes made and exit Setup. After pressing <F4> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows discarding any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow displaying the setup sub-screens.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

4.2.1 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Trusted Computing	See submenu	Trusted Computing Settings
ACPI Settings	See submenu	System ACPI parameters
S5 RTC Wake Settings	See submenu	Enable system to wake from S5 using RTC alarm
Serial Port Console Redirection	See submenu	Serial Port Console Redirection
CPU Configuration	See submenu	CPU Configuration Parameters
AMI Graphic Output Protocol Policy	See submenu	User Selected Monitor Output by Graphic Output protocol
PCI subsystem Settings	See submenu	PCI Subsystem setting
Network Stack Configuration	See submenu	Network Stack Settings
CSM Configuration	See submenu	Compatibility Support Module(CSM) Configuration: Enable/Disable, Option ROM execution Settings, etc…
NVMe Configuration	See submenu	NVMe Device Options Settings
SDIO Configuration	See submenu	SDIO Configuration Parameters
USB Configuration	See submenu	USB Configuration Parameters
Platform Trust technology	See submenu	Platform Trust Technology Parameters
Main Thermal Configuration	See submenu	Main Thermal Configuration Parameters
HSUART Transceiver Configuration	See submenu	HSUART Transceiver Configuration Utility
LVDS Configuration	See submenu	LVDS Configuration submenu *(only available when external eDP-to-LVDS module is connected)*
SMBIOS Information	See submenu	SMBIOS Information
ACPI Devices Configuration	See submenu	ACPI Devices Configuration
Embedded Controller	See submenu	Embedded Controller Parameters

4.3.1 Trusted computing submenu

Menu Item	Options	Description
Security Device Support	Enabled / Disabled	Enables or Disables BIOS support for security device. OS will not show the Security Device. TCG EFI protocol and INT1A interface will not be available. When enabled all the following items will be available.
SHA-1 PCR Bank	Enabled / Disabled	Enables or Disables SHA-1 PCR Bank
SHA256 PCR Bank	Enabled / Disabled	Enables or Disables SHA256 PCR Bank
Pending Operation	None / TPM Clear	Schedule an Operation for the Security Device. NOTE: the. Computer will reboot during restart in order to change State of Security Device.
Platform Hierarchy	Enabled / Disabled	Enables or Disables the Platform Hierarchy
Storage Hierarchy	Enabled / Disabled	Enables or Disables the Storage Hierarchy
Endorsement Hierarchy	Enabled / Disabled	Enables or Disables the Endorsement Hierarchy
TPM2.0 UEFI Spec Version	TCG_1_2 TCG_2	Select the TCG Spec Version support. TCG_1_2 is the compatible mode for Windows 8 / Windows 10. TCG 2 supports the new TCG2 protocol and event format for Windows 10 or later.
Physical Presence Spec Version	1.2 / 1.3	Select to tell OS to support PPI Spec Version 1.2 or 1.3. Please note that some HCK tests might not support 1.3
Device Select	Auto TPM 1.2 TPM 2.0	TPM 1.2 will restrict the support to TPM 1.2 devices only, TPM 2.0 will restrict the support to TPM 2.0 devices only, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

4.3.2 ACPI Settings

Menu Item	Options	Description
Enable ACPI Auto Configuration	Disabled / Enabled	Enables or Disables BIOS ACPI Auto Configuration. The following menu items will appear only when this menu item is Disabled
Enable Hibernation	Disabled / Enabled	Enables or disables system ability to Hybernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled S3 (Suspend to RAM)	Select the highest ACPI Sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy resources	Disabled / Enabled	Enables or Disables Lock of Legacy resources

4.3.3 S5 RTC Wake Settings submenu

Menu Item	Options	Description
Wake System from S5	Disabled By Every day By Day of Month	Enables or Disables System wake on alarm event. When not diabled, the following items will appear
Wake up hour	0..23	Select the wake up hour in range 0..23. Enter 3 for 3am, 15 for 3pm.
Wake up minute	0..59	Select the wake up hour in range 0..59
Wake up second	0..59	Select the wake up hour in range 0..23. Enter 3 for 3am, 15 for 3pm.
Day of Month	1..31	Only available when "Wake System from S5" is set to "By Day of Month". Set the wake up day of month in range 1..31. Error checking will be done against mm/dd/yr combinations that are not valid).

4.3.4 Serial Port Console Redirection submenu

Menu Item	Options	Description
Console redirections	Enabled / Disabled	Enables or Disables the Console redirection. When enabled the following item will appear
Console Redirection Settings	See Submenu	The settings specify how the host and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings

4.3.4.1 Console Redirection Settings submenu

Menu Item	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 ANSI	Emulation: ANSI: Extended ASCII Char set. VT100: ASCII Char set. VT100+: extends VT100 to support colour, function keys, etc. VT-UTF8: uses UTF8 encoding to map Unicode chars onto 1 or more bytes
Bits per second	9600 / 19200 / 38400 / 57600 / 115200	Select Serial port Transmission Speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data bits	7 / 8	Set Console Redirection data bits
Parity	None Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the number of 1s in the data bits is even. Odd: parity bit is 0 if the number of 1s in the data bits is odd. Mark: parity bit is always 1. Space: parity bit is always 0. Mark and Space do not allow for error detection
Stop bits	1 / 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit
Flow Control	None Hardware RTS/CTS	Flow Control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses RTS# / CTS# lines to send the start / stop signals.
VT-UTF8 Combo Key Support	Enabled / Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	Enabled / Disabled	When this mode is enabled, only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled / Disabled	Enables or disables extended terminal resolution
Legacy OS Redirection Resolution	80x24 / 80x25	On Legacy OS, the number of Columns and Rows supported redirection
Putty Keypad	VT100 / Intel Linux / XTERMR6 / SCO / ESCN /VT400	Select FunctionKey and KeyPad on Putty
Redirection after BIOS POST	Always Enabled BootLoader	When BootLoader is selected, then Legacy Console redirection is disabled before booting to Legacy OS. When 'Always Enabled' is selected, then Legacy Console redirection is enabled for Legacy OS. Default setting for this option is set to 'Always Enabled'

4.3.5 CPU Configuration submenu

Menu Item	Options	Description
Detailed CPU Information		Shows board's specific SoC information
CPU Power Management	See Submenu	CPU Power Management options
Active Processor Cores	Disabled / Enabled	Number of Cores to enable in each processor package
Core 1 Core 2 Core 3	Disabled / Enabled	Core #x Enable / Disable. Only available when "Active Processor Cores" is enabled
Intel Virtualization Technology	Disabled / Enabled	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology
VT-d	Disabled / Enabled	Enables or disables CPU VT-d
Bi-directional PROCHOT	Disabled / Enabled	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor
Thermal Monitor	Disabled / Enabled	Enables or disables the Thermal Monitor
Monitor Mwait	Disabled / Enabled / Auto	Enables or disables Monitor Mwait
P-STATE Coordination	HW_ALL / SW_ALL / SW_ANY	Change P-STATE Coordination type
DTS	Disabled / Enabled / Auto	Enables or disables the Digital Thermal Sensor

4.3.5.1 CPU Power Management submenu

Menu Item	Options	Description
EIST	Disabled / Enabled	Enables or disables Intel® SpeedStep
Turbo mode	Disabled / Enabled	Only Available when "EIST" is enabled. Enables or disables the Turbo Mode
Boot Performance mode	Max performance Max battery	Select the performance state that the BIOS will set before OS handoff.
Power Limit 1 Enable	Disabled / Enabled	Enables or disables Power Limit 1. When Enabled, the following menu items will appear-
Power Limit 1 Clamp Mode	Disabled / Enabled	When Power Limit 1 is Enabled, enables or disables the Clamp Mode
Power Limit 1 Power	Auto / 3 / 4 / 5 / 6 / 7 / 8 / 9 / 10	Power Limit 1 in Watts. Auto will program Power Limit 1 based on silicon default support value.

Power Limit 1 Time Windows	Auto / 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8 / 10 / 12 / 14 / 16 / 20 / 24 / 28 / 32 / 40 / 48 / 56 / 64 / 80 / 96 / 112 / 128	Power Limit 1 Time Window Value in Seconds. Auto will program the Power Limit 1 Time Window based on silicon default support value

4.3.6 AMI graphic Output Protocol Policy submenu

Menu Item	Options	Description
Output Select	*List of available / connected module's video interfaces*	Sets the Video Output Interface. More options will be available only when more interfaces (DP1 / DP2 / eDP) are connected

4.3.7 PCI Subsystem settings submenu

Menu Item	Options	Description
Above 4G Decoding	Enabled/Disabled	Globally enables or disables 64-bit capable Devices to be decoded in space above 4GB (only if the System supports 64-bit PCI decoding)
CPU Power Management	See Submenu	Globally enables or disables Hot-Plug Support for the entire System. If the system has Hot-plug capable slots and this option is ste to Enabled, it will provide a setup screen for selecting PCI resources padding for Hot-plug.

4.3.8 Network Stack configuration submenu

Menu Item	Options	Description
Network Stack	Enabled / Disabled	Enables or disables UEFI Network Stack. When enabled, following menu items will appear
Ipv4 PXE Support	Enabled / Disabled	Enables or disables IPV4 PXE Boot Support. If disabled, IPV4 PXE boot option will not be created
Ipv4 HTTP Support	Enabled / Disabled	Enables or disables IPV4 HTTP Boot Support. If disabled, IPV4 HTTP boot option will not be created
Ipv6 PXE Support	Enabled / Disabled	Enables or disables IPV6 PXE Boot Support. If disabled, Ipv6 PXE boot option will not be created
Ipv6 HTTP Support	Enabled / Disabled	Enables or disables IPV6 HTTP Boot Support. If disabled, Ipv6 HTTP boot option will not be created
PXE boot wait time	[0..5]	Wait time to press ESC key to abort the PXE boot
Media detect count	[1..50]	Number of times that the presence of media will be checked

4.3.9 CSM configuration submenu

Menu Item	Options	Description
CSM Support	Enabled / Disabled	Enables or disables the Compatibility Support Module (CSM) Support. When enabled, the following menu items will appear
GateA20 Active	Upon Request Always	Upon Request: GateA20 can be disabled using BIOS services, Always: do not allow disabling GateA20; this option is useful when any RT code is executed above 1MB.
INT19 Trap Response	Immediate Postponed	BIOS Reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot
Boot option filter	UEFI and Legacy Legacy only UEFI only	This option controls Legacy / UEFI ROMs priority
Network	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy PXE OpROM
Storage	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Video OpROM
Other PCI devices	Do not launch UEFI Legacy	Determines the OpROM execution policy for devices other than Network, Storage and Video

4.3.10 NVMe configuration submenu

Informative screen only

4.3.11 SDIO configuration submenu

Menu Item	Options	Description
SDIO Access Mode	Auto ADMA SDMA PIO	Auto Option: Access the SD Device in DMA mode if the controller supports it, otherwise in PIO Mode. DMA Option: Access the SD Device in DMA mode ADMA Option: Access the SD Device in Advanced DMA mode PIO Option: Access the SD Device in PIO mode
List of SDIO devices found	Auto Floppy Forced FDD Hard Disk	Mass storage device emulation type. 'Auto' enumerates devices less than 530Mb as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD.

4.3.12 USB configuration submenu

Menu Item	Options	Description
Legacy USB Support	Enabled / Disabled / Auto	Enables Legacy USB Support. AUTO Option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
XHCI hand-off	Enabled/ Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enabled/ Disabled	Enables or disables USB Mass Storage Driver Support
USB Transfer time-out	1 sec / 5 sec / 10 sec / 20 sec	Sets the time-out value for Control, Bulk and Interrupt transfers
Device reset time-out	10 sec / 20 sec / 30 sec / 40 sec	USB mass storage device Start Unit command time-out
Device power-up delay	Auto / Manual	Sets the maximum time that the device will take before it properly reports itself to the Host controller. 'Auto' uses the default vale (for a Root port it is 100ms, for a Hub port the delay is taken from the Hub descriptor).
Device power-up delay in seconds	[1..40]	Delay range in seconds, in one second increment

4.3.13 Platform Trust technology submenu

Menu Item	Options	Description
fTPM	Enabled / Disabled	Enable/Disable fTPM

4.3.14 Main Thermal Configuration submenu

Menu Item	Options	Description
Critical Temperature (°C)	80 .. 125	Above this threshold, an ACPI aware OS will perform a critical shut-down. Allowed range is from 80 to 125 included, where 125 means disabled
Passive Cooling Temperature (°C)	60..120	Above this threshold, an ACPI aware OS will begin lowering the CPU speed. Allowed range is from 60 to 120 included, where values not below Critical Temperature mean disabled
TC1	0..16	Thermal Constant 1: part of the ACPI Passive Cooling Formula
TC2	0..16	Thermal Constant 2: part of the ACPI Passive Cooling Formula
TSP (seconds)	2..32	Period of temperature sampling when Passive Cooling

4.3.15 HSUART Transceiver. Configuration submenu

Menu Item	Options	Description
Interface	RS-232 RS-422 RS-485	Available both for HSUART #0 and #2. Allows selecting the type of interface among RS-232 (default), RS-422 or RS-485
RX Termination	Enabled / Disabled	Available both for HSUART #0 and #2 when corresponding interface is not set to RS-232. Allows disabling or enabling 120Ohm Termination on Rx differential Pair (RS-422mode) / Data Differential Pair (RS-485 mode)
TX Termination	Enabled / Disabled	Available both for HSUART #0 and #2 only when corresponding interface is set to RS-422. Allows disabling or enabling 120Ohm Termination on Tx differential Pair

4.3.16 LVDS configuration submenu

Menu Item	Options	Description
LVDS Interface	Disabled / Enabled	Enables or Disables LVDS Interface. When Enabled, all following items will appear.
Edid Mode	External / Default / Custom	Allows selecting External EDID parameters, or from a default list, or to fully customize the panel timings.
EDID	600x480 / 800x480 / 800x600 / 1024x600 / 1024x768 / 1280x720 / 1280x800 / 1280x1024 / 1366x768 / 1400x900 / 1600x900 / 1680x1050 / 1920x1080	This menu item is available only when Edid Mode is set to "Default" Select a software resolution (EDID setting) to use for the internal flat panel
Pixel Clock /10000	2500 .. 22400	Working Frequency in 10kHz units, e.g 6350 → 63.5MHz. For dual Channel devices, must be equal to two times the data-sheet value
Horizontal Active	*Numerical value*	Horizontal Addressable Video in pixels, aka Horizontal resolution (e.g. 1024 on a 1024x768 LFP). For dual Channel devices, must be equal to two times the data-sheet value.
Horizontal Blank	*Numerical value*	Horizontal Blanking pixels. It's equal to Horizontal Total – Horizontal Front Porch + Horizontal Pulse Width + Horizontal Back Porch. For dual Channel devices, must be equal to two times the data-sheet value
Vertical Active	*Numerical value*	Vertical Addressable Video in pixels, aka Vertical resolution (e.g. 768 on a 1024x768 LFP).
Vertical Blank	*Numerical value*	Vertical Blanking pixels. It's equal to Vertical Total – Vertical Active and Vertical Front Porch + Vertical Pulse Width + Vertical Back Porch.
Horizontal Offset	*Numerical value*	Horizontal Front Porch in pixels
Horizontal Pulse	*Numerical value*	Horizontal Sync Pulse Width in pixels
Vertical Offset	*Numerical value*	Vertical Front Porch in pixels
Vertical Pulse	*Numerical value*	Vertical Sync Pulse Width in pixels
Color Mode	VESA 24bpp JEIDA 24bpp 18 bpp	This menu item is available only when the module has the eDP-to-LVDS bridge installed. Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.
Interface	Single Channel Dual Channel	This menu item is available only when the module has the eDP-to-LVDS bridge installed. Allows configuration of LVDS interface in Single or Dual channel mode
LFP DE Polarity	Active High / Active Low	Data Enable Polarity
LFP V-Sync Polarity	Positive / negative	Vertical Sync Polarity

LFP H-Sync Polarity	Positive / negative	Horizontal Sync Polarity
LVDS Advanced Options	See Submenu	Advanced options for LVDS panel configuration

4.3.16.1 LVDS Advanced options submenu

Using this submenu, it is possible to set all the following parameters to meet the LVDS display requirements.

Menu Item	Options	Description
Spreading Depth	No Spreading / 0.5% / 1.0% / 1.5% / 2.0% / 2.5%	Sets percentage of bandwidth of LVDS clock frequency for spreading spectrum
Output Swing	150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV / 450 mV	Sets the LVDS differential output swing
T3 Timing	0 ÷ 255	Minimum T3 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 10 (500ms)
T4 Timing	0 ÷ 255	Minimum T4 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 2 (100ms)
T12 Timing	0 ÷ 255	Minimum T12 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 20 (1s)
T2 Delay	Enabled / Disabled	When Enabled, T2 is delayed by 20ms ± 50%
T5 Delay	Enabled / Disabled	When Enabled, T5 is delayed by 20ms ± 50%
P/N Pairs Swapping	Enabled / Disabled	Enable or disable LVDS Differential pairs swapping (Positive ⇔ Negative)
Pairs Order Swapping	Enabled / Disabled	Enable or disable channel differential pairs order swapping (A ⇔ D, B ⇔ CLK, C ⇔ C)
LVDS BUS Swapping	Enabled / Disabled	Enable or disable Bus swapping (Odd ⇔ Even)
Firmware PLL	0: +/- 1.56% 1: +/- 3.12% 2: +/- 6.25% 3: +/- 12.5% 4: +/- 25% 5: +/-50% 6: +/-100%	Firmware PLL range

4.3.17 SMBios Information

Informative screen only

4.3.18 ACPI Devices configuration submenu

Menu Item	Options	Description
I2C Device Configuration	See Submenu	Allows installing external I2C Devices (enumerated from #17 up to #24) on ACPI aware OS

4.3.18.1 I2C Device configuration submenu

Menu Item	Options	Description
Device Type	Disabled 7bits 10 bits	Select I2C device #x Address format. For each device that is not disabled, the following items will appear
Address	*HEX Value*	Sets I2C device address
Speed	Standard mode Fast mode Fast-mode Plus	Configures I2C bus speed. Standard mode = 100kb/s Fast mode = 400kb/s Fast-mode Plus = 3.4Mb/s

4.3.19 Embedded Controller submenu

Menu Item	Options	Description
State After G3	Always ON Always OFF Last State	Specifies what must happen when power is re-applied after a power failure (G3 state). Always ON: the System will boot directly as soon as the power is applied. Always OFF: the system remain in power off State until power button is pressed
No C-MOS battery handling	Disabled / Enabled	Only available When "State After G3" is not set to "Always ON". In systems without C-MOS battery, the chipset will always power on after a power failure. In case "State after G3" is set to "Always OFF", or in case is set to "Last State" an the Last State was OFF, then the board will perform an immediate shutdown
Watchdog	Disabled / Enabled	Enables or disables the Watchdog. When enabled, the following parameters will appear.
Watchdog action	System Reset Power Button 1s Power Button 4s (Shutdown)	Action executed at the firing of the watchdog timeout.
Delay to Start (Sec.)	[0..600]	Seconds of delay before the watchdog timer starts counting.
Timeout (Sec.)	[20..599]	Watchdog Timeout.
Watchdog Event	Disabled / Enabled	High Active output watchdog event indicator
Deep Sleep	Disabled / Enabled	Put the system in a low power state after shutdown. Only a power button pulse will be able to wake the system from this state.
Int. PWM Frequency (Hz)	0..65535	Sets Internal PWM Frequency (Hz)
Int. PWM DC (%)	0..100	Sets Internal Duty Cycle (%)
AC0 temperature (°C)	50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100 / 105 / 110 / 115 / 120	AC0. Above this temperature, the FAN starts to run at full speed
AC1 temperature (°C)	15 / 20 / 25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100 / 105 / 110 / 115 / 120	AC1. Below this temperature, the FAN is OFF.
FAN Duty Cycle (%) Above AC1	50 / 75 / 100	FAN Duty Cycle between AC1 and AC0.
User Non Volatile Storage Content		Open a page showing the user Non Volatile Storage Area Contents

4.4 Chipset menu

Menu Item	Options	Description
South Bridge		South Bridge Parameters
Uncore Configuration		Uncore Configuration Parameters
South Cluster Configuration		South Cluster Configuration Parameters

4.4.1 South Bridge submenu

Menu Item	Options	Description
OS Selection	Windows / Android / Win7 / Intel Linux	Select the Target OS

4.4.2 Uncore Configuration submenu

Menu Item	Options	Description
GOP Brightness Level	[0..255]	Set Graphics Output Protocol (GOP) Brightness Level; value ranges from 0 to 255
DDI0 DDC Pull Type DDI1 DDC Pull Type	Pull Up 1K Pull Up 2K Pull Up 5K	Sets DDI #0 /DDI #1 Pull-up values
DDI0 Configuration Override	Disabled DP++ (Multimode DP) HDMI/DVI	Allows overriding default DDI0 configuration
LFP port	Disabled / eDP	Allows to override default eDP configuration
Integrated Graphics Device	Enabled / Disabled	Enable the Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor, or always disable it.
Primary Display	IGD / PCIe / HG	Select which of IGD / PCIe /HG graphics device should be the Primary Display
HG Delay After Power Enable	[0..1000]	Delay in milliseconds after power enable. Only available when Primary Display is set to "HG"
HG Delay After Hold Reset	[0..1000]	Delay in milliseconds after hold reset. Only available when Primary Display is set to "HG"
RC6 (Render Standby)	Enabled / Disabled	Permits to enable the render standby features, which allows the on-board graphics entering in standby mode to decrease power consumption
GTT Size	2 MB / 4 MB / 8 MB	Select the GTT (Graphics Translation Table) Size
Aperture Size	128 MB / 256 MB / 512 MB	Use this item to set the total size of Memory that must be left to the GFX Engine
DVMT Pre-Allocated	64M / 96M / 128M / 160M / 192M / 224M / 256M / 288M / 320M / 352M / 384M / 416M / 448M / 480M / 512M	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphic Device
DVMT Total Gfx Mem	128M / 256M / MAX	Select the size of DVMT (Dynamic Video Memory) 5.0 that the Internal Graphics Device will use
Cd Clock Frequency	144 MHz / 288 MHz / 384 MHz / 576 MHz / 624 MHz	Select the highest CD Clock frequency supported by the platform
GT PM Support	Enabled / Disabled	Enable / Disable GT Power Management
PAVP	Enabled / Disabled	Enable / Disable Protected Audio Video Playback (PAVP)
Memory Scrambler	Enabled / Disabled	Enable / Disable the Memory Scrambler Support

4.4.3 South Cluster Configuration submenu

Menu Item	Options	Description
HD Audio Configuration	See submenu	HD Audio Configuration Settings
LPSS Configuration	See submenu	Low Power Sub System Configuration Settings
PCI Express Configuration	See submenu	PCI Express Configuration Settings
SATA Drives	See submenu	SATA Devices Configuration Setup options
SCC Configuration	See submenu	Storage Control Cluster Configuration Settings
USB Configuration	See submenu	USB configuration Settings
Miscellaneous Configuration	See submenu	Miscellaneous Settings

4.4.3.1 HD Audio Configuration submenu

Menu Item	Options	Description
HD Audio Support	Enabled / Disabled	Enable / Disable HD Audio Support
HD- Audio DSP	Enabled / Disabled	Enable / Disable HD Audio DSP

4.4.3.2 LPSS Configuration submenu

Menu Item	Options	Description
I2C #0 (D22:F0) – M.2 Socket CN12	Disable / PCI Mode / ACPI Mode	Enable/Disable LPSS I2C #0 Support. This I2C port is available on M.2 Socket CN12
Set LPSS I2C #0 Speed	Standard Mode Fast Mode Fast Plus Mode	Only available when LPSS I2C #0 is not disabled. Select LPSS I2C #0 Speed
I2C #3 (D22:F3) – GPIO Exp. PCAL64	Disable / PCI Mode / ACPI Mode	Enable/Disable LPSS I2C #3 Support, which is used to communicate with the GPI/O Expander
Set LPSS I2C #3 Speed	Standard Mode Fast Mode Fast Plus Mode	Only available when LPSS I2C #3 is not disabled. Select LPSS I2C #3 Speed
I2C #4 (D23:F0) – CN19 Pin 3/5	Disable / PCI Mode / ACPI Mode	Enable/Disable LPSS I2C #4 Support. This I2C port is available on connector CN19, pins 3 and 5
Set LPSS I2C #4 Speed	Standard Mode Fast Mode Fast Plus Mode	Only available when LPSS I2C #4 is not disabled. Select LPSS I2C #4 Speed
I2C #5 (D23:F1) – CN19 Pin 4/6	Disable / PCI Mode / ACPI Mode	Enable/Disable LPSS I2C #5 Support. This I2C port is available on connector CN19, pins 4 and 6
Set LPSS I2C #5 Speed	Standard Mode Fast Mode Fast Plus Mode	Only available when LPSS I2C #5 is not disabled. Select LPSS I2C #5 Speed
HSUART #0 (D24:F0) – CN16	Disable / PCI Mode / ACPI Mode	Enable / Disable LPSS HS-UART #0 Support, available on connector CN16
Virtual COM 0 Enable	Enable / Disable	Enable / Disable Virtual COM 0 Subdevice in ACPI Tables
HSUART #2 (D24:F2) – CN16	Disable / PCI Mode / ACPI Mode	Enable / Disable LPSS HS-UART #2 Support, available on connector CN16
Virtual COM 1 Enable	Enable / Disable	Enable / Disable Virtual COM 1 Subdevice in ACPI Tables

4.4.3.3 PCI Express Configuration submenu

Menu Item	Options	Description
Compliance Mode	Enabled / Disabled	Compliance Mode Enable/Disable
PCIE Root Port 1 – M.2 2230 (CN12) PCIE Root Port 3 – M.2 2260/3042 (CN11) PCIE Root Port 5 – LAN0 CN17A PCIE Root Port 6 – LAN1 CN17B	See Submenu	Sets the parameters for each single PCI-e Root Port

4.4.3.3.1 PCIE Root Port #x submenus

Menu Item	Options	Description
PCIE Root Port 1 – M.2 2230 (CN12) PCIE Root Port 3 – M.2 2260/3042 (CN11) PCIE Root Port 5 – LAN0 CN17A PCIE Root Port 6 – LAN1 CN17B	Auto Enabled Disabled	Controls the PCI Express Root Port. AUTO: disable unused root port automatically for the most optimised power saving. Enable: Always enable the PCIe root port. Disable: Always disable the PCIe root port *(all the following items will disappear)*
ASPM	Disable / L0s	PCI Express Active State Power Management Settings
PCIe Speed	Auto / Gen1 / Gen2	Configure PCIe Speed

4.4.3.4 SATA Drives Configuration submenu

Menu Item	Options	Description
SATA Controller	Enabled / Disabled	Enables or Disables the Chipset SATA controller, which supports the 2 internal SATA ports available on connectors CN8 and CN11r (up to 3GB/s supported per port).
SATA Test Mode	Enabled / Disabled	Enable / Disable SATA Test Modes
Port 0 Port 1	Enabled / Disabled	Enable / Disable SATA Port #x

4.4.3.5 SCC Configuration submenu

Menu Item	Options	Description
SCC SD Card Support	Enabled / Disabled	Enable or Disable SCC SD Card Support
SCC eMMC Support	Enabled / Disabled	Enable or Disable SCC eMMC Support

4.4.3.6 USB Configuration submenu

Menu Item	Options	Description
xHCI Pre-Boot Driver	Enable / Disable	Enables or Disable the support for XHCI Pre-boot driver.
xHCI Mode	Enable / Disable	Once Disabled, the xHCI Controller would be function disabled, none of the USB devices will be detectable and usable during the boot and in the OS. Do not disable it unless for debug purposes.
USB VBUS	ON / Off	VBUS should be ON in USB Host mode. It should be OFF in OTG Device mode.
USB Port Disable Override	Enable / Disable	Allows enabling or disabling selectively each single USB port from reporting a device connection to the controller.
USB Port #0 USB Port #1 USB Port #2 USB Port #3 USB Port #4 USB Port #5 USB Port #6 USB Port #7 USB 3 Port #0 USB 3 Port #1 USB 3 Port #2	Disable Enable	Only available when "USB Port Disable Override" is Enables. Enables or disables the single USB Port #x. Once disabled, any USB device connected to the corresponding port will not be detected by the BIOS neither by the OS
XDCI Support	Disable / PCI Mode	Enables or Disables the XDCI (USB Device)
XHCI Disable Compliance Mode	True / False	Options to disable xHCI Link Compliance Mode. Set True to disable the Compliance Mode, False to leave it enabled

4.4.3.7 Miscellaneous Configuration submenu

Menu Item	Options	Description
Wake On Lan	Enabled / Disabled	Enable or disable the Wake On LAN Feature
BIOS Lock	Enabled / Disabled	Enables or disables the SC BIOS Lock enable feature. It is required that it is enabled to ensure BIOS SPI region write protect
Flash Protection Range Registers (FPRR)	Enabled / Disabled	Enable Flash Protection Range registers

4.5 Security menu

Menu Item	Options	Description
Setup Administrator Password		Set Setup Administrator Password
User Password		Set User Password
Secure Boot	See Submenu	Customizable Secure Boot Settings

4.5.1 Secure Boot submenu

Menu Item	Options	Description
Secure Boot	Enabled / Disabled	Secure Boot is activated when the Platform Key (PK) is enrolled, System Mode is User/Deployed and CSM function is disabled.
Secure Boot Mode	Standard / Custom	Set UEFI Secure Boot Mode to STANDARD Mode or CUSTOM mode. This change will be effective after save. And after reset, the mode will return to Standard
Restore factory keys	Yes / No	Only available when "Secure Boot Mode" is set to "Custom". Forces System to User Mode. Configure NVRAM so that it contain OEM-defined factory default Secure Boot Keys.
Reset to Setup Mode	Yes / No	Only available when "Secure Boot Mode" is set to "Custom". Delete the NVRAM content of all UEFI Secure Boot key databases.
Key management	See submenu	Only available when "Secure Boot Mode" is set to "Custom". Enables expert users to modify Secure Boot Policy variables without full authentication

4.5.1.1 Key Management submenu

Menu Item	Options	Description
Factory Keys Provision	Disabled / Enabled	Provision factory default keys on next re-boot only when the system is in Setup Mode
Restore factory keys	Yes / No	Forces System to User Mode. Configure NVRAM so that it contain OEM-defined factory default Secure Boot Keys.
Reset to Setup Mode	Yes / No	Delete the NVRAM content of all UEFI Secure Boot key databases.
Export Secure Boot variable		Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device
Enroll Efi Image	*File System Image*	Allow the selected image to run in Secure Boot mode. Enrol SHA256 Hash Certificates of the Image into Authorized Signature Database (db)
Remove 'UEFI CA' from DB	Yes / No	Device Guard ready system must not list in 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)
Restore DB defaults	Yes / No	Restore DB variable to factory defaults
Platform key (PK) Key Exchange Keys Authorized Signatures Forbidden Signatures Authorized Timestamps OS Recovery Signatures	Details Export Append Update Delete	Enrol factory Defaults or load certificates from a file: 1. Public Key Certificate in: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER encoded) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHA256,384,512 2. Authenticated UEFI variables 3. EFI PE/COFF Image (SHA256) Key Source: factory, External, Mixed

4.6 Boot menu

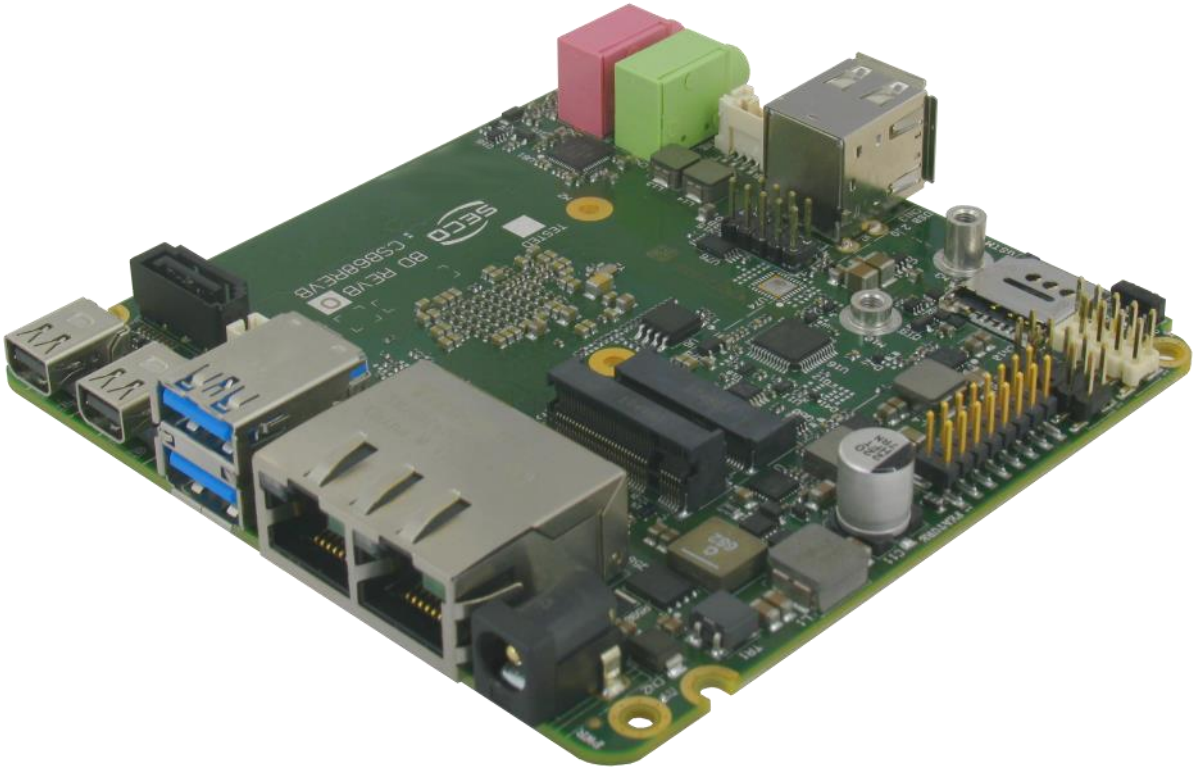
Menu Item	Options	Description
Setup Prompt Timeout	0 .. 65535	Number of seconds to wait for setup activation key. 65535 means indefinite waiting.
Bootup NumLock State	On / Off	Select the Keyboard NumLock State at boot
Quiet Boot	Enabled / Disabled	Enables or Disables Quiet Boot options
New Boot Option Policy	Default Place First Place Last	Controls the placement of newly detected UEFI boot options
Boot Mode Select	LEGACY UEFI	Select the boot mode between Legacy and UEFI
Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4 Boot Option #5 Boot Option #6 Boot Option #7 Boot Option #8	Hard Disk0 Hard Disk 1 eMMC CD/DVD SD USB Device Network Other Device Disabled	Select the system boot order
UEFI Hard Disk BSB priorities	*List of UEFI bootable drives*	Specifies the Boot Device Priority Sequence from available UEFI Hard Disk Drives
UEFI Other Drive BBS Priorities	*List of other UEFI drives*	Specifies the Boot Device Priority Sequence from available UEFI Other Drives

4.7 Save & Exit menu

Menu Item	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Changes and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset the system without saving any changes.
Save Changes		Save the changes done so far to any of the setup options.
Discard Changes		Discard the changes done so far to any of the setup options.
Restore Defaults		Restore/Load Default values for all the setup options
Save as User Defaults		Save the changes done so far as User Defaults
Restore User Defaults		Restore the User Defaults to all the setup options
List of EFI boot options		
Launch EFI Shell from filesystem device		Attempt to Launch the EFI Shell application (Shell.efi) from one of the available filesystem devices

Chapter 5.
APPENDICES

- Thermal Design
- Accessories



5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like SBC-B68-eNUC board, offer to the user very good performances in minimal spaces, therefore allowing the system's minimization. On the counterpart, the miniaturizing of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

The board can be used along with specific heatspreaders, but please remember that they will act only as thermal coupling device between the board itself and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimize the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

When using SBC-B68-eNUC boards, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilization.

Until the board is used on a laboratory shelf, on free air, just for software development and system tuning, then a heatsink with integrated fan could be sufficient for board's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all SoCs versions.

Therefore, it is always necessary that the customer studies and develops accurately the cooling solution for his system, by evaluating processor's workload, utilization scenarios, the enclosures of the system, the air flow and so on.

SECO can provide SBC-B68-eNUC specific heatspreaders, passive heatsinks and heatsinks with fan, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

The customer shall always ensure that the heatspreader/heatsink surface temperature remains in the range 0 ÷ 60 °C.

Ordering Code	Description
SB68-DISS-1-C	SBC-B68-eNUC Heatspreader Kit for commercial temperature range SoCs
SB68-DISS-1-i	SBC-B68-eNUC Heatspreader Kit for industrial temperature range SoCs

5.2 Accessories

SECO can offer various accessories in completion of SBC-B68-eNUC functionalities

5.2.1 Accessories kit CABKITB68

This accessories kit includes the following items

- *Dual USB 2.0 Type A adapter with standard PC mounting plate*. Can be used to carry out the signals of internal USB ports #2-#3 (connector CN11) to standard USB 2.0 Type A receptacles
- *Front Panel I/O board* V995, which allows the integration on a panel of an optional enclosure of two Audio jacks (Earphone and Mic in), Reset Button, Power button and two LED (for SATA activity and Power Status of the board itself).

For fixing of the front panel I/O board to the external enclosure's panel, the module is equipped with two brackets and screws for the fixing of the brackets to the module.

- Cables for connection of the Front Panel I/O board to SBC-B68-eNUC board.

Connection cable CV-837/30 is needed for audio functionalities; it is not used with SBC-B68-eNUC board.

Connection cable CV-836/30 is needed for connection of power and reset pushbuttons and SATA / power LEDs; it has to be connected to SBC-B68-eNUC board's connector CN7 and to V995 module's connector CN1.

- Serial adapter cable CV-904/20. It can be used to carry out the signals of RS-232/RS-422/RS-485 signals available on the connector CN16 to two standard DB-9 male connectors.
- SATA power cable, for connection of power rails of external SATA disks / SSDs to internal SATA power connector CN9.
- Feature connection cable CV-1088/200, for the usage of I2C ports and GPIOs available on connector CN19
- Speaker adapter cable, CV-854/30, to be used for the connection of external speakers (not included with the cable) to board's connector CN26

5.2.2 USB-to-Serial port converter modules

This optional module has been designed to convert one of the internal USB ports available on connector CN15 into a serial port, which can be of RS-232, RS-422 or RS-485 type (fixed configuration).

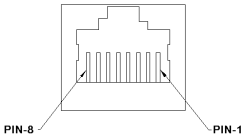
Depending on the type of serial port needed, different module configurations are available; moreover, the output of the module can be available on standard DB-9 male connector or on RJ-45 sockets.

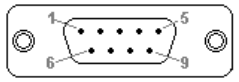
All modules type mounts an FTDI FT232R USB-to-Serial UART interface IC; RS-232 converter module then mounts a Serial Port RS-232 Transceiver with 15kV ESD protection. Instead, the other converters mount and RS-485/RS-422 transceiver.

Modules with DB-9 connector				Modules with RJ-45 socket			
Pin	Signal RS-232 converter	Signal RS-422 converter	Signal RS-485 converter	Pin	Signal RS-232 converter	Signal RS-422 converter	Signal RS-485 converter
1	DCD#	N.C.	N.C.	1	DTR#	N.C.	N.C.
2	RX	RX-	N.C.	2	CTS#	RX+	N.C.
3	TX	TX-	RX- / TX-	3	N.C.	N.C.	N.C.
4	DTR#	N.C.	N.C.	4	RX	RX-	N.C.
5	GND	GND	GND	5	N.C.	N.C.	N.C.
6	DSR#	N.C.	N.C.	6	TX	TX-	RX- / TX-
7	RTS#	TX+	RX+ / TX+	7	GND	GND	GND
8	CTS#	RX+	N.C.	8	RTS#	TX+	RX+ / TX+
9	RI#	N.C	N.C.				

In the table on the left are shown the pinout of DB-9 connector and of RJ-45 socket for all kind of modules.

120Ω termination resistors on differential pairs are available both on RS-422 and on RS-485 modules.





Ordering Code	Description
VA13-0000-1100-C0	USB to RS232 serial port converter with DB9 connector
VA13-0000-1200-C0	USB to RS422 serial port converter with DB9 connector
VA13-0000-1300-C0	USB to RS485 serial port converter with DB9 connector
VA13-0000-2100-C0	USB to RS232 serial port converter with RJ-45 connector
VA13-0000-2200-C0	USB to RS422 serial port converter with RJ-45 connector
VA13-0000-2300-C0	USB to RS485 serial port converter with RJ-45 connector

5.2.3 eDP-to-LVDS converter

This optional module has been designed to convert the eDP interface available on connector CN22 into a Single or Dual Channel 18- / 24-bit LVDS interface by using an NXP PTN3460I eDP to LVDS bridge.

eDP connector - CN2			
Pin	**Signal**	**Pin**	**Signal**
1	---	21	SW_VDD
2	GND	22	---
3	---	23	GND
4	---	24	GND
5	GND	25	GND
6	---	26	GND
7	---	27	eDP_HPD
8	GND	28	GND
9	eDP_TX1-	29	GND
10	eDP_TX1+	30	GND
11	GND	31	GND
12	eDP_TX0-	32	---
13	eDP_TX0+	33	eDP_BLT_CTRL
14	GND	34	PTN_SMB_DAT
15	eDP_AUX+	35	PTN_SMB_CLK
16	eDP_AUX-	36	SW_BACK
17	GND	37	SW_BACK
18	SW_VDD	38	SW_BACK
19	SW_VDD	39	SW_BACK
20	SW_VDD	40	3.3V_S

The eDP interface of the module is carried to another VESA® certified connectors for embedded Display Port interface, type STARCONN p/n 300E40-0110RA-G3 or equivalent (microcoaxial cable connector, 0.5mm pitch, 40 positions). It is the same identical connector to SBC-B68-eNUC board's connector CN22. The pinout is shown in the table on the left.

Only 2-lane eDP interface is required for this module.

For signals' description please refer to paragraph 3.3.4

SW_VDD and SW_BACK voltages are used only to drive the display, they are not used for module's working (see further on).

Please be aware that the eDP-to-LVDS converter is not provided with the connecting eDP cable, which must be purchased apart. SECO can provide for this cable, ordering code: YZ20453-40-20453-40/300 - eDP COAXIAL CABLE I-PEX 20453-040T-01 with pull bar to I-PEX 20453-040T-01 with pull bar (Inverted signals) L=200mm.

All the signals necessary for working of the eDP to LVDS converter module can be found on connector CN2, which can be paired to SBC-B68-eNUC board using a 1:1 direct cable connection.

I2C female connector - CN4				I2C male connector - CN5			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
2	---	1	+3.3V_A	1	---	2	+3.3V_A
4	GP_I2C_CLK	3	---	3	GP_I2C_CLK	4	---
6	GP_I2C_DAT	5	---	5	GP_I2C_DAT	6	---
8	GND	7	GND	7	GND	8	GND
10	---	9	LVDS_RST#	9	---	10	LVDS_RST#
12	---	11	---	11	---	12	---
14	---	13	---	13	---	14	---
16	---	15	---	15	---	16	---

For the occurrences when the module is paired to different boards, or when the SM_Bus is not working / connectable on connector CN2, then the module offers also the possibility of connecting to another board's I2C interface using a dedicated 16-pin connector. Such a connector is available in two factory option, as a male 2x8 pin header p 2.54mm h= 6mm (CN5), or as a female 2x8 pin connector, p2.54mm, h=11.04mm type NELTRON p/n 2214123-16G10-1B-32 (CN4) for piggyback connection

GP_I2C_CLK: General Purpose I2C Clock line

GP_I2C_DAT: General Purpose I2C Data line

LVDS_RST#: General purpose Input signal. Can be used for LVDS section's reset. 3.3V input signal with 100kΩ pull-up resistor, active low.

The I2C bus available on connectors CN4/CN5 can be used in alternative to SM Bus interface available on connector CN2 to manage the eDP to LVDS bridge.

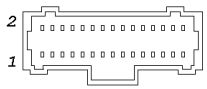
It is necessary to configure properly the module in order to use the General Purpose I2C bus (CN4/CN5) or SM Bus (CN2). The selection must be made using dip switch SW1

SW1 Switch	ON Position	OFF Position
1	SM Bus used	GP_I2C used
2	eDP-to-LVDS bridge acts as I2C bus slave	eDP-to-LVDS bridge acts as I2C bus master, can read from external EEPROM

Setting of these signals can be made according to the table on the left.

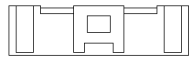
For use with SB68 board, it is suggested to set both SW1 switches in position ON

Finally, the LVDS interface is available on a connector type HR A1014WVA-S-2x25P or equivalent (2 x 25p, male, straight, P1, low profile, polarised) is provided, with the pin-out indicated in the following table (different configurations are shown).



Mating connector: HR A1014H-2X25P with HR A1014-T female crimp terminals.

Alternative mating connector, MOLEX 501189-5010 with crimp terminals series 501334.



When building a cable for connection of LVDS displays, please take care of twist as tight as possible differential pairs' signal wires, in order to reduce EMI interferences. Shielded cables are also recommended.

LVDS connector - CN3			
Pin	Signal	Pin	Signal
1	GND	2	GND
3	LVDS_ODD_TX3+	4	LVDS_EVEN_TX3+
5	LVDS_ODD_TX3-	6	LVDS_EVEN_TX3-
7	LVDS_ODD_TX2+	8	LVDS_EVEN_TX2+
9	LVDS_ODD_TX2-	10	LVDS_EVEN_TX2-
11	LVDS_ODD_TX1+	12	LVDS_EVEN_TX1+
13	LVDS_ODD_TX1-	14	LVDS_EVEN_TX1-
15	LVDS_ODD_TX0+	16	LVDS_EVEN_TX0+
17	LVDS_ODD_TX0-	18	LVDS_EVEN_TX0-
19	GND	20	GND
21	LVDS_ODD_CLK+	22	LVDS_EVEN_CLK+
23	LVDS_ODD_CLK-	24	LVDS_EVEN_CLK-
25	GND	26	GND
27	LVDS_DDC_CLK	28	BKLT_EN
29	LVDS_DDC_DATA	30	eDP_BLT_CTRL
31	+3.3V	32	VDD_ON
33	SW_VDD_LVDS	34	SW_BACK_LVDS
35	SW_VDD_LVDS	36	SW_BACK_LVDS
37	SW_VDD_LVDS	38	SW_BACK_LVDS
39	GND	40	GND
41	GND	42	GND
43	GND	44	GND
45	---	46	---
47	---	48	---
49	+3.3V	50	GND

Here following the signals related to LVDS management:

LVDS_ODD_TX0+/ LVDS_ODD_TX0-: LVDS Odd Channel differential data pair #0.

LVDS_ODD_TX1+/ LVDS_ODD_TX1-: LVDS Odd Channel differential data pair #1.

LVDS_ODD_TX2+/ LVDS_ODD_TX2-: LVDS Odd Channel differential data pair #2.

LVDS_ODD_TX3+/ LVDS_ODD_TX3-: LVDS Odd Channel differential data pair #3.

LVDS_ODD_CLK+/LVDS_ODD_CLK-: LVDS Odd Channel differential Clock.

LVDS_EVEN_TX0+/ LVDS_EVEN_TX0-: LVDS Even Channel differential data pair #0.

LVDS_EVEN_TX1+/ LVDS_EVEN_TX1-: LVDS Even Channel differential data pair #1.

LVDS_EVEN_TX2+/ LVDS_EVEN_TX2-: LVDS Even Channel differential data pair #2.

LVDS_EVEN_TX3+/ LVDS_EVEN_TX3-: LVDS Even Channel differential data pair #3.

LVDS_EVEN_CLK+/LVDS_EVEN_CLK-: LVDS Even Channel differential Clock.

LVDS_DDC_DAT: DisplayID DDC Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 4k7Ω pull-up resistor.

LVDS_DDC_CLK: DisplayID DDC Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 4k7Ω pull-up resistor.

BKLT_EN: +3.3V electrical level Output, Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected displays.

VDD_ON: +3.3V electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected display.

eDP_BLT_CTRL: this signal can be used to adjust the backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

Display supply voltages (SW_VDD_LVDS) and backlight supply voltage (SW_BACK_LVDS) are derived by SW_VDD and SW_BACK voltages, carried to the module through the eDP connector CN2, simply by turning them On and Off using signals VDD_ON and BKLT_EN.

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