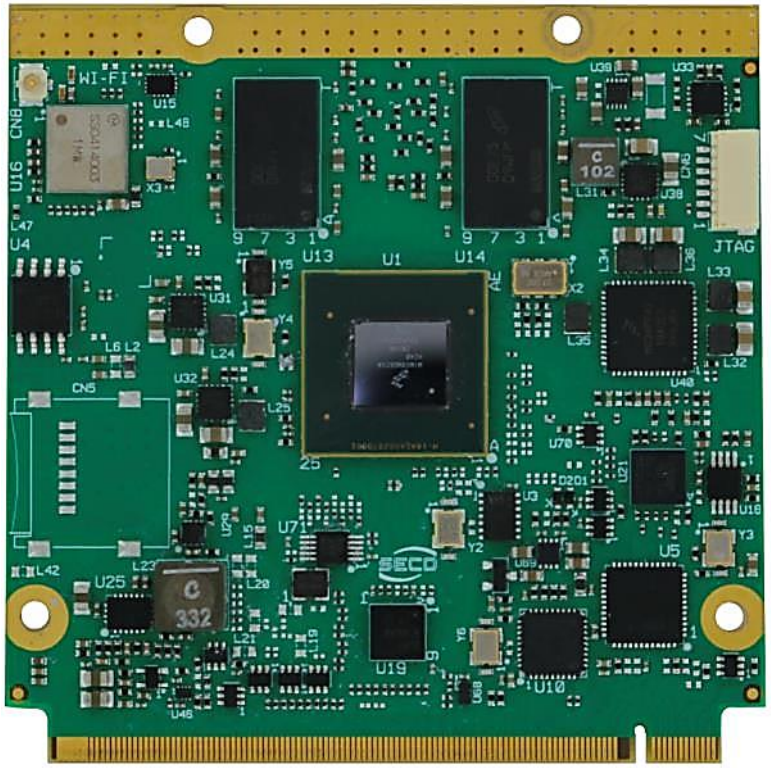
Qseven

User Manual



Q7-C25

Qseven® Rel. 2.1 Compliant Module
with NXP i.MX 8M Applications Processors

SECO

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REVISION HISTORY

Revision	Date	Note	Rif
1.0	18th August 2020	First Release	AR
1.1	19th May 2021	- Updated pictures to latest module revision - Added Safety Policy par. 1.7 - Pull-up resistor value on GbE LED signals updated (par. 3.2.6) - Minor corrections	AR
1.2	8th October 2021	- Updated USB OTG functionality info (par.3.2.7)	AR

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

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Chapter 1. INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications

1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/us/support/online-rma.html (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210
- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The Q7-C25 module uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!**
>
> Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.
>
> Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The Q7-C25 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!**
>
> Whenever handling a SM-B69 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The Q7-C25 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Policy

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, the Q7-C25 Module shall be:

- used inside a fire enclosure made of non-combustible material or V-1 material (the fire enclosure is not necessary if the maximum power supplied to the module never exceeds 100 W, even in worst-case fault);
- used inside an enclosure; the enclosure is not necessary if the temperature of the parts likely to be touched never exceeds 70 °C;
- installed inside an enclosure compliant with all applicable IEC 62368-1 requirements;

The manufacturer which includes a Q7-C25 module in his end-user product shall:

- verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition
- Prescribe temperature and humidity range for operating, transport and storage conditions;
- Prescribe to perform maintenance on the module only when it is off and has already cooled down;
- Prescribe that the connections from or to the Module have to be compliant to ES1 requirements;
- The module in its enclosure must be evaluated for temperature and airflow considerations.

1.8 Terminology and definitions

API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
CSI2	MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host processor
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
DVI	Digital Visual interface, a type of display video interface
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
LPDDR4	Low-Power Double Data Rate Synchronous Dynamic Random Access Memory, 4th generation
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port.
PCI-e	Peripheral Component Interface Express

PWM	Pulse Width Modulation
PWR	Power
RGMII	Reduced Gigabit Reduced Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer (PHY)
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
USB	Universal Serial Bus
uSDHC	Ultra Secure Digital Host Controller

1.9 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
CSI	http://www.mipi.org/specifications/camera-interface
DDC, DP, eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
NXP i.MX 8M processor	https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-8-processors/i.mx-8m-family-armcortex-a53-cortex-m4-audio-voice-video:i.MX8M
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
Qseven® Design Guide	https://sget.org/wp-content/uploads/2018/09/Qseven_Design_Guide_2_0.pdf
Qseven® specifications	https://sget.org/wp-content/uploads/2018/09/Qseven-Spec_2.1.pdf
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram

2.1 Introduction

The Q7-C25 is a Q7 Rel. 2.1 compliant module with NXP i.MX 8M Applications Processors. Featuring multicore processing (Dual or Quad ARM Cortex®-A53 cores + general purpose Cortex®-M4 processor) and 4Kp60 HEVC decoding with HDR, it is a scalable solution designed by SECO for home automation, transportation, digital signage and vending machines, and applicable to scenarios requiring advanced security, connectivity, multimedia and real-time response.

The module offers a very high level of integration, both for all most common used peripherals in the ARM domain and for bus interfaces typically used in the x86 domain, like PCI-Express.

Presented in the Q7 form factor, offering the computing abilities of a standard board, with the possibilities of combining with a ready-to-use carrier board like the SECO CQ7-A42 or customised carrier board.

For external interfacing to standard devices, a carrier board with a 230-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as the integration of other peripherals/devices not already included in Q7-C25 module.

2.2 Technical Specifications

Processors

NXP i.MX 8M Family based on ARM Cortex®-A53 cores + general purpose Cortex®-M4 processor:

- i.MX 8M Quad - 4x Cortex®-A53 cores up to 1.5GHz
- i.MX 8M Dual - 2x Cortex®-A53 cores up to 1.5GHz
- i.MX 8M QuadLite - 4x Cortex®-A53 cores up to 1.5GHz, no VPU

Memory

Soldered Down DDR4-2400 memory, 32-bit interface, up to 4GB

Graphics

Integrated Graphics Processing Unit, supports 2 independent displays.
Embedded VPU (not available on QuadLite), supports H/W decoding of HEVC, H.264, H.263, MPEG-4, MPEG-2, AVC, VC-1, RV, DivX, VP6, VP8, VP9, JPEG
Supports OpenGL ES 3.1, Open CL 1.2, OpenGL 2.X, Vulkan, DirectX, Open VG 1.1

Video Interfaces

1 x HDMI 2.0a / Display Port 1.3 interface, supporting HDCP 2.2 and HDCP 1.4
1 x LVDS 18/24-bit Dual Channel or 1 x eDP interface (factory alternatives)

Video Resolution

HDMI, resolution up to 4096x2160 @ 60Hz
MIPI-DSI, LVDS, resolution up to 1920x1080 @ 60Hz

Mass Storage

eMMC 5.0 Drive soldered on-board, up to 64GB
Optional microSD slot on board
8MB QuadSPI Flash soldered-onboard

PCI Express

Up to 2 x PCI-e x1 Gen2 ports

Networking

1 x Gigabit Ethernet interface
Optional WiFi + BT LE module onboard

USB

1 x USB 3.0 Host or Client Port
Up to 4 x USB 2.0 Host Ports

Audio

I2S Audio interface

Serial ports

1x UART Tx/Rx/RTS/CTS (Optional)
1x Debug UART
1x CAN Bus (TTL level)

Other Interfaces

I2C Bus
SM Bus
Optional SPI interface
8 x GPI/Os
UltraLow Power RTC
Power Management Signals
Watchdog

Power supply voltage: +5V_{DC} ±5% and +5V_{SB} (optional)

RTC voltage: 3.3V

Operating temperature:

Commercial version 0°C ÷ +60°C **.
Industrial version -40°C ÷ +85°C **.

Dimensions: 70 x 70 mm (2.76" x 2.76")

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated.*
Please also check paragraph 4.1

2.3 Electrical Specifications

According to Qseven® specifications, Q7-C25 board needs to be supplied only with an external +5V_{DC} power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from +5V_RUN power rail.

2.3.1 Power Consumption

Q7-C25 module, like all Qseven modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Anyway, it has been possible to measure power consumption directly on VCC power rail (5V_{DC})that supplies the board.

The power consumption has been measured in a Q7-C25 module with the following configuration on the commercial version:

- CPU iMX8M Quad 1.5GHz
- RAM DDR4 4GB, eMMC 8 GB
- LVDS + HDMI/DP video outputs

Status	Average value	Peak Value
Idle	4W, 0.78A	/
Video 1080p 60fps	4.43W, 0.87A	/
GPU working at full load, video output on HDMI	5.7W, 1.12A	/
Video 1080p 60fps ,GPU working at full load, CPU 100%	6.9W, 1.35A	7.7W, 1.5A
RTC Power consumption on VDD_RTC (when VDD_IN off)	230nA	

Please consider that power consumption is strongly dependent on the board's configuration, on number of processor cores active and from the interfaces that are SW enabled.

2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VCC: Power Supply +5VDC ±5%

VCC_5V_SB: Standby Power Supply +5VDC ±5%

VCC_RTC: 3V backup cell input. VCC_RTC is connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

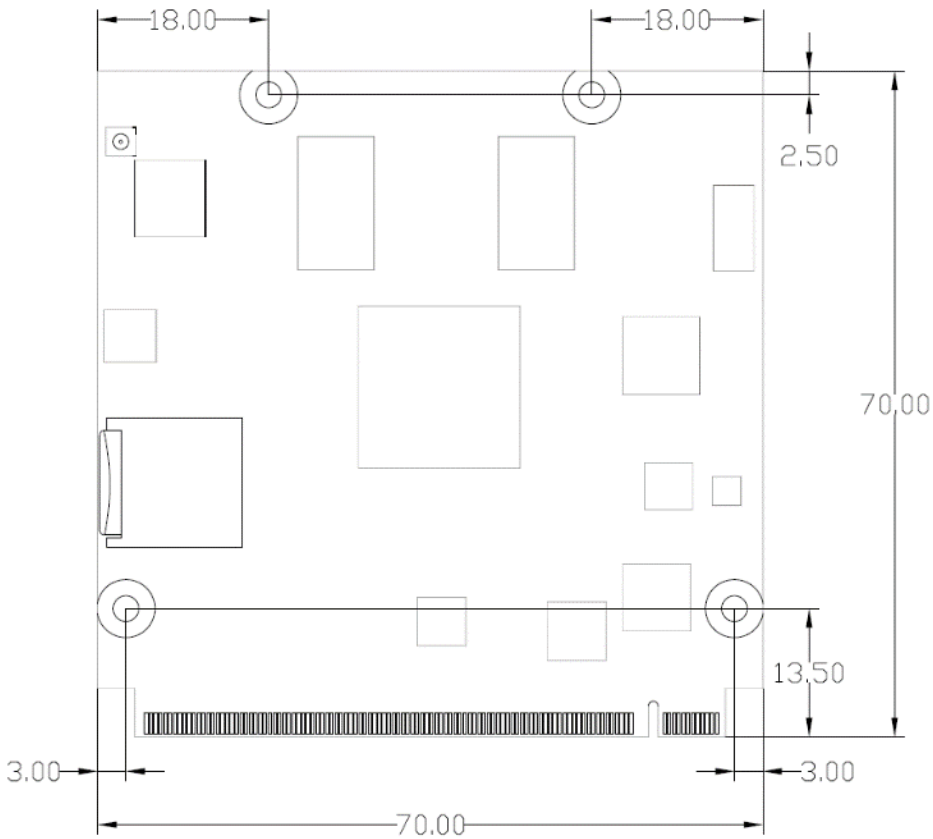
2.4 Mechanical Specifications

According to Qseven® specifications, board dimensions are: 70 x 70 mm (2.76” x 2.76”).

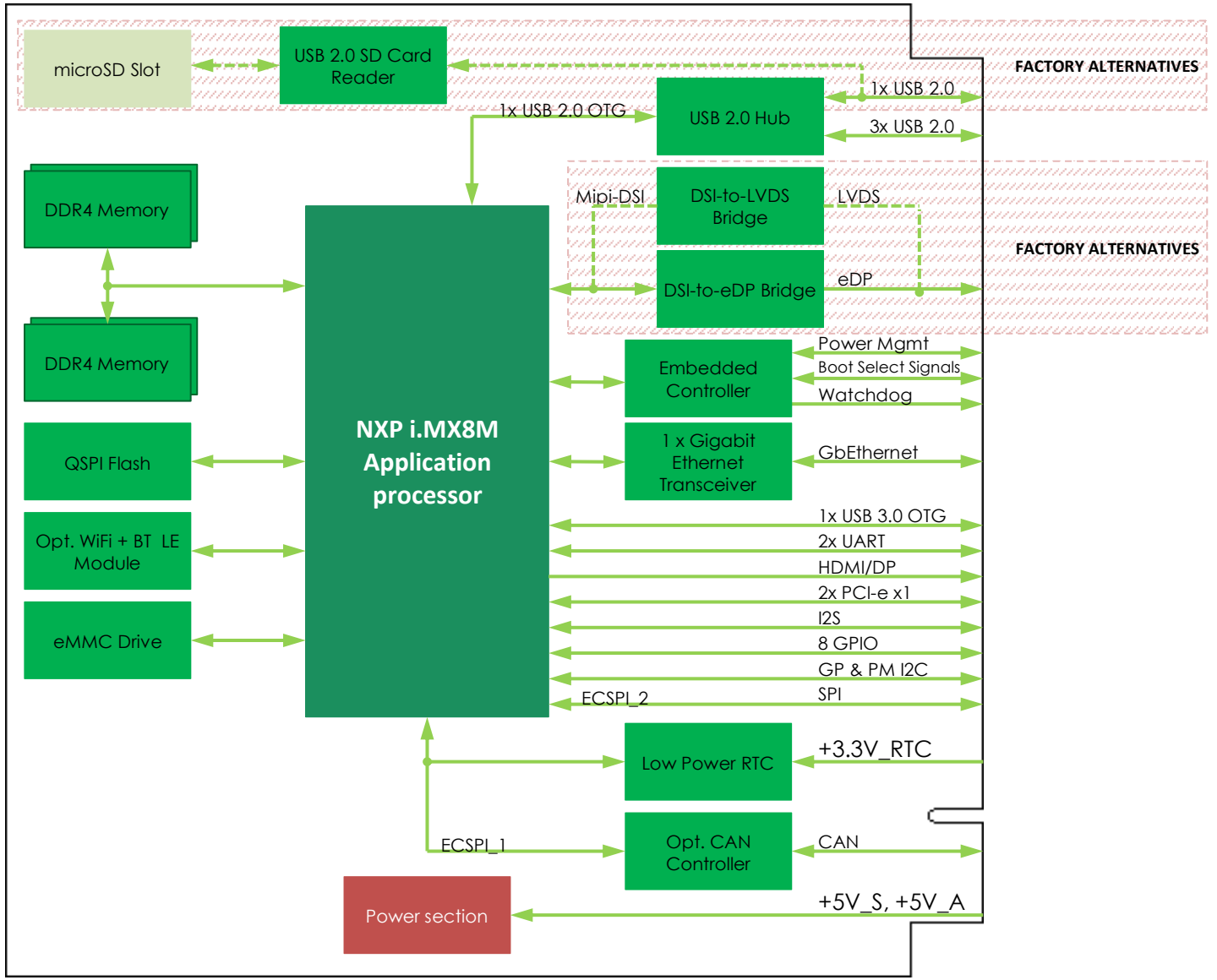
Printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs. Qseven® specification suggests two connector heights, 7.8mm and 7.5mm, but it is also possible to use different connector heights, also remaining compliant to the standard.

When using different connector heights, please consider that, according to Qseven® specifications, components placed on bottom side of Q7-C25 will have a maximum height of 2.2mm ± 0.1. Keep this value in mind when choosing the MXM connector’s height, if it is needed to place components on the carrier board in the zone below the Qseven® module.



2.5 Block Diagram



Chapter 3. CONNECTORS

- Introduction
- Connectors description

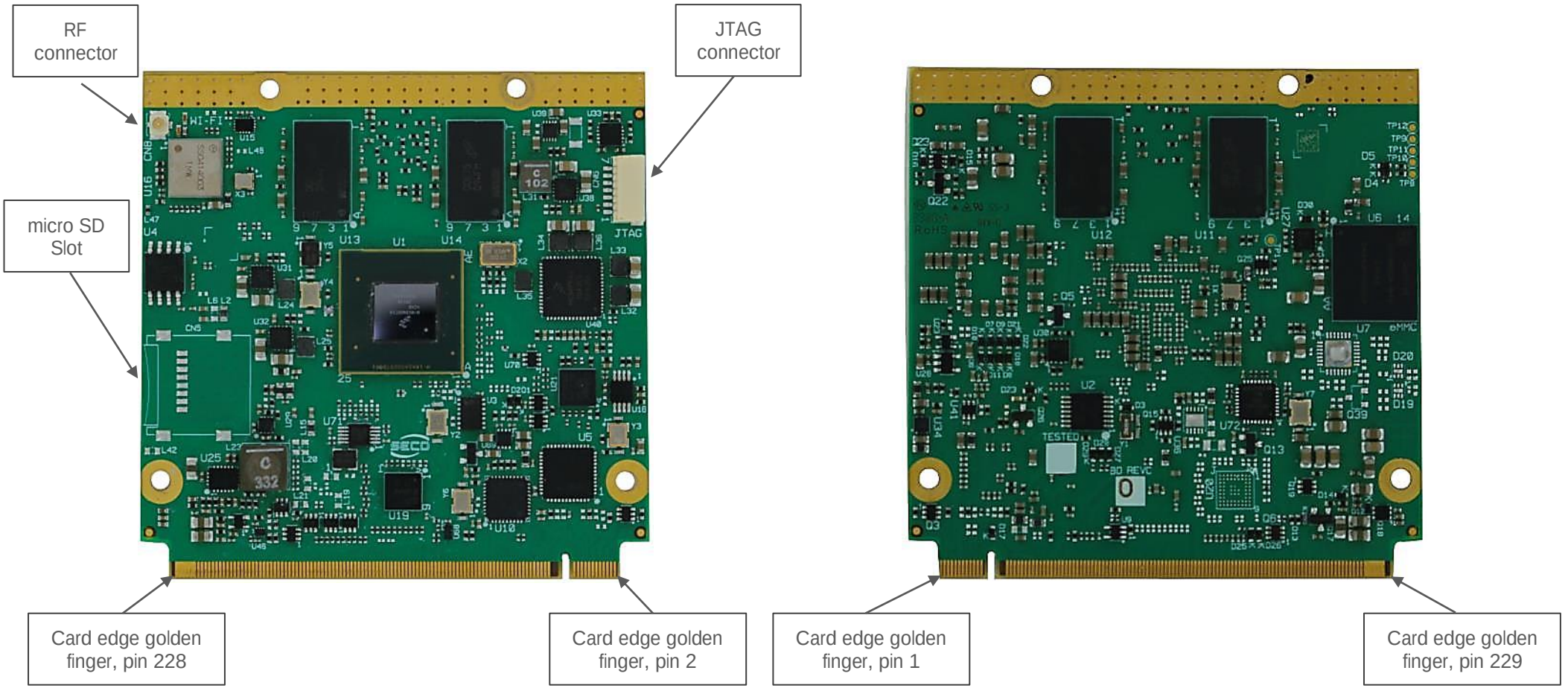
3.1 Introduction

According to Qseven® specifications, all interfaces to the board are available through a single card edge connector.

Moreover, an additional RF connector for antenna on Wifi module, a JTAG connector and micro SD slot have been placed.

TOP SIDE

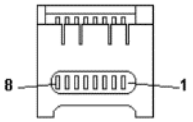
BOTTOM SIDE



3.2 Connectors description

3.2.1 µSD Card Slot

NXP i.MX8M processors offer many different SDIO interfaces, that can be used independently one from the other to implement different mass storages media (internal eMMC, internal SD Card, external SDI/O interface).



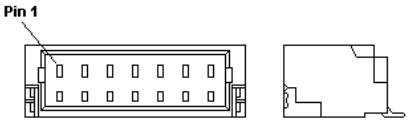
The µSD card slot CN5, type TOWNES p/n TKS0192003, on this module is soldered on top side of the module and realized through Alcor Micro AU6465R for data transmission between USB and card interface. In this case, USBP4 host port 2.0 is not available as an external interface on Q7 card edge connector.

> **!** Please be aware that the µSD card slot is a flip-top type: this means that, in order to insert / extract / change a µSD card, the heatsink/heatspreader must not be mounted, otherwise it will be impossible to access/open the flip top slot.

3.2.2 JTAG connector

JTAG Connector- CN6	
1	+3.3V_ALW
2	JTAG_TCK
3	JTAG_TMS
4	JTAG_TDI
5	JTAG_TDO
6	JTAG_TRST_B
7	GND

NXP i.MX8M processors have a system JTAG Controller (SJC) and support two JTAG modes, debug mode and test mode. This interface is accessible through connector CN6, type JST p/n SM07B-SRSS-TB with the following pinout. Please refer to NXP i.MX8M development reference manual for correct implementation.



Mating connector: JST SHR-07V-S or SHR-07V-S-B receptacle with JST SSH-003T-P0.2H female crimp terminals.

All these signals are at electrical level +3.3_ALW, please refer to NXP i.MX 8M development reference manual for correct implementation.

3.2.3 Qseven® Connector

According to Qseven® specifications, all interface signals are reported on the card edge connector, which is a 230-pin Card Edge that can be inserted into standard 230 pin MXM connectors, as described in Qseven® specifications.

Not all signals contemplated in Qseven® standard are implemented on MXM connector, due to the functionalities really implemented on Q7-C25 CPU module. Therefore, please refer to the following table for a list of effective signals reported on MXM connector.

For accurate signals description, please consult the following paragraphs.

NOTE: Even pins are available on top side of CPU board; odd pins are available on bottom side of CPU board. Please refer to board photos.

Qseven® Golden Finger Connector - CN4

BOTTOM SIDE				TOP SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	1	2	GND	PWR	
GBE	I/O	GBE_MDI3-	3	4	GBE_MDI2-	I/O	GBE
GBE	I/O	GBE_MDI3+	5	6	GBE_MDI2+	I/O	GBE
GBE	O	GBE_LINK100#	7	8	GBE_LINK1000#	O	GBE
GBE	I/O	GBE_MDI1-	9	10	GBE_MDI0-	I/O	GBE
GBE	I/O	GBE_MDI1+	11	12	GBE_MDI0+	I/O	GBE
GBE	O	GBE_LINK#	13	14	GBE_ACT#	O	GBE
GBE	O	GBE_CTREF	15	16	SUS_S5#	O	PWR_MGMT
PWR_MGMT	I	WAKE#	17	18	SUS_S3#	O	PWR_MGMT
PWR_MGMT	O	GPO0	19	20	PWRBTN#	I	PWR_MGMT
PWR_MGMT	I	SLP_BTN#	21	22	LID_BTN#	I	PWR_MGMT
	PWR	GND	23	24	GND	PWR	
	PWR	GND	25	26	PWGIN	I	PWR_MGMT
PWR_MGMT	I	BATLOW#	27	28	RSTBTN#	I	PWR_MGMT
	N.A.	N.C.	29	30	N.C.	N.A.	
	N.A.	N.C.	31	32	N.C.	N.A.	
	N.A.	N.C.	33	34	GND	PWR	
	N.A.	N.C.	35	36	N.C.	N.A.	

	N.A.	N.C.	37	38	N.C.	N.A.	
	PWR	GND	39	40	GND	PWR	
BOOT SELECT	I	BOOT_ALT#	41	42	N.C.	N.A.	
	N.A.	N.C.		44	N.C.	N.A.	
	N.A.	N.C.		46	N.C.	N.A.	
	N.A.	N.C.		48	N.C.	N.A.	
	N.A.	N.C.		50	N.C.	N.A.	
	N.A.	N.C.		52	RESERVED	O	UART_TX
UART_CTS	I	RESERVED	53	54	RESERVED	I	UART_RX
UART_RTS	O	RESERVED	55	56	USB_OTG_PEN	O	USB
	PWR	GND	57	58	GND	PWR	
AUDIO	O	I2S_WS	59	60	SMB_CLK	I/O	MISC
AUDIO	O	I2S_RST#	61	62	SMB_DAT	I/O	MISC
AUDIO	O	I2S_CLK	63	64	SMB_ALERT#	I/O	MISC
AUDIO	I	I2S_SDI	65	66	GP0_I2C_CLK	I/O	MISC
AUDIO	O	I2S_SDO	67	68	GP0_I2C_DAT	I/O	MISC
MISC	I	THRM#	69	70	WDTRIG#	I	MISC
MISC	O	THRMTRIP#	71	72	WDOUT	O	MISC
	PWR	GND	73	74	GND	PWR	
	N.A.	N.C.	75	76	N.C.	N.A.	
	N.A.	N.C.	77	78	N.C.	N.A.	
	N.A.	N.C.	79	80	USB_4_5_OC#	I	USB
	N.A.	N.C.	81	82	USBP4-	I/O	USB
	N.A.	N.C.	83	84	USBP4+	I/O	USB
USB	I	USB_2_3_OC#	85	86	USB_0_1_OC#	I	USB
USB	I/O	USBP3-	87	88	USBP2-	I/O	USB
USB	I/O	USBP3+	89	90	USBP2+	I/O	USB
USB	I	USB_VBUS	91	92	USB_ID	O	USB
USB	I/O	USBP1-	93	94	USBP0-	I/O	USB
USB	I/O	USBP1+	95	96	USBP0+	I/O	USB

	PWR	GND	97	98	GND	PWR	
LVDS/eDP	O	LVDS_A0+ / eDP0_TX0+	99	100	LVDS_B0+ / eDP1_TX0+	O	LVDS/eDP
LVDS/eDP	O	LVDS_A0- / eDP0_TX0-	101	102	LVDS_B0- / eDP1_TX0-	O	LVDS/eDP
LVDS/eDP	O	LVDS_A1+ / eDP0_TX1+	103	104	LVDS_B1+ / eDP1_TX1+	O	LVDS/eDP
LVDS/eDP	O	LVDS_A1- / eDP0_TX1-	105	106	LVDS_B1- / eDP1_TX1-	O	LVDS/eDP
LVDS/eDP	O	LVDS_A2+ / eDP0_TX2+	107	108	LVDS_B2+ / eDP1_TX2+	O	LVDS/eDP
LVDS/eDP	O	LVDS_A2- / eDP0_TX2-	109	110	LVDS_B2- / eDP1_TX2-	O	LVDS/eDP
LVDS/eDP	O	LVDS_PPEN	111	112	LVDS_BLEN	O	LVDS/eDP
LVDS/eDP	O	LVDS_A3+ / eDP0_TX3+	113	114	LVDS_B3+ / eDP1_TX3+	O	LVDS/eDP
LVDS/eDP	O	LVDS_A3- / eDP0_TX3-	115	116	LVDS_B3- / eDP1_TX3-	O	LVDS/eDP
	PWR	GND	117	118	GND	PWR	
LVDS	O	LVDS_A_CLK+ / eDP0_AUX+	119	120	LVDS_B_CLK+ / eDP1_AUX+	O	LVDS/eDP
LVDS	O	LVDS_A_CLK- / eDP0_AUX-	121	122	LVDS_B_CLK- / eDP1_AUX-	O	LVDS/eDP
LVDS/eDP	O	LVDS_BLT_CTRL	123	124	HDMI_CEC	I/O	HDMI
LVDS	O	LVDS_DID_DAT	125	126	N.C.	N.A.	
LVDS	O	LVDS_DID_CLK	127	128	N.C.	N.A.	
CAN	O	CAN0_TX	129	130	CAN0_RX	I	CAN
HDMI/DP	O	TMDS_CLK+ / DP_LANE3+	131	132	USB_SSTX1-	O	USB
HDMI/DP	O	TMDS_CLK- / DP_LANE3-	133	134	USB_SSTX1+	O	USB
	PWR	GND	135	136	GND	PWR	
HDMI/DP	O	TMDS_LANE1+ / DP_LANE1+	137	138	DP_AUX+	I/O	DP
HDMI/DP	O	TMDS_LANE1- / DP_LANE1-	139	140	DP_AUX-	I/O	DP
	PWR	GND	141	142	GND	PWR	
HDMI/DP	O	TMDS_LANE0+ / DP_LANE2+	143	144	USB_SSRX1-	I	USB
HDMI/DP	O	TMDS_LANE0- / DP_LANE2-	145	146	USB_SSRX1+	I	USB
	PWR	GND	147	148	GND	PWR	
HDMI/DP	O	TMDS_LANE2+ / DP_LANE0+	149	150	HDMI_CTRL_DAT	I/O	HDMI
HDMI/DP	O	TMDS_LANE2- / DP_LANE0-	151	152	HDMI_CTRL_CLK	I/O	HDMI
HDMI/DP	I	HDMI_HPD#	153	154	DP_HPD#	I	DP
PCI-E	O	PCIE_CLK_REF+	155	156	PCIE_WAKE#	I	PCI-E

PCI-E	O	PCIE_CLK_REF-	157	158	PCIE_RST#	O	PCI-E
	PWR	GND	159	160	GND	PWR	
	N.A.	N.C.	161	162	N.C.	N.A.	
	N.A.	N.C.	163	164	N.C.	N.A.	
	PWR	GND	165	166	GND	PWR	
	N.A.	N.C.	167	168	N.C.	N.A.	
	N.A.	N.C.	169	170	N.C.	N.A.	
UART	O	UART0_TX	171	172	UART0_RTS#	O	UART
PCI-E	O	PCIE1_TX+	173	174	PCIE1_RX+	I	PCI-E
PCI-E	O	PCIE1_TX-	175	176	PCIE1_RX-	I	PCI-E
UART	I	UART0_RX	177	178	UART0_CTS#	I	UART
PCI-E	O	PCIE0_TX+	179	180	PCIE0_RX+	I	PCI-E
PCI-E	O	PCIE0_TX-	181	182	PCIE0_RX-	I	PCI-E
	PWR	GND	183	184	GND	PWR	
GPIO	I/O	LPC_AD0/GPIO0	185	186	LPC_AD1/GPIO1	I/O	GPIO
GPIO	I/O	LPC_AD2/GPIO2	187	188	LPC_AD3/GPIO3	I/O	GPIO
GPIO	I/O	LPC_CLK/GPIO4	189	190	LPC_FRAME#/GPIO5	I/O	GPIO
GPIO	I/O	SERIRQ/GPIO6	191	192	LPC_LDRQ#/GPIO7	I/O	GPIO
	PWR	VCC_RTC (+3.3V_A)	193	194	SPKR	O	MISC
MISC	I	FAN_TACHOIN	195	196	FAN_PWMOUT	O	MISC
	PWR	GND	197	198	GND	PWR	
SPI	O	SPI_MOSI	199	200	SPI_CS0#	O	SPI
SPI	I	SPI_MISO	201	202	SPI_CS1#	O	SPI
SPI	O	SPI_SCK	203	204	MFG_NC4	N.A.	MFG
	PWR	VCC_5V_SB	205	206	VCC_5V_SB	PWR	
MFG	N.A.	MFG_NC0	207	208	MFG_NC2	N.A.	MFG
MFG	N.A.	MFG_NC1	209	210	MFG_NC3	N.A.	MFG
	N.A.	N.C.		212	\	N.A.	
	N.A.	N.C.		214	N.C.	N.A.	
	N.A.	N.C.		216	N.C.	N.A.	

N.A.	N.C.		218	N.C.	N.A.
PWR	VCC	219	220	VCC	PWR
PWR	VCC	221	222	VCC	PWR
PWR	VCC	223	224	VCC	PWR
PWR	VCC	225	226	VCC	PWR
PWR	VCC	227	228	VCC	PWR
PWR	VCC	229	230	VCC	PWR

3.2.4 PCI Express interface signals

The Q7-C25 module can offer two PCI Express x1 lanes, which are directly managed by i.MX8M processor (all versions).

PCI express Gen 2.0 (5Gbps) is supported.

Here following the signals involved in PCI express management

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair

PCIE1_RX+/PCIE1_RX-: PCI Express lane #1, Receiving Input Differential pair

PCIE1_TX+/PCIE1_TX-: PCI Express lane #1, Transmitting Output Differential pair

PCIE_CLK_REF+/PCIE_CLK_REF-: PCI Express Reference Clock, Differential Pair

PCIE_RST#: Reset Signal that is sent from Qseven® Module to any PCI-e device available on the carrier board. It is a +3.3V_RUN active-low signal; it can be used directly to drive externally a single RESET Signal. In case there is the need to supply Reset signal to multiple devices, it is recommended to provide for a buffer on the carrier board.

PCIE_WAKE#: Wake up Signal that is asserted from any PCI-e device available on the carrier board to Qseven® Module. It is a 3V3_ALW active-low signal with a 10kΩ pull-up resistor. Controlled by a STM32 MCU soldered onboard the Q7 module.

3.2.5 UART interface signals

According to Qseven® Rel. 2.1 specifications, Q7-C25 offers one UART interface, directly managed by i.MX8M processor (all versions). This interface is optional, and is available when UART is not used for WiFi + BT module. Please be sure of factory configuration for the module ordered.

Here following the signals related to UART interface:

UART0_TX: UART Interface, Serial data Transmit (output) line, +3.3V_RUN electrical level.

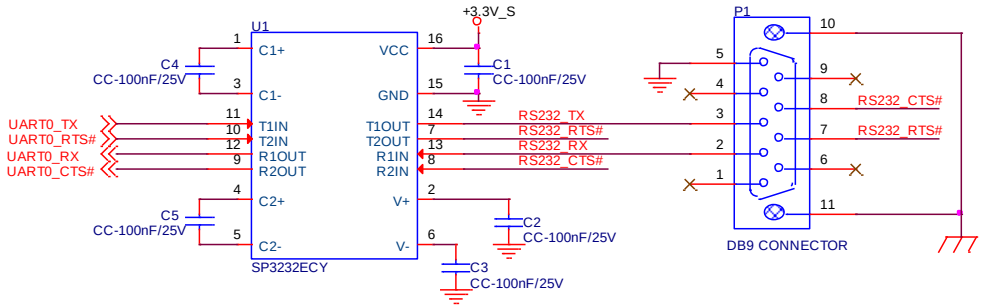
UART0_RX: UART Interface, Serial data Receive (input) line, +3.3V_RUN electrical level.

UART0_RTS#: UART Interface, Handshake signal, Request to Send (output) line, +3.3V_RUN electrical level.

UART0_CTS#: UART Interface, Handshake signal, Clear to Send (Input) line, +3.3V_RUN electrical level.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it isn't needed explicitly to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The following schematic shows an example of implementation of RS-232 transceiver for the Carrier board



All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.p.A for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

Based on Qseven® Rel. 2.1 specifications, this module offers one UART interface. This interface and another internal UART can be used by i.XM8M processors for different scopes, depending on the factory configuration when ordering the module. This table below summarizes all the possible uses.

Configuration	UART2	UART4
QC25-XXXX-XXX1-X1	Q7_UART0	Q7_SPI
QC25-XXXX-XXX3-X1	WiFi + BT	Q7_SPI
QC25-XXXX-XXX4-X1	Q7_UART0	WiFi + BT

3.2.6 Gigabit Ethernet signals

The Gigabit Ethernet interface is realised, on Q7-C25 module by using a Texas Instruments DP83867CRRGZR Gigabit Ethernet transceiver, which is interfaced to NXP i.MX 8M processor through an RGMII interface.

Here following the signals involved in PCI express management

GBE_MDI0+/GBE_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE_MDI1+/GBE_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE_MDI2+/GBE_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

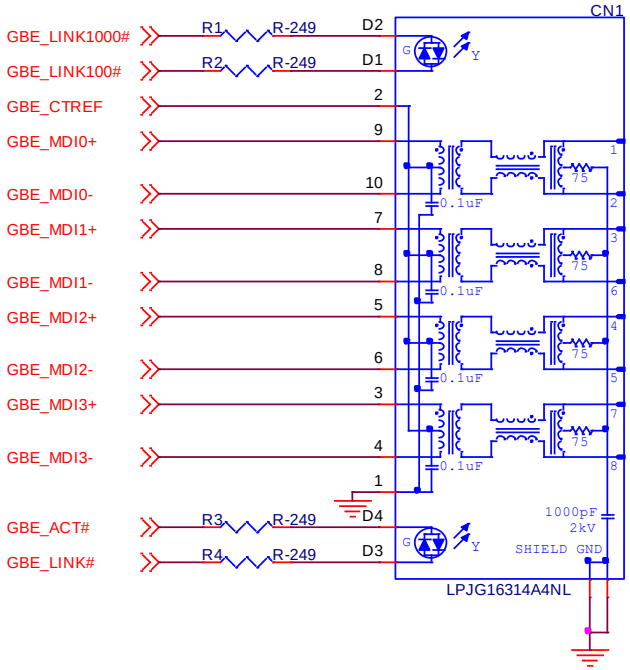
GBE_MDI3+/GBE_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE_ACT#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_RUN with 240Ω pull-up resistor

GBE_LINK#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_RUN with 240Ω pull-up resistor

GBE_LINK100#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_RUN with 240Ω pull-up resistor

GBE_LINK1000#: Ethernet controller 1Gbps link indicator, Active Low Output signal, electrical level +3.3V_RUN with 240Ω pull-up resistor



These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected. Please look to the schematic above as an example of implementation of Gigabit Ethernet connector. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. DP83867 PHY, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on Qseven® golden finger connector

3.2.7 USB interface signals

The module has up to 5x USB ports consisting of 1x USB 3.0 Host or Client programmable port from the NXP i.MX 8M processor USB controller, and 4x USB 2.0 host ports coming from a Microchip USB 2514B-AEZC USB 2.0 hub controller.

Here following the signals related to USB interfaces.

USBP0+/USBP0-: Universal Serial Bus Downstream Port #1 differential pair (coming out from USB 2.0 hub controller).

USBP1+/USBP1-: Universal Serial Bus Port #1 differential pair (coming out from NXP i.MX 8M processor USB 2.0 controller).

USBP2+/USBP2-: Universal Serial Bus Downstream Port #2 differential pair (coming out from USB 2.0 hub controller).

USBP3+/USBP3-: Universal Serial Bus Downstream Port #3 differential pair (coming out from USB 2.0 hub controller).

USBP4+/USBP4-: Universal Serial Bus Downstream Port #4 differential pair (coming out from USB 2.0 hub controller).

USB_SSRX1+/ USB_SSRX1-: USB Super Speed Port #1 receive differential pair (coming out from NXP i.MX 8M processor USB 3.0 controller).

USB_SSTX1+/ USB_SSTX1-: USB Super Speed Port #1 transmit differential pair (coming out from NXP i.MX 8M processor USB 3.0 controller).

USB_0_1_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin is used to monitor the USB power over current of the USB Ports 0 and 1 of Q7-C25 module.

USB_2_3_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin is used to monitor the USB power over current of the USB Ports 2 and 3 of Q7-C25 module.

USB_4_5_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin is used to monitor the USB power over current of the USB Ports 4 of Q7-C25 module.

USB_ID: USB ID Input This signal must be driven as an open collector signal by external circuitry placed on the carrier board. It must be tied to GND when USB Port #1 has to be set to work in Host mode. When not driven, USB Port#1 will work in Client mode.

USB_VBUS: USB Client Connect Pin, electrical level +5V_ALW. When USB Port #1 is set to work in Client mode, then this signal shall be used to inform the USB controller when an external USB Host is connected (signal High) or disconnected (Signal Low)

USB_OTG_PEN: USB Power enable pin for USB Port 1, electrical level +3.3V_RUN. This pin Enables the Power for the USB-OTG port on the carrier board.

Please notice that for correct management of overcurrent signals, power distribution switches are needed on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

The two USB Controllers embedded in the i.MX 8M processor offer both the OTG functionality, but USB 3.0 Controller #2 is used to manage the USB 2.0 Hub. Therefore, only USB Controller #1 can be used to implement OTG functionality, which, according to Qseven specifications, shall be mapped on USB port #1. This implies that also the superspeed signals must be mapped on port #1, leaving unconnected the superspeed signal related to port #0 (which works only in USB 2.0 mode).

Please take note that USB Port #1 with its Superspeed Signals can be set to work in host mode or client mode only during BSP compiling.

3.2.8 Audio interface signals

Q7-C25 module supports I2S audio format, thanks to native support offered by the processor to this audio codec standard.

Here following the signals related to AC'97/I2S Audio interface:

I2S_WS: I2S Word Select Signal. Output from the module to the Carrier board, electrical level +3.3V_RUN.

I2S_RST#: I2S Codec Reset. Active Low signal Output from the module to the Carrier board, electrical level +3.3V_RUN.

I2S_CLK: I2S Serial Data Clock signal. Output from the module to the Carrier board, electrical level +3.3V_RUN.

I2S_SDO: I2S Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_RUN.

I2S_SDI: I2S Serial Data In signal. Input to the module from the Carrier board, electrical level +3.3V_RUN.

All these signals have to be connected, on the Carrier Board, to an I2S Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.9 LVDS and eDP Flat Panel signals

All processors included in i.MX8M family provide a four-lane MIPI display serial interface operating up to a maximum bit rate of 1.5 Gbps. The MIPI-DSI is used to implement a 18/24 bit Dual Channel LVDS or, as a factory alternative, an eDP interface

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for primary channel are LVDS:

LVDS_A0+ / LVDS_A0- : LVDS Channel #A differential data pair #0
LVDS_A1+/ LVDS_A1-: LVDS Channel #A differential data pair #1
LVDS_A2+/LVDS_A2-: LVDS Channel #A differential data pair #2
LVDS_A3+/ LVDS_A3-: LVDS Channel #A differential data pair #3
LVDS_A_CLK+ / LVDS_A_CLK-: LVDS Channel #A differential Clock

OR the signals for primary channel are eDP:

eDP0_TX0+/ eDP0_TX0-: embedded DisplayPort Channel #0 differential data pair #0
eDP0_TX1+/ eDP0_TX1-: embedded DisplayPort Channel #0 differential data pair #1
eDP0_TX2+/ eDP0_TX2-: embedded DisplayPort Channel #0 differential data pair #2
eDP0_TX3+/ eDP0_TX3-: embedded DisplayPort Channel #0 differential data pair #3
eDP0_AUX+/ eDP0_AUX-: embedded DisplayPort Channel #0 auxiliary channel

The signals for secondary channel are LVDS:

LVDS_B0+ / LVDS_B0- : LVDS Channel #B differential data pair #0

LVDS_B1+/ LVDS_B1-: LVDS Channel #B differential data pair #1

LVDS_B2+/LVDS_B2-: LVDS Channel #B differential data pair #2

LVDS_B3+/ LVDS_B3-: LVDS Channel #B differential data pair #3

LVDS_B_CLK+ / LVDS_B_CLK-: LVDS Channel #B differential Clock

In addition, the following control signals are present:

LVDS_PPEN: +3.3V_RUN electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected display.

LVDS_BLEN: +3.3V_RUN electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected display.

LVDS_BLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

LVDS_DID_DAT: LCD I2C Data. This signal is used to read the LCD display EDID EEPROM. +3.3V_RUN electrical level Bidirectional

LVDS_DID_CLK: LCD I2C Clock: This signal is used to read the LCD display EDID EEPROM. +3.3V_RUN electrical level Output

The module has a Texas Instruments SN65DSI84 DSI to FlatLink™ compatible LVDS output bridge, connected from one channel of the four-lane MIPI-DSI of the processor to the LVDS Channel #A and #B interfaces of the edge connector.

As a factory alternative, the module has a Texas Instrument SN65DSI86 MIPI® DSI to eDP™ bridge, connected from one channel of the four-lane MIPI display serial interface to eDP0 interface of the edge connector.

3.2.10 HDMI interface signals

The NXP i.MX 8M processor has an HD Display Transmitter Controller (HDMI TX), which offers multi-protocol support of standards such as HDMI, DisplayPort, eDP, with one of these standards supported at a time. In case HDMI is selected, it provides an HDMI standard interface for HDMI 2.0a compliant displays. Supports HDCP 2.2 and HDCP 1.4

The signals are:

TMDS_LANE0+ / TMDS_LANE0-: HDMI Output Differential Pair #0

TMDS_ALNE1+ / TMDS_LANE1-: HDMI Output Differential Pair #1

TMDS_LANE2+ / TMDS_LANE2-: HDMI Output Differential Pair #2

TMDS_CLK+ / TMDS_CLK-: HDMI Differential Clock

HDMI_HPD#: Hot Plug Detect Input signal. +3.3V_RUN electrical level with a 10kΩ pull-up resistor

HDMI_CEC: Consumer Electronics Control. Bidirectional signal, +3.3V_RUN electrical level with a 2.2kΩ pull-up resistor

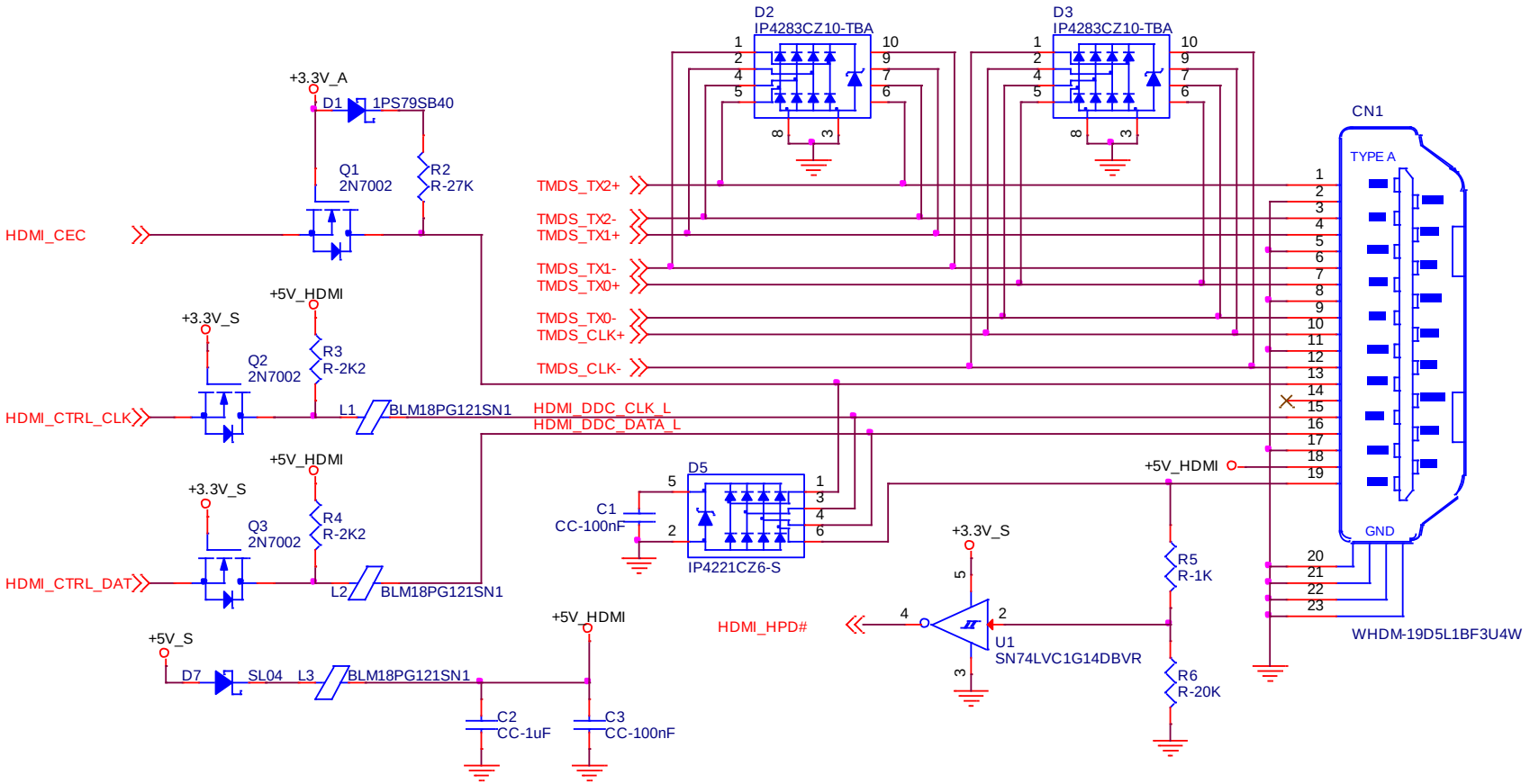
HDMI_CTRL_CLK: DDC Clock line for HDMI panel. Bidirectional signal, +3.3V_RUN electrical level with a 1.5kΩ pull-up resistor

HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, +3.3V_RUN electrical level with a 1.5kΩ pull-up resistor

Since HDMI Tx module is embedded in the i.MX 8M processors, it is not necessary to implement voltage level shifter for TMDS differential pairs on the Carrier board. It is still necessary, however, to implement voltage level shifters on Control data/Clock signals, as well as for Hot Plug Detect signal.

Voltage clamping diodes are also highly recommended on all signal lines for ESD suppression.

Please refer to the following schematics as an example of implementation of HDMI connection + voltage level shifters on the carrier board.



3.2.11 DP interface signals

As said previously, the NXP i.MX 8M processor has an HD Display Transmitter Controller (HDMI TX), which offers multi-protocol support of standards, such as Display Port 1.3 interface. Therefore, the TMDS interface signals are shared with the signals for the DisplayPort interface.

If the board purchased is in DP configuration, then the following signals will be available on Qseven® golden finger connector:

DP_LANE3+/DP_LANE3-: Display Port differential pair #3.

DP_LANE2+/DP_LANE2-: Display Port differential pair #2.

DP_LANE1+/DP_LANE1-: Display Port differential pair #1

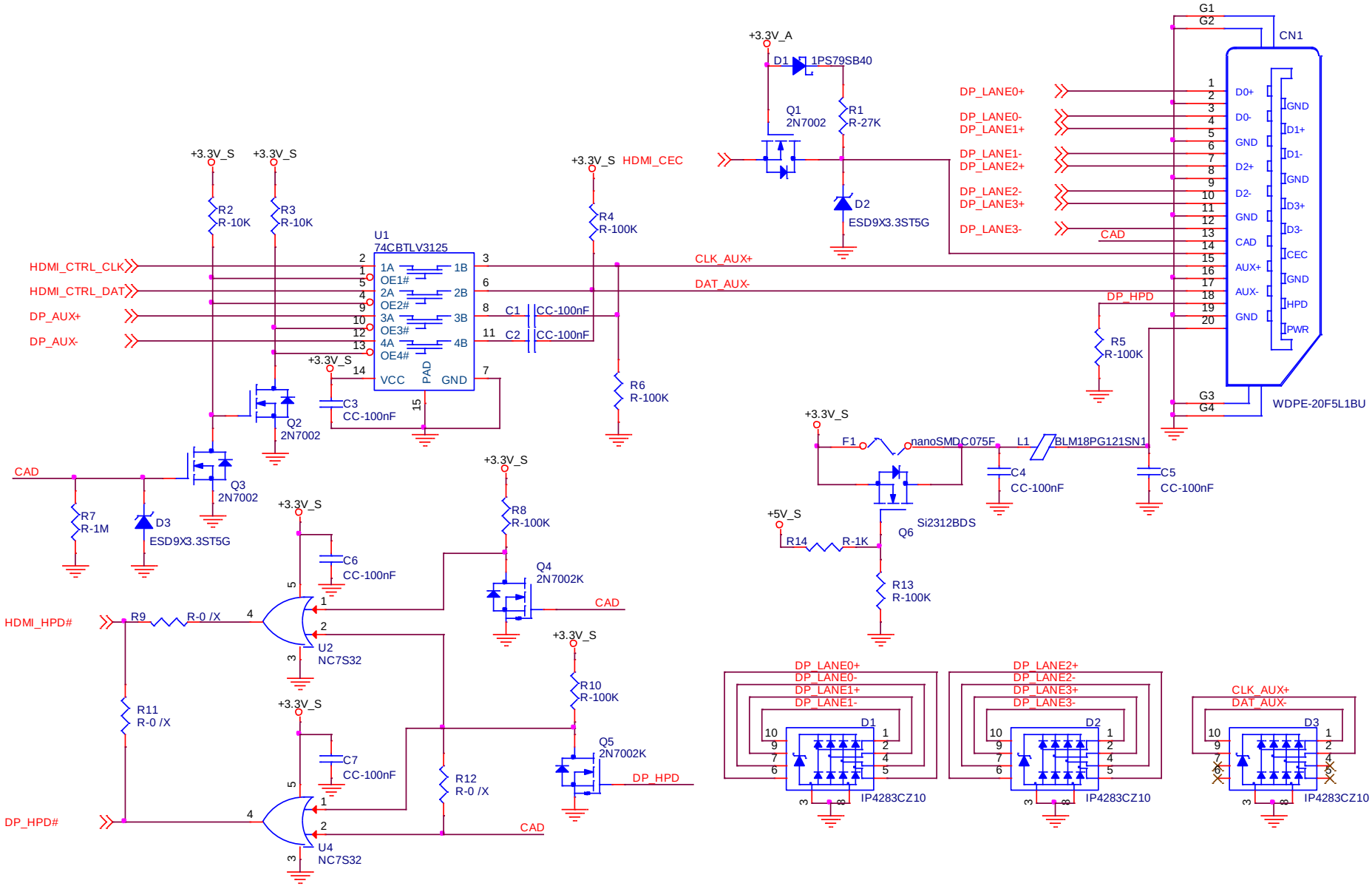
DP_LANE0+/DP_LANE0-: Display Port differential pair #0

DP_AUX+/DP_AUX-: Display Port auxiliary channel differential pair.

DP_HPD#. DisplayPort Hot Plug Detect Input signal. +3.3V_RUN electrical level signal, active low with 10kΩ pull-up resistor. This signal was present on Qseven® specifications until rev. 1.2, while it has been deleted with Qseven specifications rev. 2.0, since the Hot Plug signal for Display Port had been merged with the HPD signal for HDMI. Qseven® specification Errata Sheet for version 2.0, published by SGET consortium, reintroduced this signal for compatibility with Qseven® modules Rel 1.2 compliant.

DP and HDMI interfaces share the same pins on Qseven® Golden Finger Connector. Default SW for Q7-C25 is for HDMI support, to have DP support customer needs to load a dedicated boot.

Please refer to the following schematics as an example of implementation of multimode DisplayPort connection on the carrier board, which will allow the use of external adapters for the conversion to HDMI/DVI.


+3.3V_A
D1
1PS79SB40
Q1
2N7002
R1
R-27K
D2
ESD9X3.3ST5G
+3.3V_S
HDMI_CEC
R4
R-100K
U1
74CBTLV3125
HDMI_CTRL_CLK
HDMI_CTRL_DAT
DP_AUX+
DP_AUX-
CLK_AUX+
DAT_AUX-
C1
CC-100nF
C2
CC-100nF
C3
CC-100nF
R6
R-100K
R2
R-10K
R3
R-10K
Q2
2N7002
CN1
WDPE-20F5L1BU
DP_LANE0+
DP_LANE0-
DP_LANE1+
DP_LANE1-
DP_LANE2+
DP_LANE2-
DP_LANE3+
DP_LANE3-
CAD
DP_HPD
R5
R-100K
F1
nanoSMDC075F
L1
BLM18PG121SN1
C4
CC-100nF
C5
CC-100nF
+5V_S
R14
R-1K
Q6
Si2312BDS
R13
R-100K
Q3
2N7002
R7
R-1M
D3
ESD9X3.3ST5G
R8
R-100K
Q4
2N7002K
C6
CC-100nF
HDMI_HPD#
R9
R-0 /X
U2
NC7S32
R10
R-100K
Q5
2N7002K
C7
CC-100nF
R12
R-0 /X
R11
R-0 /X
DP_HPD#
U4
NC7S32
IP4283CZ10
IP4283CZ10
IP4283CZ10

3.2.12 SPI interface signals

The signals related to SPI are as follows:

SPI_CS0#: SPI primary Chip select, active low output signal. Electrical level +3.3V_RUN

SPI_CS1#: SPI secondary Chip select, active low output signal. Electrical level +3.3V_RUN. This signal must be used only in case there are two SPI devices on the carrier board, and the first chip select signal (SPI_CS0#) has already been used. It must not be used in case there is only one SPI device

SPI_SCK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +3.3V_RUN

SPI_MISO: SPI0 Master Data Input, electrical level +3.3V_RUN. Input to i.MX 8M from SPI devices embedded on the Carrier Board

SPI_MOSI: SPI0 Master Data Output, electrical level +3.3V_RUN. Output from i.MX 8M to SPI devices embedded on the Carrier Board

SPI interface can support speed up to 20MHz. Note that this interface is not available in all factory configurations. Please be sure of factory configuration for the module ordered.

3.2.13 GPIO interface signals

The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

This module provides up to 8xGPIO.

The signals related to GPIO are as follows:

GPIO[0:7]: General Purpose Input/Output, electrical level +3.3V_RUN.

3.2.14 CAN interface signals

The NXP i.MX 8M processor provide a Controller Area Network (CAN) interface through a Microchip MCP2518FD External CAN FD Controller with SPI interface.

The signals related to CAN are as follows:

CAN0_TX: CAN transmitting signal, electrical level +3.3V_RUN

CAN0_RX: CAN receiving signal, electrical level +3.3V_RUN

Please consider that it is not possible to connect Qseven® CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

3.2.15 Power Management signals

According to Qseven® specifications, on the golden edge finger connector there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWGIN: Power Good Input, +5V_RUN tolerant active high signal. It must be driven on the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

PWRBTN#: Power Button Input, active low, +3.3V_ALW. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

RSTBTN#: Reset Button Input, active low, +3.3V_RUN voltage signal with 10kΩ pull-up resistor. This signal can be connected to a momentary push-button: a pulse to GND of this signal will reset the Qseven® module.

BATLOW#: Battery Low Input, active low, +3.3V_ALW voltage signal with 10kΩ pull-up resistor. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. Can be left unconnected if not used

WAKE#: Wake Input, active low +3.3V_ALW electrical voltage signal with 10kΩ pull-up resistor. This signal can be driven low, on the carrier board, to report that a Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

SUS_S3#: S3 status output, active low +3.3V_ALW electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S5#: S5 status output, active low +3.3V_ALW electrical voltage signal. This signal is used, on the carrier board, to shut off the power supply to all the devices that must become inactive only during S5 (Soft Off) power state.

SLP_BTN#: Sleep button Input, active low +3.3V_ALW electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

LID_BTN#: LID button Input, active low +3.3V_ALW electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

3.2.16 Miscellaneous, Thermal Management and Fan control signals

Here following, a list of Qseven® compliant signals that complete the features of Q7-C25 module.

SMB_CLK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_ALW (but enabled via +3.3V_RUN voltage) with a 2k2Ω pull-up resistor. It is directly managed by ST Microelectronics STM32F100R6H6 microcontroller.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_ALW (but enabled via +3.3V_RUN voltage) with a 2k2Ω pull-up resistor. It is directly managed by ST Microelectronics STM32F100R6H6 microcontroller.

SMB_ALERT#: SM Bus Alert line for System Management. Bidirectional signal, active low, electrical level +3.3V_ALW. directly managed by ST Microelectronics STM32F100R6H6 microcontroller. Any device place on the SM Bus can drive this signal low to signal an event on the bus itself.

GP0_I2C_CLK: general purpose I2C Bus clock line. Bidirectional signal, electrical level +3.3V_RUN with a 2.2kΩ pull-up resistor. It is managed by the SOCs' I2C controller. I2C Bus is able to work in Standard mode (bitrate up to 100Kbps), Fast mode (bitrate up to 400Kbps), Fast-mode Plus (bitrate up to 1Mbps), High-speed mode (bitrate up to 3.4Mbps).

GP0_I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3.3V_RUN with a 2.2kΩ pull-up resistor. It is managed by the SOCs' I2C controller.

WDTRIG#: Watchdog Trigger Input. It is an active low signal, +3.3V_RUN voltage with a 10kΩ pull-up resistor This signal can be used to reset and restart, via Hardware, the internal Watchdog Timer (which is usually managed via Software using Q7-C25 dedicated API - Application Program Interface - libraries).

WDOUT: Watchdog event indicator Output. It is an active high signal, +3.3V_RUN voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW.

BOOT_ALT#: Boot Alternate Input, active low +3.3V_RUN voltage signal with 10kΩ pull-up resistor. When this signal is driven low, then i.MX8M processors starts to work in peripheral mode, i.e. it begins to wait for inputs from an external Host connected to the system. This is used usually when it is necessary to program the

module.

FAN_TACHOIN: External FAN Tachometer Input. +3.3V_RUN voltage signal with 10kΩ pull-up resistor, directly managed by ST Microelectronics STM32F100R6H6 microcontroller

FAN_PWMOUT: PWM output for FAN speed management, +3.3V_RUN voltage signal. It is managed by SOCs' GPIO section.

SPKR: Speaker output, +3.3V_RUN voltage signal, directly managed by SOCs' GPIO section.

THRM#: Thermal Alarm Input. Active Low, +3.3V_RUN voltage signal with 10kΩ pull-up resistor, directly managed by ST Microelectronics STM32F100R6H6 microcontroller. This input gives the possibility, to carrier board's hardware, to indicate to the main module an overheating situation, so that the SoC can begin thermal throttling.

THRMTRIP#: Thermal Trip Output. Active Low, +3.3V_RUN voltage signal with 10kΩ pull-up resistor, directly managed by ST Microelectronics STM32F100R6H6 microcontroller. Thermal Trip indicates an overheating condition of the processor. When goes active, the system immediately transitions to the S5 State (Soft Off).

3.2.17 Manufacturing signals

According to Qseven® Standard specifications, rel. 2.1, on pin designed as MFG_NCx (207÷210) are carried through a multiplexer NXP i.MX8M Internal UART1 signals for firmware and boot loader implementations. Pin 204 (MFG_NC4) drives the selection pin of the multiplexer to enable debug UART1. This pin must be floated to enable debug UART

Pin 207 (MFG_NC0) signal	Pin 208 (MFG_NC2) signal	Pin 209 (MFG_NC1) signal	Pin 210 (MFG_NC3) signal
UART1_RTS	UART1_RXD	UART1_TXD	UART1_CTS

!

The UART interface available on MFG_NCx pins is reserved only for the manufacturing phase; it must not be used by the customer.

It is not possible at all to use these pins to trace the software (for debug purposes)

Chapter 4. Appendices

- Thermal Design

4.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like Q7-C25 module, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

Qseven® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the Qseven® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsinks in some situation can represent the cooling solution. Indeed, when using Q7-C25 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide Q7-C25 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
QC25-DISS-1-PK	Q7-C25 Heat Spreader (Passive)
QC25-DISS-2-PK	Q7-C25 Heatsink (Passive)

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