Qseven

User Manual

Q7-A36

Qseven® Rel. 2.0 Compliant Module
with the Intel® Bay Trail family SOCs

SECO

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	24th June 2015	First Release	SB
1.1	27th July 2015	BIOS Section updated	SB
1.2	7th October 2015	Qseven® Design guide reference Link updated. BIOS Section updated to BIOS rel. 1.07	SB
2.0	29th January 2016	Product name change BIOS Section updated to BIOS rel. 1.09	SB
2.1	9th June 2017	BIOS Section updated	SB
2.2	8th September 2017	BIOS Section updated	SB
2.3	29th September 2017	Display Port connector reference schematics corrected	SB

Every effort has been made to ensure the accuracy of this manual. However, SECO S.r.l. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.r.l. reserves the right to change precise specifications without prior notice to supply the best product possible.

Some of the information found in the BIOS SETUP Chapter has been extracted from the following copyrighted Insyde Software Corp. documents:

- InsydeH2O™ Setup Utility - User Reference Guide

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

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Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
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- Reference specifications

1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.r.l. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.r.l. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The Q7-A36 module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The Q7-A36 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

Whenever handling a Q7-A36 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The Q7-A36 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control
CRT	Cathode Ray Tube. Initially used to indicate a type of monitor, this acronym has been used over time to indicate the analog video interface used to drive them.
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
DDR3	DDR, 3rd generation
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
EHCI	Enhanced Host Controller interface, a high-speed controller for USB ports, able to support USB2.0 standard
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
JTAG	Joint Test Action Group, common name of IEEE1149.1 standard for testing printed circuit boards and integrated circuits through the Debug port
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pairs copper cables, usually used for video applications
MAC	Medium Access Controller, the hardware implementing the Data Link Layer of ISO/OSI-7 model for communication systems

Mbps	Megabits per second
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card having the same interface of SD cards. The eMMC is the embedded version of the MMC. They are devices that incorporate both the memory controller and the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenCL	Open Computing Language, a software library based on C99 programming language, conceived explicitly to realise parallel computing using Graphics Processing Units (GPU)
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OS	Operating System
PCI-e	Peripheral Component Interface Express
PHY	Abbreviation of Physical, it is the device implementing the Physical Layer of ISO/OSI-7 model for communication systems
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
PXE	Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDHC	Secure Digital Host Controller
SM Bus	System Management Bus, a subset of the I2C bus protocol dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signaling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
USB	Universal Serial Bus
V_REF	Voltage reference Pin
VGA	Video Graphics Array. An analog computer display standard, commonly referred to also as CRT.
xHCI	eXtensible Host Controller Interface, Host controller for USB 3.0 ports, which can also manage USB 2.0 and USB1.1 ports

1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
CSI	http://www.mipi.org/specifications/camera-interface
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
JTAG	http://standards.ieee.org/develop/wg/Boundary_Scan_Architecture.html
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
OpenCL	http://www.khronos.org/opencl
OpenGL	http://www.opengl.org
PCI Express	http://www.pcisig.com/specifications/pciexpress
PCI Express mini cards	http://www.pcisig.com/specifications/pciexpress/specifications/specifications/pciexpress/base2/#MCEM2
Qseven® Design Guide	http://www.sget.org/uploads/media/Qseven_Design_Guide_2_0.pdf
Qseven® specifications	http://www.sget.org/uploads/media/Qseven-Spec_2.0_SGET.pdf
Qseven® Errata to rel. 2.0	http://www.sget.org/uploads/media/Qseven-Spec_2.0_SGET_errata_sheet_E2.00-001.pdf

SATA	https://www.sata-io.org
SD Card Association	https://www.sdcard.org/home
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
UEFI	http://www.uefi.org
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip
Intel® Atom™ and Celeron® Bay Trail family	http://ark.intel.com/it/products/codename/55844/Bay-Trail#@Embedded

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram

2.1 Introduction

Q7-A36 is a CPU module, in new Qseven® format, based on the Intel® Atom™ and Celeron® family of System-on-Chips (SOCs) formerly coded as Bay Trail, a series of Single/ Dual / Quad SOCs with 64-bit instruction set.

These SOCs embed all the features usually obtained by combination of CPU + platform Controller hubs, all in one single IC, which allows, therefore, the system minimisation and performance optimisation, which is essential for boards with sizes so reduced as for Qseven® boards, which offers all functionalities of standard PC boards in just 70x70mm.

The board is also available in EXTREME configuration, with all the components mounted onboard certified for industrial temperature ranges (this configuration is not available with the Celeron® processors).

The embedded memory controller allows the integration of up to 8GB of DDR3L Memory directly soldered onboard, speed up to 1333MHz (it depends on the SoC used).

All SOCs embed an Intel® HD Graphics 400 series controller, which offer high graphical performances, with support for Microsoft® DirectX11, OpenGL 3.0, OpenCL 1.2, OpenGLES 2.0 and HW acceleration for video decoding of H.264, MPEG2, MVG, VC-1, VP8 and MJPEG video standards (for H.264, MPEG2 and MVG also HW encoding is offered). This embedded GPU is able to drive two independent displays, by using the interfaces available on Qseven® golden finger connector.

Mass Storage capabilities of the board include two external S-ATA channels, a standard SD interface and one optional eMMC Disk soldered on board.

Other than the interfaces already discussed previously, on Qseven® golden finger connector there are the signals necessary for the implementation of Gigabit Ethernet, one USB 3.0 port, up to 5 x USB 2.0 ports, 18/24-bit Single/Dual Channel LVDS or embedded Display Port interface, HDMI or multi-mode DisplayPort interface, 3 x PCI-Express x 1 lanes, HD Audio interface, I^2C, SPI, LPC and SM buses, UART interface.

Interfacing to the board comes through a single card edge connector, whose pinout is defined by Qseven® specifications Rel.2.0. For external interfacing to standard devices, a carrier board with a 230-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as integration of other peripherals/devices not already included in Q7-A36 CPU module.

On customer request, a FFC/FPC connector can be provided to give access to Image Signal Processor (ISP) of Intel® Atom™ E38xx SOCs (not on Celeron® processors), which supports CSI-2 camera interface (sensors requiring up to four CSI data lanes are supported), with a maximum resolution supported of 1080p60. Please be aware that specific drivers for the camera interface have to be written by the customer, SECO will not provide them.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

2.2 Technical Specifications

System-On-Chips

Intel® Atom™ E3845, Quad Core @1.91GHz, 2MB Cache, 10W TDP
Intel® Atom™ E3827, Dual Core @1.75GHz, 1MB Cache, 8W TDP
Intel® Atom™ E3826, Dual Core @1.46GHz, 1MB Cache, 7W TDP
Intel® Atom™ E3825, Dual Core @1.33GHz, 1MB Cache, 6W TDP
Intel® Atom™ E3815, Single Core @1.46GHz, 512KB Cache, 5W TDP
Intel® Celeron® J1900, Quad Core @2.0GHz, 2MB Cache, 10W TDP
Intel® Celeron® N2930, Quad Core @1.83GHz, 2MB Cache, 7.5W TDP
Intel® Celeron® N2807, Dual Core @1.58GHz, 1MB Cache, 4.3W TDP

Memory

Soldered Down onboard DDR3L memory
E3845, E3827, J1900, N2930: up to 8GB Dual-Channel DDR3L 1333MHz
E3826: up to 8GB Dual-Channel DDR3L 1066MHz
N2807: up to 4GB Single-Channel DDR3L 1333MHz
E3825, E3815: up to 4GB Single-Channel DDR3L 1066MHz

For Industrial Temperature range modules, the maximum capacity of memory currently available is 2GB Single Channel (E3825 and E3815 SoC) or 4GB Dual Channel (E3845, E3827 and E3826 SoC).

Graphics

Integrated Intel® HD Graphics 4000 series controller
Dual independent display support
HW decoding of H.264, MPEG2, MVC, VC1, VP8, MJPEG formats
HW encoding of H.264, MPEG2 and MVC formats

Video Interfaces

HDMI or Multimode Display Port interface
Embedded Display Port or 18/24 bit dual channel LVDS interface
Optional Camera interface

Video Resolutions

HDMI:	Up to 1920x1080p@60Hz
Display Port, eDP:	Up to 2560x1600@60Hz
Optional LVDS interface:	Up to 1920x1200@60Hz

Mass Storage

2 x external S-ATA channels
SD interface
Optional eMMC Disk soldered onboard

USB

1 x USB 3.0 Host Port
6 x USB2.0 Host ports (one shared with USB 2.0 interface)

Networking

Gigabit Ethernet interface

Audio

HD Audio interface

PCI Express

3 x PCI-e x1 lanes

Serial Ports

1 x Serial port (TTL interface)

Other Interfaces

I2C bus
LPC Bus
SM Bus
Thermal / FAN management
SPI interface
Power Management Signals

Power supply voltage: $+5V_{DC}$ ± 5%

Operating temperature: 0°C ÷ +60°C (commercial version) **
-40°C ÷ +85°C (industrial version) **

Dimensions: 70 x70 mm (2.76" x 2.76")

! *** Temperatures indicated are the minimum and maximum temperature that the heatspreader / heatsink can reach in any of its parts. This means that it is customer's responsibility to use any passive cooling solution along with an application-dependent cooling system, capable to ensure that the heatspreader / heatsink temperature remains in the range above indicated. Please also check paragraph 5.1*

2.3 Electrical Specifications

According to Qseven® specifications, Q7-A36 board needs to be supplied only with an external +5V$_{DC}$ power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from +5V_S power rail.

2.3.1 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_S: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_S, +5V_S.

_A: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_A, +3.3V_A.

_U: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_U

2.3.2 Power Consumption

Q7-A36 module, like all Qseven® modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Anyway, power consumption has been measured on +5V_S power rail that supplies the board. For this reason, the values indicated in the table below are real average power consumptions of the board, and are independent from those of the peripherals connected to the Carrier Board.

Power consumption in Suspend and Soft-Off States have been measured on +5V_A power rail. RTC power consumption has been measured on carrier board's backup battery when the system is not powered.

The current consumptions, written in the table of this page, have been measured using the following setups:

- Intel® Atom™ E3845 SoC, 4GB DDR3L, 16GB eMMC soldered onboard
- Intel® Celeron® N2807 SoC, 2GB DDR3L, 32GB eMMC soldered onboard
- Intel® Celeron® J1900 SoC, 4GB DDR3L, no eMMC soldered onboard
- O.S. Windows 7 ultimate SP1
- Bios Release 1.02
- USB mouse and keyboard connected
- HDMI display connected.

Status	SoC		
	E3845	N2807	J1900
Idle, power saving configuration	620 mA	860 mA	548 mA
OS Boot, power saving configuration	680 mA	870 mA	680 mA
Video reproduction@720p, power saving configuration	792 mA	980 mA	745 mA
Video reproduction@1080p, power saving configuration	1017 mA	1056 mA	870 mA
3DMarkVantage benchmark, power saving configuration	1478 mA	1585 mA	1477 mA
3DMarkVantage benchmark, maximum performance	2060 mA	2008 mA	2050mA
Suspend to RAM (typical)		57 mA	
Soft Off (typical)		24 mA	
RTC Power consumption (typical)	2,5µA	2,5µA	2,5µA

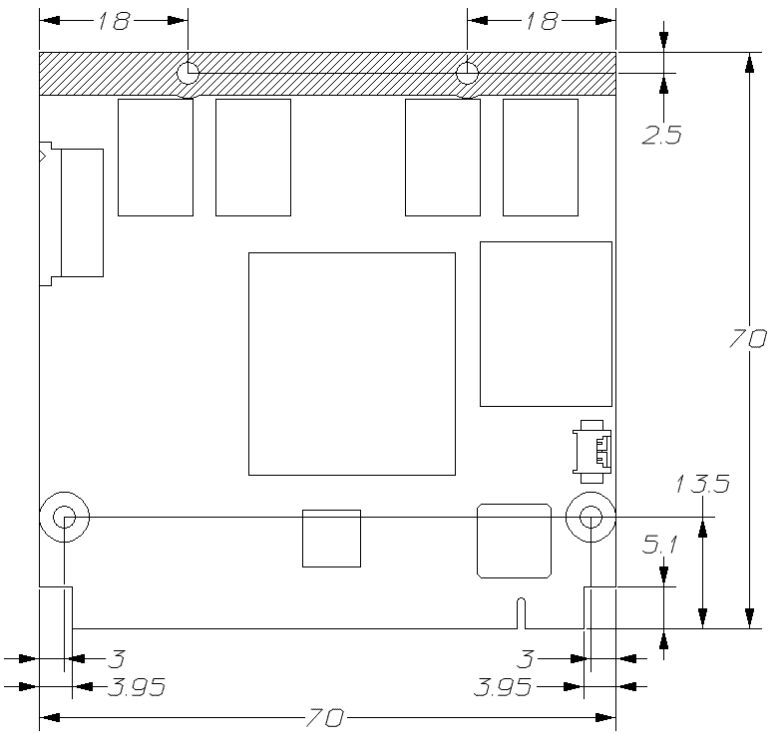
2.4 Mechanical Specifications

According to Qseven® specifications, board dimensions are: 70 x 70 mm (2.76” x 2.76”).

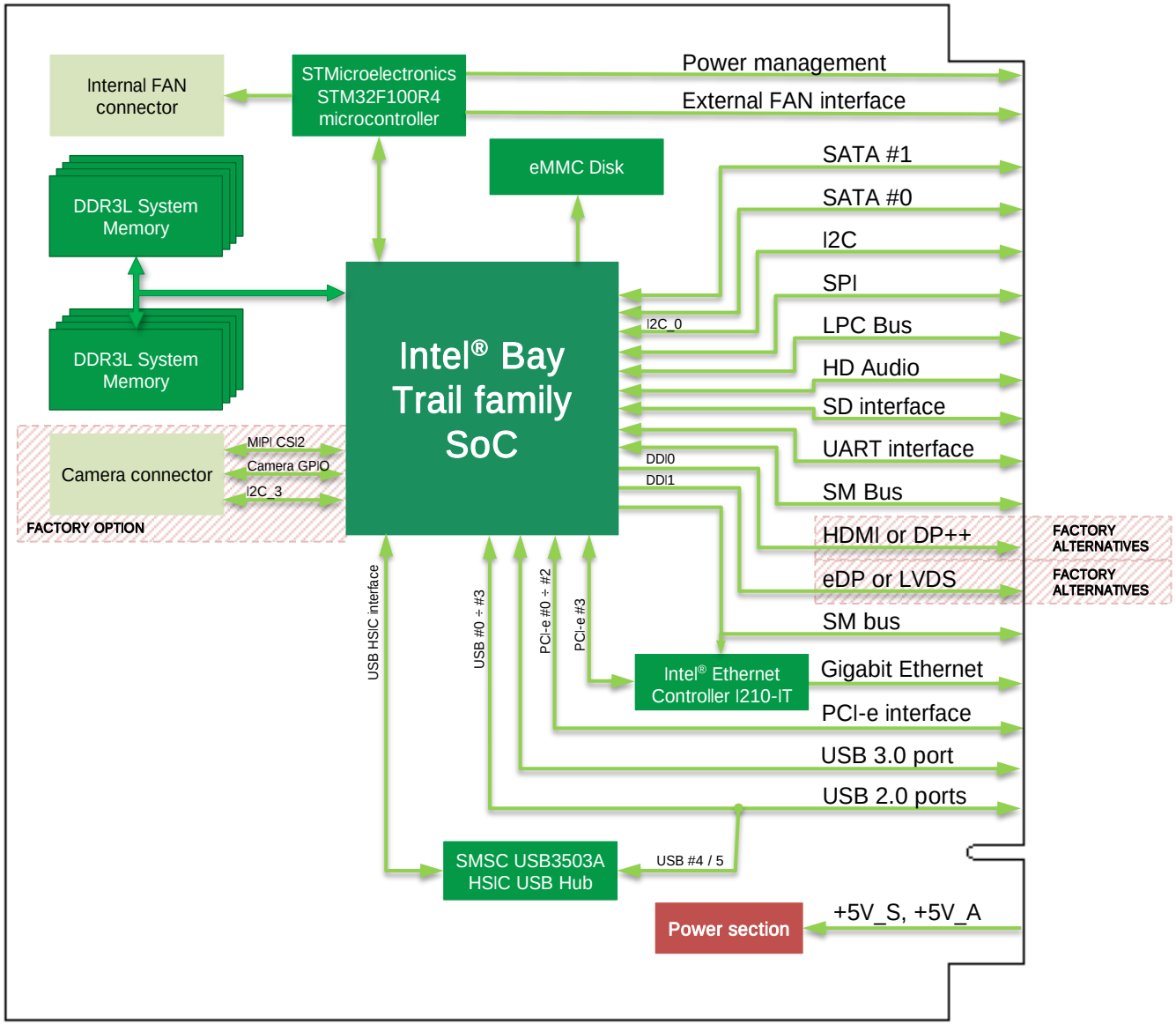
Printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs. Qseven® specification suggests two connector heights, 7.8mm and 7.5mm, but it is also possible to use different connector heights, also remaining compliant to the standard.

When using different connector heights, please consider that, according to Qseven® specifications, components placed on bottom side of Q7-A36 will have a maximum height of 2.2mm ± 0.1. Keep this value in mind when choosing the MXM connector’s height, if it is needed to place components on the carrier board in the zone below the Qseven® module.



2.5 Block Diagram



Chapter 3.
CONNECTORS

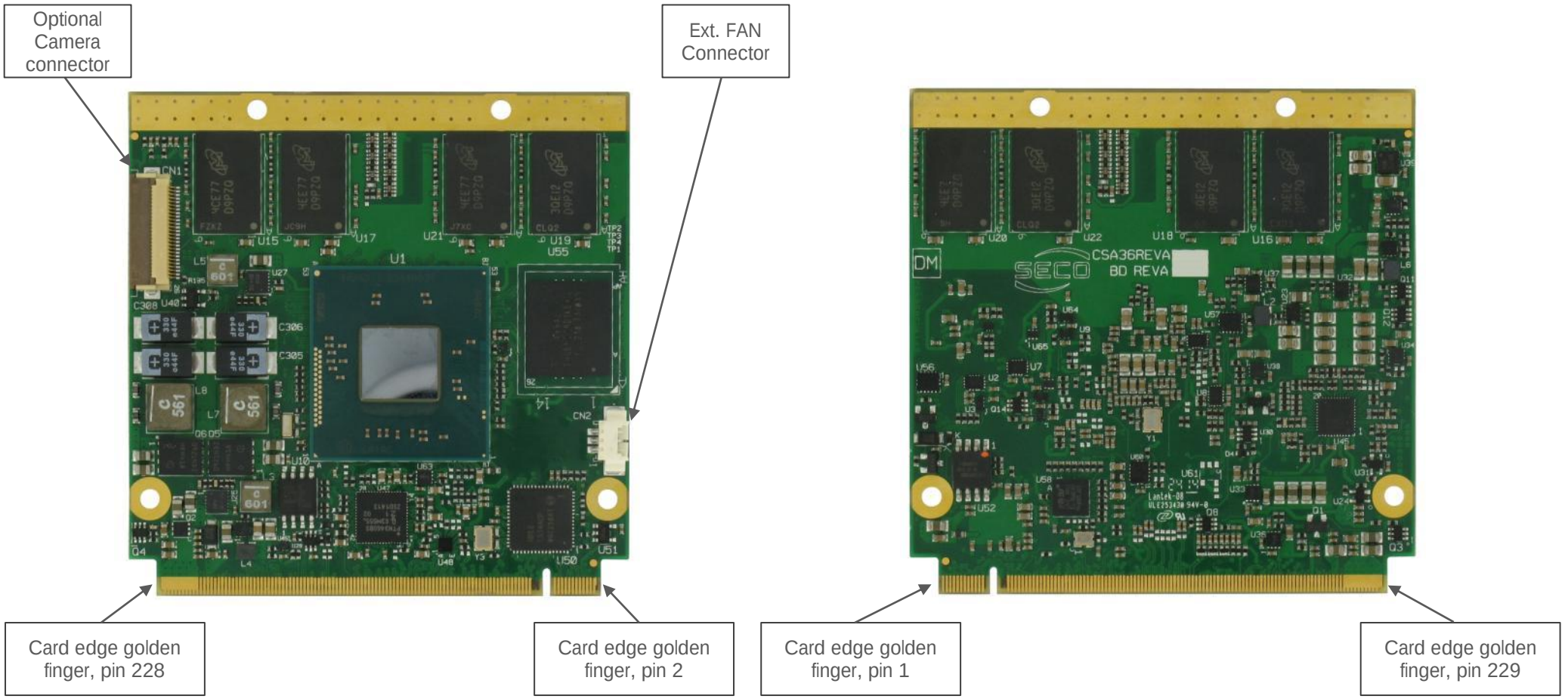
- Introduction
- Connectors description

3.1 Introduction

According to Qseven® specifications, all interfaces to the board are available through a single card edge connector. In addition, a CRT FFC/FPC connector card slot is present on the left side of the board to take advantage of the Intel® Atom™ E38xx family of SOCs' native CRT interface. Moreover, an additional Fan connector has been placed on the right side of the board, in order to allow an easier connection of active heatsinks to the module

TOP SIDE

BOTTOM SIDE

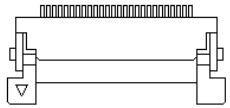


3.2 Connectors description

3.2.1 Optional Camera Connector

Camera Connector - CN1			
Pin	**Signal**	**Pin**	**Signal**
1	CSI_CLK-	14	CSI_GPIO1
2	CSI_CLK+	15	CSI_GPIO2
3	GND	16	CSI_GPIO3
4	CSI_D0-	17	CSI_GPIO4
5	CSI_D0+	18	CSI_GPIO5
6	CSI_D1-	19	CSI_GPIO6
7	CSI_D1+	20	CSI_GPIO9
8	CSI_D2-	21	GND
9	CSI_D2+	22	I2C_DAT
10	CSI_D3-	23	I2C_CLK
11	CSI_D3+	24	GND
12	GND	25	+3.3V_S
13	CSI_GPIO0	26	+3.3V_S

Qseven® specifications Rel. 2.0 define an area, on the PCB, that can be used to place optional I/O connectors of any kind.



For this reason, on customer specific request, the Q7-A36 boards can be provided with an additional connector, which carries out MIPI_CSI-2 interface coming out from Intel® Atom™ E38xx SOCs (not available on Celeron® processors). Please be aware that drivers needed for the Camera interface shall be written by the Customer, will not be provided by SECO.

The Camera connector is an FFC/FPC connector, top contacts, type HIROSE FH12A-26S-0.5SH(55), with pinout shown in the table on the left. The connector mates with 0.5mm pitch 26-poles FFC cables.

Here following the Camera interface signals' description:

CSI_CLK+/CSI_CLK-: MIPI CSI2 Input Clock, Differential pair

CSI_D0+/CS_D0-: MIPI CSI2 Port#1 Input, Differential Pair #0.

CSI_D1+/CS_D1-: MIPI CSI2 Port#1 Input, Differential Pair #1.

CSI_D2+/CS_D2-: MIPI CSI2 Port#1 Input, Differential Pair #2.

CSI_D3+/CS_D3-: MIPI CSI2 Port#1 Input, Differential Pair #3.

CSI_GPIO0: Bidirectional signal, +1.8V level. Used as an output from the shutter switch when pressed halfway.

CSI_GPIO1: Bidirectional signal, +1.8V level. Used as an output from the shutter switch when pressed full way.

CSI_GPIO2: Bidirectional signal, +1.8V level. Usually used as an active high control signal for Xenon Flashes to start charging the capacitor.

CSI_GPIO3: Bidirectional signal, +1.8V level. Usually used as an active low output from Xenon Flashes to signal that the capacitor is fully charged.

CSI_GPIO4: Bidirectional signal, +1.8V level. Usually used as an active high control signal for triggering Xenon Flashes or to enable Torch Mode on LED Flash IC.

CSI_GPIO5: Bidirectional signal, +1.8V level. Usually used to enable Red Eye reduction LED for Xenon Flashes or to Trigger STROBE on LED Flash IC.

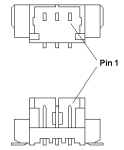
CSI_GPIO6: Bidirectional signal, +1.8V level. Usually used as Camera Strobe signal to indicate to the SoC the beginning of capture, or an active high signal to still camera for powering down the device.

CSI_GPIO9: Bidirectional signal, +1.8V level. Usually used as an active low output to reset the digital still camera.

3.2.2 FAN Connector

FAN Connector - CN2	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN

Depending on the usage model of Q7-A36, for critical applications/environments on the module itself it is available a 3-pin dedicated connector for an external +5VDC FAN.



FAN Connector is a 3-pin single line SMT connector, type MOLEX 53261-0371 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

Please refer to chapter 5.1 for considerations about thermal dissipation.

FAN_POWER: +5V_S derived power rail for FAN, managed by the embedded microcontroller via PWM signal.

FAN_TACHO_IN: tachometric input from the fan to the embedded microcontroller, +3.3V_S electrical level signal with 10kΩ pull-up resistor.

3.2.3 Qseven® Connector

According to Qseven® specifications, all interface signals are reported on the card edge connector, which is a 230-pin Card Edge that can be inserted into standard 230 pin MXM connectors, as described in Qseven® specifications.

Not all signals contemplated in Qseven® standard are implemented on MXM connector, due to the functionalities really implemented on Q7-A36 CPU module. Therefore, please refer to the following table for a list of effective signals reported on MXM connector.

For accurate signals description, please consult the following paragraphs.

NOTE: Even pins are available on top side of CPU board; odd pins are available on bottom side of CPU board. Please refer to board photos.

Qseven® Golden Finger Connector - CN4

BOTTOM SIDE				TOP SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	1	2	GND	PWR	
GBE	I/O	GBE_MDI3-	3	4	GBE_MDI2-	I/O	GBE
GBE	I/O	GBE_MDI3+	5	6	GBE_MDI2+	I/O	GBE
GBE	O	GBE_LINK100#	7	8	GBE_LINK1000#	O	GBE
GBE	I/O	GBE_MDI1-	9	10	GBE_MDI0-	I/O	GBE
GBE	I/O	GBE_MDI1+	11	12	GBE_MDI0+	I/O	GBE
GBE	O	GBE_LINK#	13	14	GBE_ACT#	O	GBE
	N.A.	N.C.	15	16	SUS_S5#	O	PWR_MGMT
PWR_MGMT	I	WAKE#	17	18	SUS_S3#	O	PWR_MGMT
PWR_MGMT	O	SUS_STAT#	19	20	PWRBTN#	I	PWR_MGMT
PWR_MGMT	I	SLP_BTN#	21	22	LID_BTN#	I	PWR_MGMT
	PWR	GND	23	24	GND	PWR	
	PWR	GND	25	26	PWGIN	I	PWR_MGMT
PWR_MGMT	I	BATLOW#	27	28	RSTBTN#	I	PWR_MGMT
SATA	O	SATA0_TX+	29	30	SATA1_TX+	O	SATA
SATA	O	SATA0_TX-	31	32	SATA1_TX-	O	SATA
SATA	O	SATA_ACT#	33	34	GND	PWR	
SATA	I	SATA0_RX+	35	36	SATA1_RX+	O	SATA

SATA	I	SATA0_RX-	37	38	SATA1_RX-	O	SATA
	PWR	GND	39	40	GND	PWR	
	N.A.	N.C.	41	42	SDIO_CLK	O	SDIO
SDIO	I	SDIO_CD#	43	44	N.C.	N.A.	
SDIO	I/O	SDIO_CMD	45	46	SDIO_WP	I	SDIO
SDIO	O	SDIO_PWR#	47	48	SDIO_DAT1	I/O	SDIO
SDIO	I/O	SDIO_DAT0	49	50	SDIO_DAT3	I/O	SDIO
SDIO	I/O	SDIO_DAT2	51	52	N.C.	N.A.	
	N.A.	N.C.	53	54	N.C.	N.A.	
	N.A.	N.C.	55	56	N.C.	N.A.	
	PWR	GND	57	58	GND	PWR	
AUDIO	O	HDA_SYNC	59	60	SMB_CLK	I/O	MISC
AUDIO	O	HDA_RST#	61	62	SMB_DAT	I/O	MISC
AUDIO	O	HDA_BCLK	63	64	SMB_ALERT#	I/O	MISC
AUDIO	I	HDA_SDI	65	66	GP0_I2C_CLK	I/O	MISC
AUDIO	O	HDA_SDO	67	68	GP0_I2C_DAT	I/O	MISC
MISC	I	THRM#	69	70	WDTRIG#	I	MISC
	N.A.	N.C.	71	72	WDOUT	O	MISC
	PWR	GND	73	74	GND	PWR	
USB	I/O	USB_SSTX0-	75	76	USB_SSRX0-	I/O	USB
USB	I/O	USB_SSTX0+	77	78	USB_SSRX0+	I/O	USB
	N.A.	N.C.	79	80	USB_4_5_OC#	I	USB
USB	I/O	USB_P5-	81	82	USB_P4-	I/O	USB
USB	I/O	USB_P5+	83	84	USB_P4+	I/O	USB
USB	I	USB_2_3_OC#	85	86	USB_0_1_OC#	I	USB
USB	I/O	USB_P3-	87	88	USB_P2-	I/O	USB
USB	I/O	USB_P3+	89	90	USB_P2+	I/O	USB
	N.A.	N.C.	91	92	N.C.	N.A.	
USB	I/O	USB_P1-	93	94	USB_P0-	I/O	USB
USB	I/O	USB_P1+	95	96	USB_P0+	I/O	USB

	PWR	GND	97	98	GND	PWR	
LVDS/eDP	O	LVDS_A0+ / eDP0_TX0+	99	100	LVDS_B0+	O	LVDS
LVDS/eDP	O	LVDS_A0- / eDP0_TX0-	101	102	LVDS_B0-	O	LVDS
LVDS/eDP	O	LVDS_A1+ / eDP0_TX1+	103	104	LVDS_B1+	O	LVDS
LVDS/eDP	O	LVDS_A1- / eDP0_TX1-	105	106	LVDS_B1-	O	LVDS
LVDS/eDP	O	LVDS_A2+ / eDP0_TX2+	107	108	LVDS_B2+	O	LVDS
LVDS/eDP	O	LVDS_A2- / eDP0_TX2-	109	110	LVDS_B2-	O	LVDS
LVDS/eDP	O	LVDS_PPEN	111	112	LVDS_BLEN	O	LVDS/eDP
LVDS/eDP	O	LVDS_A3+ / eDP0_TX3+	113	114	LVDS_B3+	O	LVDS
LVDS/eDP	O	LVDS_A3- / eDP0_TX3-	115	116	LVDS_B3-	O	LVDS
	PWR	GND	117	118	GND	PWR	
LVDS	O	LVDS_A_CLK+ / eDP0_AUX+	119	120	LVDS_B_CLK+	O	LVDS
LVDS	O	LVDS_A_CLK- / eDP0_AUX-	121	122	LVDS_B_CLK-	O	LVDS
LVDS/eDP	O	LVDS_BLT_CTRL	123	124	HDMI_CEC	I/O	HDMI
LVDS	O	LVDS_DID_DAT	125	126	eDP0_HPD#	O	eDP
LVDS	O	LVDS_DID_CLK	127	128	N.C.	N.A.	
	N.A.	N.C.	129	130	N.C.	N.A.	
HDMI/DP	O	TMDS_CLK+ / DP_LANE3+	131	132	N.C.	N.A.	
HDMI/DP	O	TMDS_CLK- / DP_LANE3-	133	134	N.C.	N.A.	
	PWR	GND	135	136	GND	PWR	
HDMI/DP	O	TMDS_TX1+ / DP_LANE1+	137	138	DP_AUX+	I/O	DP
HDMI/DP	O	TMDS_TX1- / DP_LANE1-	139	140	DP_AUX-	I/O	DP
	PWR	GND	141	142	GND	PWR	
HDMI/DP	O	TMDS_TX0+ / DP_LANE2+	143	144	N.C.	N.A.	
HDMI/DP	O	TMDS_TX0- / DP_LANE2-	145	146	N.C.	N.A.	
	PWR	GND	147	148	GND	PWR	
HDMI/DP	O	TMDS_TX2+ / DP_LANE0+	149	150	HDMI_CTRL_DAT	I/O	HDMI
HDMI/DP	O	TMDS_TX2- / DP_LANE0-	151	152	HDMI_CTRL_CLK	I/O	HDMI
HDMI/DP	I	HDMI_HPD#	153	154	DP_HPD#	I	DP
PCI-E	O	PCIE_CLK_REF+	155	156	PCIE_WAKE#	I	PCI-E

PCI-E	O	PCIE_CLK_REF-	157	158	PCIE_RST#	O	PCI-E
	PWR	GND	159	160	GND	PWR	
	N.A.	N.C.	161	162	N.C.	N.A.	
	N.A.	N.C.	163	164	N.C.	N.A.	
	PWR	GND	165	166	GND	PWR	
PCI-E	O	PCIE2_TX+	167	168	PCIE2_RX+	I	PCI-E
PCI-E	O	PCIE2_TX-	169	170	PCIE2_RX-	I	PCI-E
UART	O	UART0_TX	171	172	UART0_RTS#	O	UART
PCI-E	O	PCIE1_TX+	173	174	PCIE1_RX+	I	PCI-E
PCI-E	O	PCIE1_TX-	175	176	PCIE1_RX-	I	PCI-E
UART	I	UART0_RX	177	178	UART0_CTS#	I	UART
PCI-E	O	PCIE0_TX+	179	180	PCIE0_RX+	I	PCI-E
PCI-E	O	PCIE0_TX-	181	182	PCIE0_RX-	I	PCI-E
	PWR	GND	183	184	GND	PWR	
LPC	I/O	LPC_AD0	185	186	LPC_AD1	I/O	LPC
LPC	I/O	LPC_AD2	187	188	LPC_AD3	I/O	LPC
LPC	O	LPC_CLK	189	190	LPC_FRAME#	O	LPC
LPC	I/O	SERIRQ	191	192	N.C.	N.A.	
	PWR	VCC_RTC (+3.3V_A)	193	194	SPKR	O	MISC
MISC	I	FAN_TACHOIN	195	196	FAN_PWM_OUT	O	MISC
	PWR	GND	197	198	GND	PWR	
SPI	O	SPI_MOSI	199	200	SPI_CS0#	O	SPI
SPI	I	SPI_MISO	201	202	N.C.	N.A.	
SPI	O	SPI_CLK	203	204	MFG_NC4	N.A.	MFG
	PWR	+5V_A	205	206	+5V_A	PWR	
MFG	N.A.	MFG_NC0	207	208	MFG_NC2	N.A.	MFG
MFG	N.A.	MFG_NC1	209	210	MFG_NC3	N.A.	MFG
	PWR	+5V_S	211	212	+5V_S	PWR	
	PWR	+5V_S	213	214	+5V_S	PWR	
	PWR	+5V_S	215	216	+5V_S	PWR	

PWR	+5V_S	217	218	+5V_S	PWR
PWR	+5V_S	219	220	+5V_S	PWR
PWR	+5V_S	221	222	+5V_S	PWR
PWR	+5V_S	223	224	+5V_S	PWR
PWR	+5V_S	225	226	+5V_S	PWR
PWR	+5V_S	227	228	+5V_S	PWR
PWR	+5V_S	229	230	+5V_S	PWR

3.2.3.1 PCI Express interface signals

Q7-A36 can offer externally three PCI Express lane, which are directly managed by Intel® Bay trail family of SOCs.

PCI express Gen 2.0 (5Gbps) is supported.

Here following the signals involved in PCI express management

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE1_TX+/PCIE1_TX-: PCI Express lane #1, Transmitting Output Differential pair

PCIE1_RX+/PCIE1_RX-: PCI Express lane #1, Receiving Input Differential pair

PCIE2_TX+/PCIE2_TX-: PCI Express lane #2, Transmitting Output Differential pair

PCIE2_RX+/PCIE2_RX-: PCI Express lane #2, Receiving Input Differential pair

PCIE_CLK_REF+/ PCIE_CLK_REF-: PCI Express Reference Clock, Differential Pair. Please consider that only one reference clock is supplied, while there are three different PCI express lanes. When more than one PCI Express lane is used on the carrier board, then a zero-delay buffer must be used to replicate the reference clock to all the devices.

PCIE_WAKE#: Qseven® Module's Wake Input, it must be externally driven by devices requiring waking up the system. Since it is an Active-Low Input to the module, this signal is pulled-up with a 27kΩ resistor to +3.3V_A power rail. On the carrier board, connect it directly to the PCI-e/miniPCI-e connector's WAKE# signal, or to WAKE# signal of any eventual PCI-e Controller present on the Carrier Board.

PCIE_RST#: Reset Signal that is sent from Qseven® Module to any PCI-e device available on the carrier board. It is a 3.3V active-low signal; it can be used directly to drive externally a single RESET Signal. In case Reset signal is needed for multiple devices, it is necessary to provide for a buffer on the carrier board.

3.2.3.2 UART interface signals

According to newest Qseven® Rel. 2.0 specifications, Q7-A36 offers one UART interface, directly managed by Intel® Bay Trail family of SOCs.

Here following the signals related to UART interface:

UART0_TX: UART Interface, Serial data Transmit (output) line, 3.3V_S electrical level.

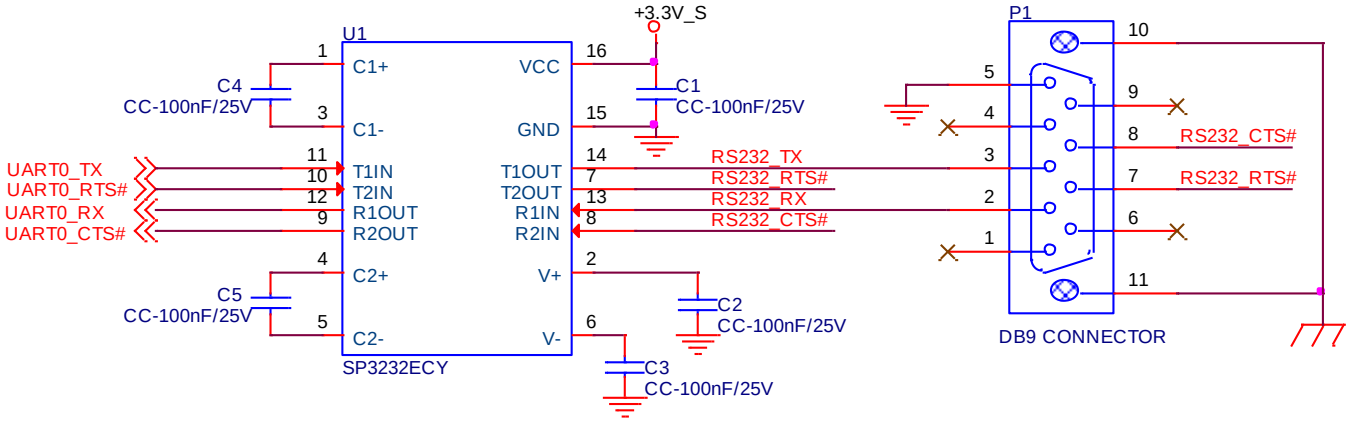
UART0_RX: UART Interface, Serial data Receive (input) line, 3.3V_S electrical level.

UART0_RTS#: UART Interface, Handshake signal, Request to Send (output) line, 3.3V_S electrical level.

UART0_CTS#: UART Interface, Handshake signal, Clear to Send (Input) line, 3.3V_S electrical level.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it isn't needed explicitly to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The following schematic shows an example of implementation of RS-232 transceiver for the Carrier board



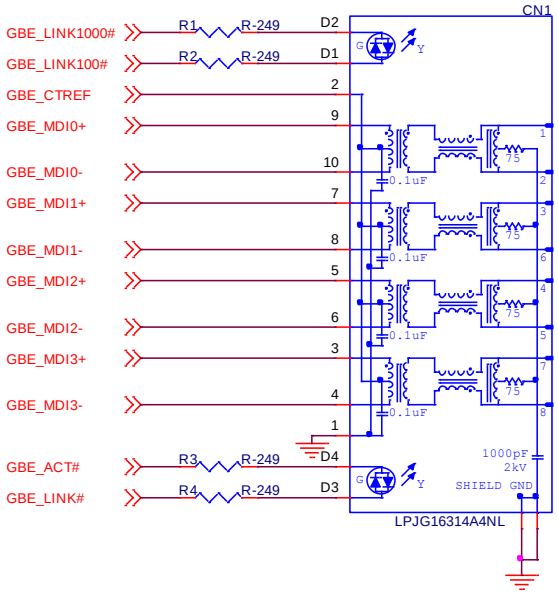
All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.r.l. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

3.2.3.3 Gigabit Ethernet signals

The Gigabit Ethernet interface is realised, on Q7-A36 module, using an Intel® I210 Gigabit Ethernet controller, which is interfaced to the SoC through PCI-express lane #3.



Here following the signals involved in PCI express management

GBE_MDI0+/GBE_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE_MDI1+/GBE_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE_MDI2+/GBE_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE_MDI3+/GBE_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE_ACT#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_A.

GBE_LINK#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_A.

GBE_LINK100#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_A.

GBE_LINK1000#: Ethernet controller 1Gbps link indicator, Active Low Output signal, electrical level +3.3V_A.

These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected. Please look to the schematic on the left as an example of implementation of Gigabit Ethernet connector. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. Intel® I210 Gigabit Ethernet controller, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on Qseven® golden finger connector

3.2.3.4 S-ATA signals

The Intel® Bay Trail family of SOCs offers two S-ATA interfaces, which are carried out on the golden finger connector.

The interfaces are SATA II, with support of 1.5Gbps and 3.0 Gbps data rates

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair

SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair (optional, factory alternative to embedded SSD).

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair (optional, factory alternative to embedded SSD).

SATA_ACT#: Serial ATA Activity Led. Active low output signal at +3.3V_S voltage.

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

On the carrier board, these signals can be carried out directly to the SATA connector.

3.2.3.5 USB interface signals

The Intel® Bay Trail family of SOCs offers an xHCI controller, which is able to manage one Superspeed port (i.e. USB 3.0 compliant) and four USB 1.x / 2.0 Host ports, or, alternatively, an EHCI Controller, which is able to manage only the four USB 1.x / USB 2.0 host ports. It is possible to select which one of the controllers (xHCI or EHCI) must be enabled via BIOS settings (please check par. 4.3.3 for further details).

Furthermore, the SoC makes available one HSIC interface, which is used to manage an HSIC USB Hub that allows the module to have up to 6 USB 2.0 ports.

All USB 2.0 ports are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Here following the signals related to USB interfaces.

USB_P0+/USB_P0-: Universal Serial Bus Port #0 differential pair (coming out from Intel® Atom™ E38xx SoC).

USB_P1+/USB_P1-: Universal Serial Bus Port #1 differential pair (coming out from Intel® Atom™ E38xx SoC).

USB_P2+/USB_P2-: Universal Serial Bus Port #2 differential pair (coming out from Intel® Atom™ E38xx SoC).

USB_P3+/USB_P3-: Universal Serial Bus Port #3 differential pair (coming out from Intel® Atom™ E38xx SoC).

USB_P4+/USB_P4-: Universal Serial Bus Port #4 differential pair (coming out from SMSC USB3503 HSIC USB Hub Downstream port #2).

USB_P5+/USB_P5-: Universal Serial Bus Port #5 differential pair (coming out from SMSC USB3503 HSIC USB Hub Downstream port #3).

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair; it is managed by xHCI controller.

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair; it is managed by xHCI controller.

USB_0_1_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port#0 and #1 of Q7-A36 module

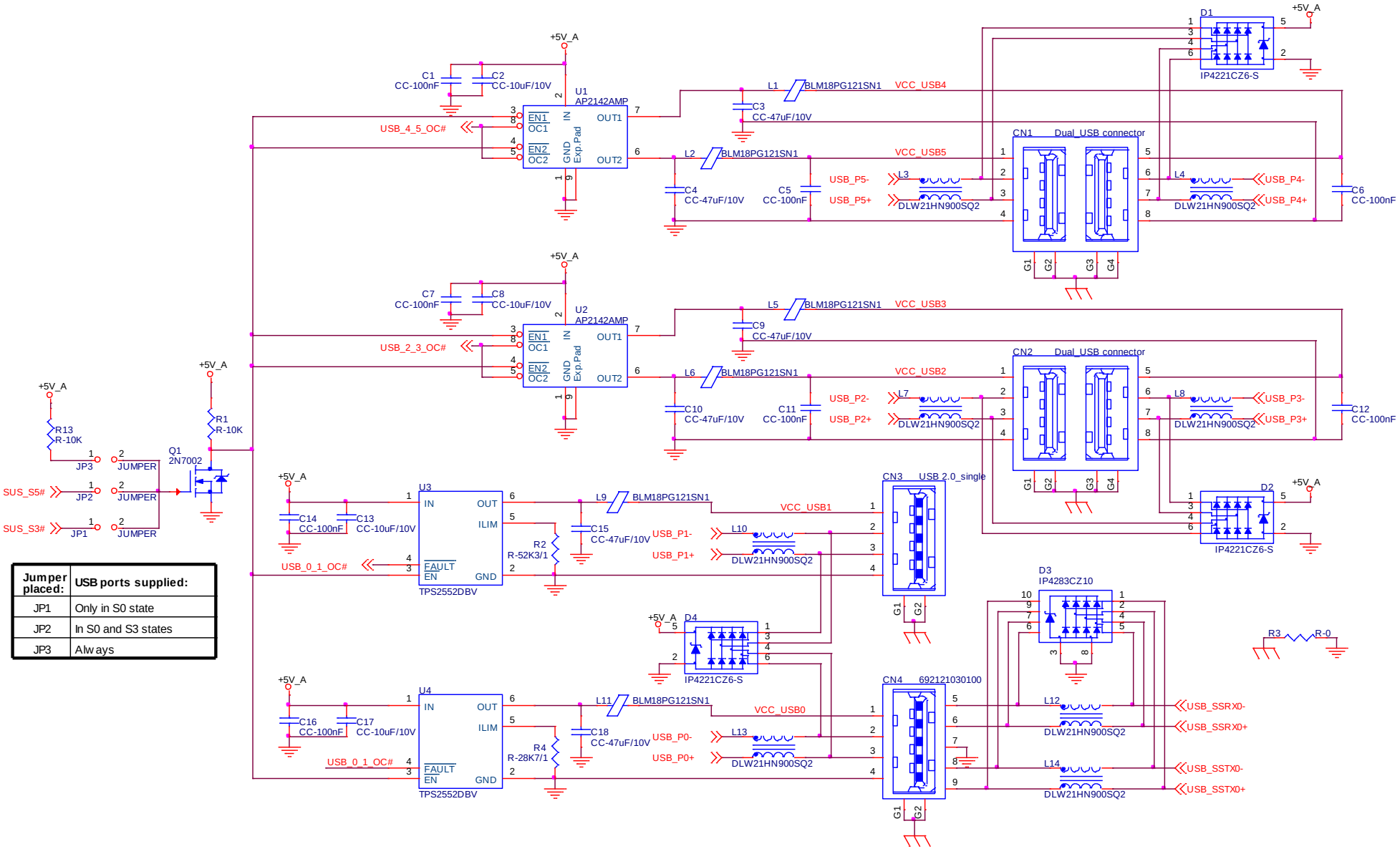
USB_2_3_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Ports #2 and #3 of Q7-A36 module

USB_4_5_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #4 and/or #5 of Q7-A36 module (those managed by SMSC USB 3503 HSIC USB Hub)

Please notice that for correct management of Overcurrent signals, power distribution switches are needed on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

The schematics in the following page show an example of implementation on the Carrier Board. In there, USB ports #1, #2, #3, #4 and #5 are carried out to standard USB 2.0 Type A receptacles, while USB 2.0 port #0, along with the Superspeed USB port, is carried to a standard USB 3.0 Type A receptacle. For correct implementation of USB 3.0 connection, the Superspeed port must be paired with USB 2.0 port #0.



Jumper placed:	USB ports supplied:
JP1	Only in S0 state
JP2	In S0 and S3 states
JP3	Always

3.2.3.6 SD interface signals

The Intel® Bay Trail family of SOCs offers one SD Card controller, able to support SD Card 3.0 interface.

Such an SD controller complies with SD Host Controller Standard Specification version 3.0.

The SD port is externally accessible through the golden edge finger connector, and can work in 1-bit and 4-bit mode.

Signals involved with SD interface are the following:

SDIO_PWR#: SD power enable. Active Low Output signal, electrical level +3.3V_S. This signal can be used on the Carrier board to enable the power line for the SD card.

SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +3.3V_S with 100kΩ pull-up resistor. This signal must be externally pulled low to signal that a SD Card Device is present.

SDIO_CLK: Clock Line (output), 50MHz maximum frequency for SD High Speed Mode

SDIO_CMD: Command/Response line. Bidirectional signal, electrical level +3.3V_S, used to send command from Host (E38xx SoC) to the connected card, and to send the response from the card to the Host.

SDIO_WP: Write Protect input, electrical level +3.3V_S with 100kΩ pull-up resistor. It is used to communicate the status of Write Protect switch of the external SD card. Since microSD cards don't manage this signal, it is important that, when designing carrier boards with microSD slots, this signal must be tied to GND, otherwise the OS will always consider the card as protected from writing.

SDIO_DAT[0÷3]: SD Card data bus. SDIO_DAT0 signal is used for all communication modes. SDIO_DAT[1÷3] signals are required for 4-bit communication mode.

3.2.3.7 Audio interface signals

Q7-A36 module supports HD audio format, thanks to native support offered by the processor to this audio codec standard.

Here following the signals related to HD Audio interface:

HDA_SYNC: HD Audio Serial Bus Synchronization. 48kHz fixed rate output from the module to the Carrier board, electrical level +3.3V_S.

HDA_RST#: HD Audio Codec Reset. Active low signal, output from the module to the Carrier board, electrical level +3.3V_S.

HDA_BCLK: HD Audio Serial Bit Clock signal. 24MHz serial data clock generated by the Intel HD audio controller, output from the module to the Carrier board, electrical level +3.3V_S.

HDA_SDO: HD Audio Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_SDI: HD Audio Serial Data In signal. Input to the module from the Carrier board, electrical level +3.3V_S.

All these signals have to be connected, on the Carrier Board, to an HD Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.3.8 LVDS Flat Panel signals

The Intel® Bay Trail family of SOCs offers two multi-purpose Digital Display Interfaces, which allow the implementation of HDMI/DVI, Display Port (DP) or embedded Display Port (eDP).

The LVDS interface, which is frequently used in many application fields, is not directly supported by the SoC.

For this reason, considering that LVDS interface can be multiplexed on the same pin with the eDP interface, on Q7-A36 module can be implemented an eDP to LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hx (dual channel mode). Such an interface is derived from SOCs' Digital Display Interface #1.

> **!** Please remember that LVDS interface is not native for the Intel® Bay Trail family of SOCs, it is derived from an optional eDP-to-LVDS bridge. Depending on the factory option purchased, on the same pins it is possible to have available LVDS **or** eDP interface.
>
> Please take care of specifying if it is necessary LVDS interface or eDP, before placing an order of Q7-A36 module.

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Primary Channel #0 differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Primary Channel #0 differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Primary Channel #0 differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Primary Channel #0 differential data pair #3.

LVDS_A_CLK+/LVDS_A_CLK-: LVDS Primary Channel #0 differential clock.

LVDS_B0+/LVDS_B0-: LVDS Secondary Channel #0 differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Secondary Channel #0 differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Secondary Channel #0 differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Secondary Channel #0 differential data pair #3.

LVDS_B_CLK+/LVDS_B_CLK-: LVDS Secondary Channel differential Clock

LVDS_PPEN: +3.3V_S electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display.

LVDS_BLEN: +3.3V_S electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display.

LVDS_BLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

LVDS_DID_DAT: DisplayID DDC Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

LVDS_DID_CLK: DisplayID DDC Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

3.2.3.9 Embedded Display Port (eDP) signals

As described in the previous paragraph, the Intel® Bay Trail family of SOCs offers two multi-purpose Digital Display Interfaces, which allow the implementation of HDMI/DVI, Display Port (DP) or embedded Display Port (eDP).

When the board is not configured with the eDP-to-LVDS bridge, the on the golden edge finger connector is available an eDP interface (derived from SOCs' Digital Display Interface #1), which allows supporting displays with a resolution up to 2560 x 1600 @ 60Hz.

Here following the signals related to eDP management:

eDP0_TX0+/eDP0_TX0-: eDP channel differential data pair #0.

eDP0_TX1+/eDP0_TX1-: eDP channel differential data pair #1.

eDP0_TX2+/eDP0_TX 2-: eDP channel differential data pair #2.

eDP0_TX3+/eDP0_TX3-: eDP channel differential data pair #3.

eDP0_AUX+/eDP0_AUX-: eDP channel differential auxiliary channel.

eDP0_HPD#: eDP channel Hot Plug Detect. Active Low Signal, +3.3V_S electrical level input with 100kΩ pull-up resistor.

LVDS_PPEN: +3.3V_S electrical level output, Panel Power Enable signal. It can be used to turn On/Off the connected display.

LVDS_BLEN: +3.3V_S electrical level output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected display.

LVDS_BLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

3.2.3.10 HDMI interface signals

As told in the previous paragraph, the Intel® Bay Trail family of SOCs offers two Digital Display Interfaces, configurable to work in HDMI/DVI/DP++/eDP modes.

Digital Display Interface #0, in particular, is used to implemented HDMI **or** Multimode Display Port interface.

> **!** Please be aware that the board is factory configured to have HDMI **or** Multimode Display Port interface.
>
> If the board purchased is in HDMI configuration, then voltage level shifters on the carrier board are not necessary (they can also interfere with regular working of the board). When placing an order of Q7-A36 module, please take care of specifying if it must have HDMI interface or DP.

Signals involved in HDMI management are the following:

TMDS_CLK+/TMDS_CLK-: TMDS differential Clock.

TMDS_TX0+/TMDS_TX0-: TMDS differential pair #0

TMDS_TX1+/TMDS_TX1-: TMDS differential pair #1

TMDS_TX2+/TMDS_TX2-: TMDS differential pair #2

HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor. Also used as a strap signal for the Q7-A36 module (please check par. 3.2.4 for further details).

HDMI_CTRL_CLK: DDC Clock line for HDMI panel. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

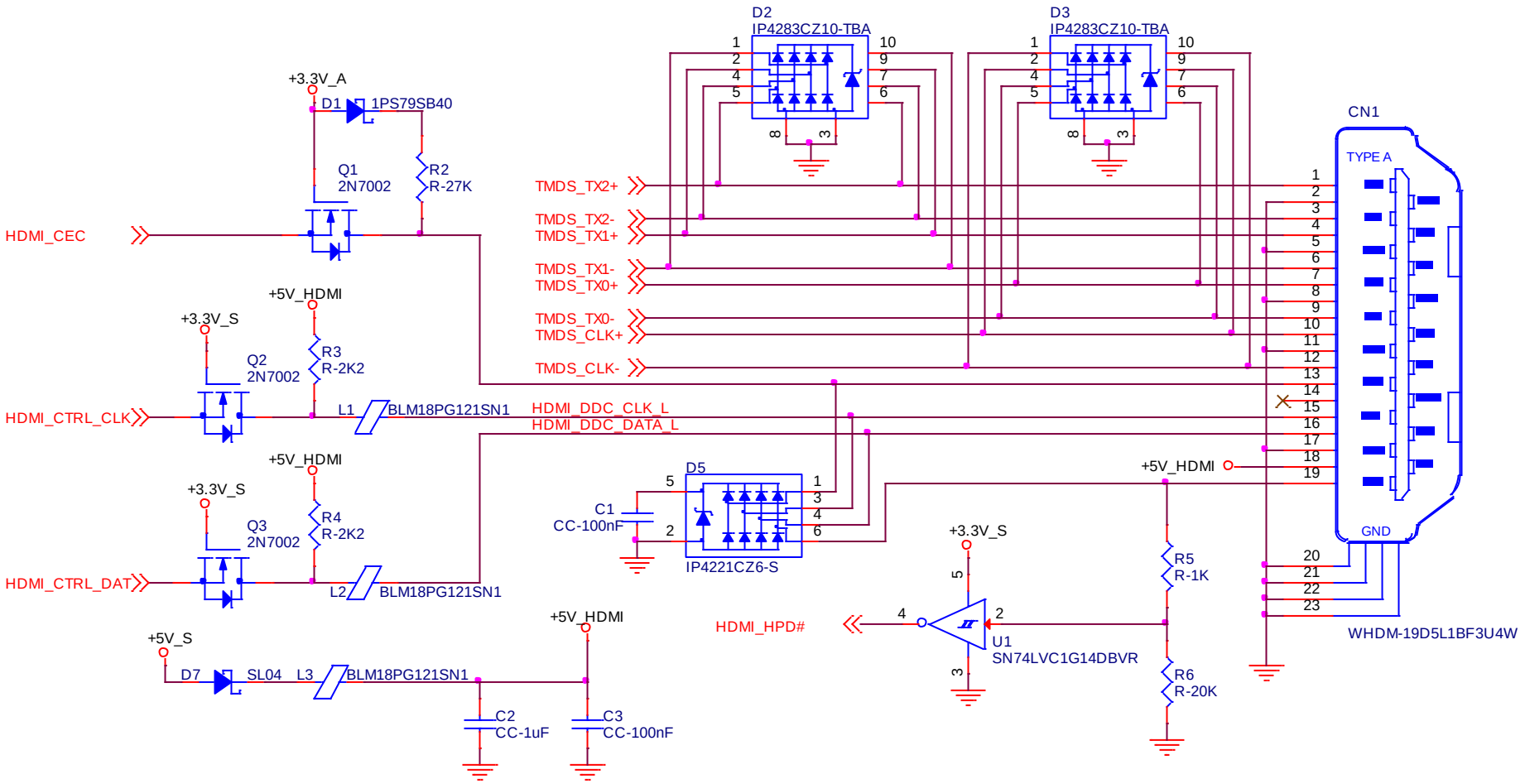
HDMI_CEC: HDMI Consumer Electronics Control (CEC) Line. Bidirectional signal, electrical level +3.3V_S. According to Qseven® specifications, the signal is, in reality, a General Purpose 1_wire bus interface, that can be used for implementation of HDMI_CEC. Real usage of this signal depends on Q7-A36 dedicated API libraries.

HDMI_HPD#: Hot Plug Detect Input signal. +3.3V_S electrical level signal, active low with 100kΩ pull-up resistor. Please consider that HDMI specification assume that the Hot Plug signal is active high, and at +5V_S level. An inverting voltage level shifter is therefore needed on the Carrier board to ensure the working of HDMI port

Please be aware that it is not necessary to implement voltage level shifter for TMDS differential pairs on the Carrier board, but such level shifters are still necessary on Control data/Clock signals, as well as for Hot Plug Detect signal.

Voltage clamping diodes are also highly recommended on all signal lines for ESD suppression.

Please refer to the following schematics as an example of implementation of HDMI connection + voltage level shifters on the carrier board.


D2
IP4283CZ10-TBA
D3
IP4283CZ10-TBA
CN1
TYPE A
GND
WHDM-19D5L1BF3U4W
+3.3V_A
D1
1PS79SB40
Q1
2N7002
R2
R-27K
HDMI_CEC
+5V_HDMI
+3.3V_S
Q2
2N7002
R3
R-2K2
HDMI_CTRL_CLK
L1
BLM18PG121SN1
+5V_HDMI
+3.3V_S
Q3
2N7002
R4
R-2K2
HDMI_CTRL_DAT
L2
BLM18PG121SN1
+5V_S
D7
SL04
L3
BLM18PG121SN1
+5V_HDMI
C2
CC-1uF
C3
CC-100nF
TMDS_TX2+
TMDS_TX2-
TMDS_TX1+
TMDS_TX1-
TMDS_TX0+
TMDS_TX0-
TMDS_CLK+
TMDS_CLK-
HDMI_DDC_CLK_L
HDMI_DDC_DATA_L
D5
C1
CC-100nF
IP4221CZ6-S
+5V_HDMI
+3.3V_S
HDMI_HPD#
U1
SN74LVC1G14DBVR
R5
R-1K
R6
R-20K

3.2.3.11 DP interface signals

As told in the previous paragraph, the Intel® Bay Trail family of SOCs offers two Digital Display Interfaces, configurable to work in HDMI/DVI/DP/eDP modes.

Digital Display Interface #0, in particular, is used to implemented HDMI **or** Multimode Display Port interface.

Please be aware that this interface is a multimode Display Port: this means that it is possible to use it directly for the connection of Display Port compatible monitors or converted to HDMI/DVI interface on the carrier board or on the external connector (by using an adapter)

If the board purchased is in DP configuration, then the following signals will be available on Qseven® golden finger connector:

DP_LANE3+/DP_LANE3-: Display Port differential pair #3.

DP_LANE2+/DP_LANE2-: Display Port differential pair #2.

DP_LANE1+/DP_LANE1-: Display Port differential pair #1

DP_LANE0+/DP_LANE0-: Display Port differential pair #0

DP_AUX+/DP_AUX-: Display Port auxiliary channel differential pair.

HDMI_HPD#: Hot Plug Detect Input signal. +3.3V_S electrical level signal, active low with 100kΩ pull-up resistor. Please consider that Display Port specifications assume that the Hot Plug signal is active high. On the carrier board, therefore, it is necessary to invert the signal to ensure the working of Display Port interface.

DP_HPD#. DisplayPort Hot Plug Detect Input signal. +3.3V_S electrical level signal, active low with 100kΩ pull-up resistor. This signal was present on Qseven specifications until rev. 1.2, while it has been deleted with Qseven specifications rev. 2.0, since the Hot Plug signal for Display Port had been merged with the HPD signal for HDMI. Qseven® specification Errata Sheet for version 2.0, published by SGET consortium, reintroduced this signal for compatibility with Qseven® modules Rel 1.2 compliant. On Q7-A36 module, this signal is electrically tied to DPHDMI_HPD#.

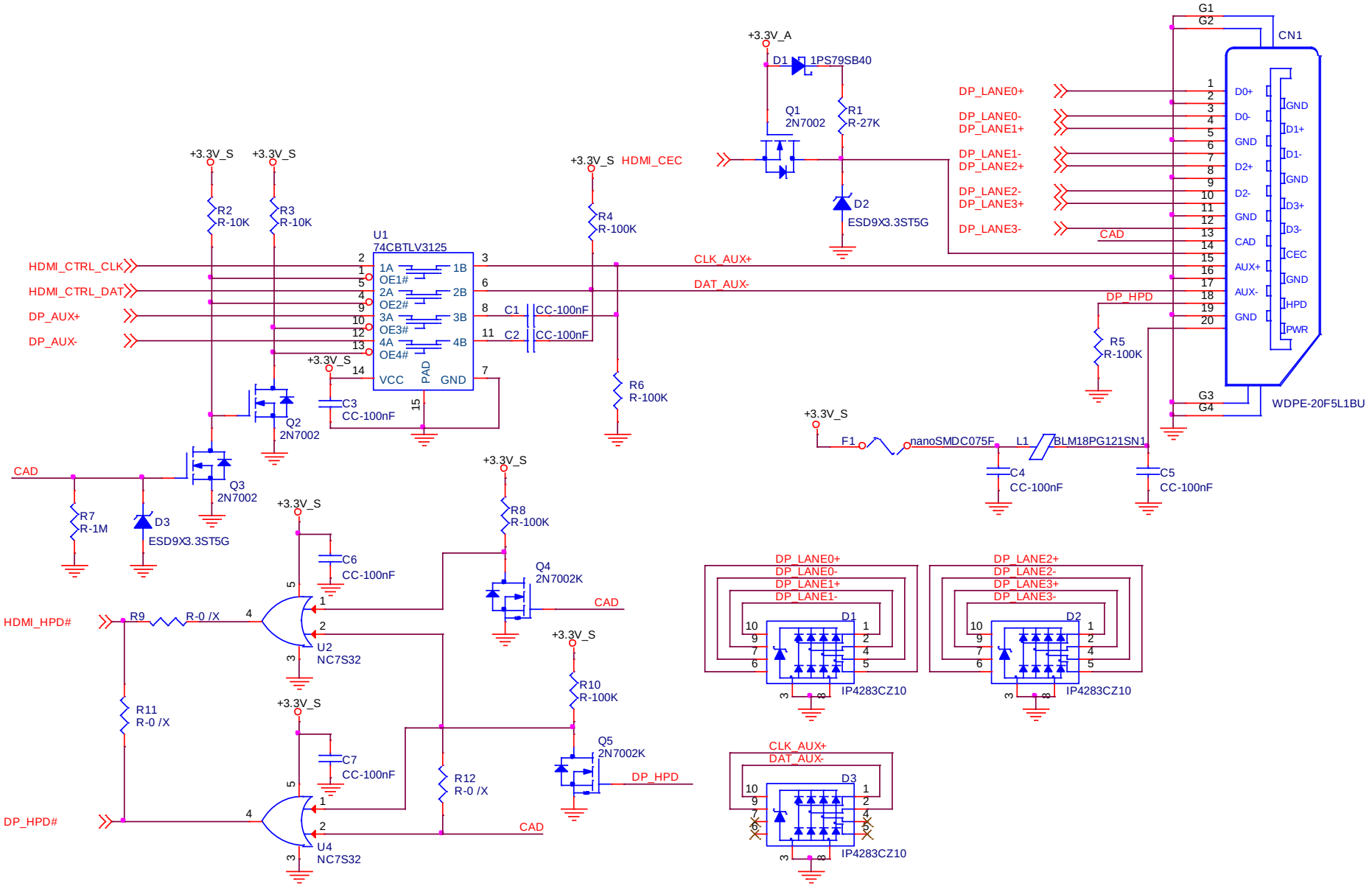
The following signals, used only for HDMI interface, are also available, for a correct implementation, on the Carrier Board, of a multi-mode Display Port connection.

HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor. Also used as a strap signal for the Q7-A36 module (please check par. 3.2.4 for further details).

HDMI_CTRL_CLK: DDC Clock line for HDMI panel. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

HDMI_CEC: HDMI Consumer Electronics Control (CEC) Line. Bidirectional signal, electrical level +3.3V_S. According to Qseven® specifications, the signal is, in reality, a General Purpose 1_wire bus interface, that can be used for implementation of HDMI_CEC. Real usage of this signal depends on Q7-A36 dedicated API libraries.

Please refer to the following schematics as an example of implementation of multimode DisplayPort connection on the carrier board, which will allow the use of external adapters for the conversion to HDMI/DVI.


+3.3V_A
D1
1PS79SB40
Q1
2N7002
R1
R-27K
D2
ESD9X3.3ST5G
HDMI_CEC
+3.3V_S
R4
R-100K
U1
74CBTLV3125
HDMI_CTRL_CLK
HDMI_CTRL_DAT
DP_AUX+
DP_AUX-
CLK_AUX+
DAT_AUX-
C1
CC-100nF
C2
CC-100nF
C3
CC-100nF
R2
R-10K
R3
R-10K
R6
R-100K
Q2
2N7002
CN1
WDPE-20F5L1BU
DP_LANE0+
DP_LANE0-
DP_LANE1+
DP_LANE1-
DP_LANE2+
DP_LANE2-
DP_LANE3+
DP_LANE3-
CAD
DP_HPD
R5
R-100K
F1
nanoSMDC075F
L1
BLM18PG121SN1
C4
CC-100nF
C5
CC-100nF
Q3
2N7002
R7
R-1M
D3
ESD9X3.3ST5G
R8
R-100K
Q4
2N7002K
C6
CC-100nF
HDMI_HPD#
R9
R-0 /X
U2
NC7S32
R10
R-100K
Q5
2N7002K
R11
R-0 /X
C7
CC-100nF
R12
R-0 /X
DP_HPD#
U4
NC7S32
IP4283CZ10
IP4283CZ10
IP4283CZ10

3.2.3.12 LPC interface signals

According to Qseven® specifications rel. 2.0, on the golden edge finger connector there are 8 pins that are used for implementation of Low Pin Count (LPC) Bus interface.

> **Warning:** Although the Qseven® specification states that pins 185-192 can be used for the implementation of the LPC bus or as 8 GPIOs, this option is intended only for the manufacturers of the modules who are free to choose the option they deem more appropriate.
>
> On the Q7-A36 module, the aforementioned pins have been dedicated to the LPC bus; use of these pins for different implementations other than LPC (i.e. as GPIOs) is therefore not possible.

The following signals are available:

LPC_AD[0÷3]: LPC address, command and data bus, bidirectional signal, +3.3V_S electrical level.

LPC_CLK: LPC Clock Output line, +3.3V_S electrical level. Since only a clock line is available, if it is necessary to connect more LPC devices on the carrier board, then provide for a zero-delay clock buffer to connect all clock lines to the single clock output of Qseven® module.

LPC_FRAME#: LPC Frame indicator, active low output line, +3.3V_S electrical level. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

SERIRQ: LPC Serialised IRQ request, bidirectional line, +3.3V_S electrical level. This signal is used only by peripherals requiring Interrupt support.

3.2.3.13 SPI interface signals

The Intel® Bay Trail family of SOCs offers also one dedicated controller for Serial Peripheral Interface (SPI), which can be used for connection of EEPROMs and Serial Flash devices. This interface does not support platform firmware (BIOS).

SPI interface supports master mode only can support speed up to 15Mbps.

Signals involved with SPI management are the following:

SPI_MOSI: SPI Master Out Slave In, Output from Qseven® module to SPI devices embedded on the Carrier Board. Electrical level +3.3V_S.

SPI_MISO: SPI Master In Slave Out, Input to Qseven® module from SPI devices embedded on the Carrier Board. Electrical level +3.3V_S.

SPI_CLK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +3.3V_S.

SPI_CS0#: SPI Chip select, active low output signal (+3.3V_S electrical level).

3.2.3.14 Power Management signals

According to Qseven® specifications, on the golden edge finger connector there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWGIN: Power Good Input, +5V_S tolerant active high signal. It must be driven on the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

PWRBTN#: Power Button Input, active low, +3.3V_A buffered voltage signal with 10kΩ pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

RSTBTN#: Reset Button Input, active low, +3.3V_A buffered voltage signal with 10kΩ pull-up resistor. This signal can be connected to a momentary push-button: a pulse to GND of this signal will reset the Qseven® module.

BATLOW#: Battery Low Input, active low, +3.3V_A buffered voltage signal with 10kΩ pull-up resistor. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. Can be left unconnected if not used

WAKE#: Wake Input, active low +3.3V_A electrical voltage signal with 10kΩ pull-up resistor and series Schottky diode. This signal can be driven low, on the carrier board, to report that a Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

SUS_STAT#: Suspend status output, active low +3.3V_A electrical voltage signal. This output can be used to report to the devices on the carrier board that the module is going to enter in one of possible ACPI low-power states.

SUS_S3#: S3 status output, active low +3.3V_A electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S5#: S5 status output, active low +3.3V_A electrical voltage signal. This signal is used, on the carrier board, to shut off the power supply to all the devices that must become inactive only during S5 (Soft Off) power state.

SLP_BTN#: Sleep button Input, active low +3.3V_A electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

LID_BTN#: LID button Input, active low +3.3V_A electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

3.2.3.15 Miscellaneous signals

Here following, a list of Qseven® compliant signals that complete the features of Q7-A36 module.

SMB_CLK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_A (but enabled via +3.3V_S voltage) with a 2k2Ω pull-up resistor. It is managed by the SOCs' PCU System Management Bus controller.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_A (but enabled via +3.3V_S voltage) with a 2k2Ω pull-up

resistor. It is managed by the SOCs' PCU System Management Bus controller.

SMB_ALERT#: SM Bus Alert line for System Management. Bidirectional signal, electrical level +3.3V_A with a 10kΩ pull-up resistor. It is managed by the SOCs' PCU System Management Bus controller. Any device place on the SM Bus can drive this signal low to signal an event on the bus itself.

GP0_I2C_CLK: general purpose I2C Bus clock line. Bidirectional signal, electrical level +3.3V_S with a 560Ω pull-up resistor. It is managed by the SOCs' I2C controller #0. I2C Bus is able to work in Standard mode (bitrate up to 100Kbps), Fast mode (bitrate up to 400Kbps), Fast-mode Plus (bitrate up to 1Mbps), High-speed mode (bitrate up to 3.4Mbps).

GP0_I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3.3V_S with a 560Ω pull-up resistor. It is managed by the SOCs' I2C controller #0.

WDTRIG#: Watchdog Trigger Input. It is an active low signal, +3.3V_S voltage, with 1kΩ pull-up resistor. This signal can be used to reset and restart, via Hardware, the internal Watchdog Timer (which is usually managed via Software using Q7-A36 dedicated API - Application Program Interface - libraries).

WDOUT: Watchdog event indicator Output. It is an active high signal, +3.3V_S voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW.

THRM#: Thermal Alarm Input. Active Low +3.3V_S voltage signal with 10kΩ pull-up resistor, directly managed by ST Microelectronics STM32F100R4H6 microcontroller. This input gives the possibility, to carrier board's hardware, to indicate to the main module an overheating situation, so that the SoC can begin thermal throttling.

FAN_TACHOIN: External FAN Tachometer Input. +3.3V_S voltage signal, directly managed by ST Microelectronics STM32F100R4H6 microcontroller.

FAN_PWM_OUT: PWM output for FAN speed management, +3.3V_S voltage signal. It is managed by ST Microelectronics STM32F100R4H6 microcontroller.

SPKR: Speaker output, +3.3V_S voltage signal, directly managed by Intel® Atom™ E38xx SOCs' embedded 8254 Timer.

3.2.3.16 Manufacturing signals

According to Qseven® Standard specifications, rel. 2.0, on pin designed as MFG_NCx (pins 204, 207÷210) are carried the JTAG signal necessary to program Q7-A36 embedded microcontroller.

> **!** The JTAG interface available on MFG_NCx pins is reserved only for the manufacturing phase; **it must not be used by the customer**.
>
> It is not possible at all to use these pins to trace the software (for debug purposes)

3.2.4 BOOT Strap Signals

Configuration straps are signals that, during system reset, are set as inputs (independently by their behaviour during normal operations) in order to allow the proper configuration of the processor / chipset. For this reason, on Q7-A36 are placed the pull-up or pull-down resistors that are necessary to configure the board properly.

The customer must avoid to place, on the carrier board, pull-up or pull-down resistors on signals that are used as strap signal, since it could result in malfunctions of Q7-A36 module.

The following signals are used as configuration straps by the Intel® Bay Trail family of SOCs at system reset.

HDMI_CTRL_DAT: pin 150 of golden finger connector. Normally used as DDC Data line for HDMI panel. Signal at +3.3V_S voltage level with a 2k2Ω pull-up resistor. It is used as a strap signal of Q7-A36 module to configure properly the digital display interface used for HDMI / DVI / DP.

Chapter 4.
BIOS SETUP

- InsydeH2O setup Utility
- Main setup menu
- Advanced menu
- Security menu
- Power menu
- Boot menu
- Exit menu

4.1 InsydeH2O setup Utility

Basic setup of the board can be done using Insyde Software Corp. “InsydeH2O Setup Utility”, that is stored inside an onboard SPI Serial Flash.

It is possible to access to InsydeH2O Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select “SCU” icon.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
<F5> / <F6>	<F5> and <F6> keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows displaying the General Help screen.
<F9>	<F9> key allows loading Setup Defaults for the board. After pressing <F9> BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<F10>	<F10> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows discarding any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow displaying the setup sub- screens.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

4.2.1 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Boot Configuration	See submenu	Configures settings for Boot Phase
PCI Express Configuration	See submenu	PCI Express Configuration Settings
USB Configuration	See submenu	Configures USB Section
Audio Configuration	See submenu	Configures Audio Section
LPSS & SCC Configuration	See submenu	Configures LPSS (Low-Power Sub-System, i.e. DMA, PWM, UART and I2C interfaces) and SCC (Storage Control Cluster) devices
Miscellaneous Configuration	See submenu	Enable / Disable Misc. features
Security configuration (TXE)	See submenu	Trusted Execution Environment Security Configurations
Video Configuration	See submenu	Configures the options for video section
Chipset Configuration	See submenu	Configure Chipset's parameters
SATA Configuration	See submenu	Select the SATA controller and hard disk drive type installed in the system
Console Redirection	See submenu	Configures the parameters for Console redirection
ACPI Table / Features Control	See submenu	Configures the parameters for ACPI management
Super I/O Configuration	See submenu	Super I/O Setup Configuration Utility
Virtual Super I/O Configuration	See submenu	Install legacy UARTs on ACPI aware OS
INT/IRQ Configuration	See submenu	Configures PCI INT and IRQ assignments

4.3.1 Boot configuration submenu

Menu Item	Options	Description
Numlock	On / Off	Allows to choose whether NumLock Key at system boot must be turned On or Off

4.3.2 PCI Express configuration submenu

Menu Item	Options	Description
PCI Express Root Port 0 PCI Express Root Port 1 PCI Express Root Port 2 PCI Express Root Port 3 (internal LAN)	See submenu	

4.3.2.1 PCI Express Root Port #x configuration submenus

Menu Item	Options	Description
PCI Express Root Port #0 PCI Express Root Port #1 PCI Express Root Port #2 PCI Express Root Port #3 (internal LAN)	Disabled / Enabled	Enable or Disable single PCI Express Root Port #x. PCI Express Root Ports #0÷#2 are those routed to Qseven® card edge connector PCI Express Root Port#3 is internally connected to Intel® Gigabit Ethernet Controller I210. Disabling this port will result in disabling Ethernet interface.
PCI Express Port #x Speed	Auto / Gen1 / Gen2	This menu item is available only when corresponding Root Port is set to Enabled. Set PCI-e ports link speed/capability. Not available for PCI Express Root Port #3
PCI Express Port #x ASPM	Disabled / L0s / L1 / L0s & L1 / Auto	This menu item is available only when corresponding Root Port is set to Enabled. Manages PCI Express L0s and L1 power states, for OSs able to handle Active State Power Management (ASPM). Not available for PCI Express Root Port #3

4.3.3 USB configuration submenu

Menu Item	Options	Description
USB BIOS Support	Disabled / Enabled / UEFI Only	Sets the support for USB keyboard / mouse / storage under UEFI and DOS environment. When set to UEFI only, then it will support exclusively UEFI environment.
xHCI Mode	Disabled Enabled Auto Smart Auto Best Auto	Mode of operation of xHCI controller Disabled: USB 3.0 functionalities are always disabled, USB 3.0 devices will work in High Speed Mode Enabled: USB 3.0 functionalities are available both in BIOS and in OS (also for booting, provided that the xHCI driver is installed). Auto: USB 3.0 devices will work only when OS has started, provided that hcSwitch and xHCI drivers are installed. In BIOS and during boot USB 3.0 devices will work in High Speed mode Smart Auto: when starting from a Mechanical Off (G3) state, USB 3.0 functionalities are available both in BIOS and in OS (also for booting, provided that the hcSwitch and xHCI driver is installed). When the system boots from a different ACPI state, USB 3.0 devices will be managed by xHCI or EHCI controller depending on the last used configuration. Best Auto: always route to xHCI
Win7 Uninstall xHCI driver workaround	Disabled / Enabled	Enable / Disable Windows 7 Uninstall xHCI driver workaround. When enabled, Windows 7 USB (EHCI mode) will still work after uninstalling xHCI driver, but the WHCK test will fail
xHCI Controller	Disabled / Enabled	Enable/Disable xHCI Controller for USB 3.0 functionalities support
USB2 Link Power Management	Disabled / Enabled	Can be changed only when “xHCI Controller” is Enabled Enable/Disable the USB2 Link Power Management, i.e. the management of different Link Power (Lx) States of connected USB devices depending on the workload of the device itself.
xHCI Streams	Disabled / Enabled	Can be changed only when “xHCI Controller” is Enabled Enable/Disable the xHCI Stream Support.
EHCI Controller	Disabled / Enabled	Controls the USB EHCI (USB 2.0) functionalities. One EHCI controller must always be enabled.
USB EHCI debug	Disabled / Enabled	Can be changed only when “EHCI Controller” is Enabled Enable / Disable PCH EHCI debug capability
USB Per-Port Control	Disabled / Enabled	Allows to enable / disable singularly each of USB ports #0 ÷ #3
USB Port #0 / USB Port #1 / USB Port #2 / USB Port #3	Disabled / Enabled	Available only when “USB Per-Port Control” is Enabled. Allows to enable / disable individually each USB port
USB Ignore Settings	See Submenu	Allows excluding BIOS support for single USB Devices/Ports/Hosts.

USB Ignore Request Timeout (sec.)	0÷30	When enabled (i.e., timeout greater than zero), for each USB bootable device it is required the user confirmation. Without any action, when the timeout expires the USB device is ignored. If the timeout is set to zero, it means that this feature is disabled, and the boot sequence works in the standard way. When enabled, the Confirm Dialog Box is displayed only for disks with a valid MBR.
Display USB Device's Name	Disabled / Enabled	Available only when "USB Ignore request Timeout (Sec.)" is Set. Allows enabling / disabling the disabling of USB Device's name in the timeout string.

4.3.3.1 USB Ignore Settings submenu

Using this submenu, it is possible to define up to four (4) rules for the USB ports to be ignored from BIOS support, if desired. Each rule will offer the following options:

Menu Item	Options	Description
Host Controller	None / All / Int. xHCI (Usb3.0) / Int. EHCI (Usb2.0)	Select the Host Controller to ignore
Port	None / All / Port 0 / Port 1 / Port 2 / Port 3 / Port 4 / Port 5 / Port 6 / Port 7	Select the USB Port to ignore
USB Class	None / All / HID / Mass Storage	Select the USB Class of Devices to ignore. HID: Touch Controllers, Mouses, Keyboards Mass Storage: USB disks, CD/DVD, Floppy Disks
Vendor ID	0x0001 ÷ 0 x FFFE	Specify the Vendor ID to ignore. 0xFFFF = Ignore All 0xFFFE = Ignore None
Device ID	0x0001 ÷ 0 x FFFE	Specify the Device ID to ignore. 0xFFFF = Ignore All 0xFFFE = Ignore None

! If the BIOS support is excluded for all ports and/or all HID devices, it will be impossible to enter in the Setup Configuration utility using USB keyboards.

Please be careful before changing these settings.

4.3.4 Audio configuration submenu

Menu Item	Options	Description
Audio Controller	Disabled / Enabled	Enable or Disable the HD Audio Controller
VC1 Enable	Disabled / Enabled	Available only when "Audio Controller" is Enabled Enable or Disable Virtual Channel 1 of Audio Controller
HDMI Codec	Disabled / Enabled	Enable or Disable internal HDMI Codec for audio

4.3.5 LPSS & SCC configuration submenu

Menu Item	Options	Description
LPSS & SCC Devices Mode	ACPI Mode PCI Mode	Allows setting the Working mode of LPSS (Low-Power Sub-System) and SCC (Storage Control Cluster) devices. Use PCI mode for Windows® 7, use ACPI mode for Android and Windows® 8
LPSS & SCC Auto Switch	Enable / Disable	Available only when "LPSS & SCC Devices Mode" is set to ACPI Mode. Auto switches LPSS and SCC devices to PCI mode when the OS doesn't support ACPI mode.
Hide unsupported LPSS devices	Enable / Disable	Available only when "LPSS & SCC Devices Mode" is set to ACPI Mode. Hide unsupported LPSS devices when in ACPI mode.
SCC eMMC Boot Controller	Enable / Disable	Disable or enable the eMMC Boot controller against the stepping
eMMC Secure Erase	Enable / Disable	Disable/Enable eMMC Secure Erase. When enabled, all the data on eMMC will be erased.
DDR50 Capability Support	Enable / Disable	Enable or Disable SCC eMMC 4.5 DDR50 support
HS200 Capability Support	Enable / Disable	Enable or Disable SCC eMMC 4.5 DDR50 support
Re Tune Timer Value	0 / 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8 / 9 / 10 / 11 / 12 / 13 / 14 / 15	Can be changed only when "SCC eMMC Boot Controller" is enabled and "DDR50 Capability Support is disabled. Sets the re-tune timer value
SCC SD Card Support	Disabled / Enabled	Enable/ Disable SD Card Support
LPSS DMA #1 Support	Disabled / Enabled	Allows to enable first DMA Channel, which onboard is used to support the UART interface and the SPI Bus
LPSS HSUART #1 Support	Disabled / Enabled	Enable / Disable the UART interface available on Q7 card edge connector
LPSS SPI Support	Disabled / Enabled	Enable / Disable the SPI interface available on Q7 card edge connector
LPSS DMA #2 Support	Disabled / Enabled	Allows to enable second DMA Channel, which onboard is used to support the I2C Channel
LPSS I2C #1 Support	Disabled / Enabled	Enable / Disable the I2C Bus available on Q7 card edge connector

4.3.6 Miscellaneous Configuration submenu

Menu Item	Options	Description
HPET - HPET Support	Enabled / Disabled	If this feature is enabled, the High Precision Event Timer table will be added into ACPI Tables.
Clock Spread Spectrum	Enabled / Disabled	Allows enabling Clock Chip's Spread Spectrum feature.
BIOS Lock	Enabled / Disabled	Enable or disable BIOS SPI region write protect.
PCI MMIO Size	0.75GB 1.5GB 2GB	Setup PCI Memory Mapped IO Space, 0.75GB, 1.5GB or 2GB. Note: to avoid system hangs caused by insufficient memory allocation, reducing this value may lead to the reduction of the IGD aperture size selected in Advanced Menu → Video Configuration submenu.
Memory optimization for 32-bit Windows OS	Enabled / Disabled	When using Windows 32-bit versions, enabling this feature will allow a better memory resource allocation.
PCI Express Dynamic Clock Gating	Enabled / Disabled	Enable or Disable PCI Express Dynamic Clock Gating.
Force Legacy Free	Enable / Disable	When enabled, this item will force the Legacy Free mode (it will disable the KBC).
Serial IRQ	Enabled / Disabled	Enables or disables the Serial IRQ.
Serial IRQ Mode	Quiet Mode Continuous Mode	Select Serial IRQ Mode. In continuous mode, the host will continually check for device interrupts. In Quiet Mode, Host will wait for a SERIRQ slave to generate a request by driving the SERIRQ line low.
Intel I210/I211 Led1	Default Activity	Intel® I210/I211 Gb Ethernet controller LED1 behaviour. Default setting makes LED1 active on link. Setting to "Activity" makes LED1 active only when network traffic is present

4.3.7 Security configuration (TXE) submenu

Please notice that all these items can be modified only with Celeron® SOCs. With Atom™ SOCs, these items cannot be modified.

Menu Item	Options	Description
TXE	Disabled / Enabled	Enable or Disable the Intel® Trusted Execution Engine (TXE, available only on Celeron CPUs)
TXE HMRFP0	Disabled / Enabled	Enable this option to remove temporarily the flash protection, in order to program the Intel® TXE region
TXE Firmware update	Disabled / Enabled	Enable this option to require a re-flashing of TXE Firmware Image
TXE EOP Message	Disabled / Enabled	Send EOP (End of POST) Message before entering OS
TXE Unconfiguration Perform	Yes / No	Only selectable on CPUs with the TXE feature. Allows to revert TXE settings to the factory defaults

4.3.8 Video configuration submenu

Menu Item	Options	Description
VBIOS Selection	Default / Intel ISG Optimized	Allows to select an optimized VBIOS to solve an issue present on Linux Kernels causing video configuration wrong detection.
DDI0	Disabled / Enabled	Enable / Disable DDI0 Video Output
DDI1	Disabled / Enabled	Enable / Disable DDI1 Video Output
Primary Display	DDI0 / DDI1 / None	Select the Primary Display for the use in WEC7 operating System
Secondary Display	DDI0 / DDI1 / None	Select the Secondary Display for the use in WEC7 operating System
Display Mode	Single / Extended / Extended Vertical / Clone	Select the Display Mode for the use in WEC7 operating System
LFP	Custom / 640x480 / 800x480 / 800x600 / 1024x600 / 1024x768 / 1280x720 / 1280x800 / 1280x1024 / 1366x768 / 1400x900 / 1600x900 / 1680x1050 / 1920x1080	Select a software resolution (EDID settings) to be used for the internal flat panel.
LFP Custom parameters	See submenu	Only available when “LFP” is set to Custom. Select Detailed Timing Descriptor Parameters
LFP Color Mode	VESA 24bpp JEIDA 24bpp 18 bpp	Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.
LFP Interface	Single Channel Dual Channel	Allows configuration of LVDS interface in Single or Dual channel mode
LFP Default brightness (%)	0 ÷ 100	LFP Default brightness percentage. Valid values are in the range 0-100, where 0 means backlight OFF. This setup configuration, during the BIOS boot, is valid only with a single LFP connected (no multi-monitor).
LFP Max ACPI Brightness (%)	0 ÷ 100	Maximum ACPI Brightness percentage allowed with an ACPI aware OS
LVDS Advanced Options	See Submenu	LVDS Advanced Options Configurations
Integrated Graphics Device	Disabled / Enabled	Enabled: enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disabled: always disable IGD. **Warning:** when the IGD is disabled, there will be no video output at all (unless there is an external PCIe graphic card selected as Primary Display) and restoring BIOS options to default values will be possible only by moving blindly in the setup menu.

Primary Display	Auto / IGD / PCIe	Select which of IGD or external PCI-e Graphic Controller should be the Primary display
RC6(Render Standby)	Disabled / Enabled	Permits to enable the render standby features, which allows the onboard graphics entering in standby mode to decrease power consumption
PAVC	Disabled / LITE Mode / SERPENT Mode	Allows enabling the hardware acceleration of decoding of Protected Audio Video streams. When not disabled, it is possible to choose between LITE encryption and SERPENT encryption modes.
Power Management Lock	Disabled / Enabled	Enable / Disable Power Management Lock
DOP CG	Disabled / Enabled	Enable / Disable DOP Clock Gating
GTT Size	1MB / 2MB	Select the GTT (Graphics Translation Table) Size
Aperture Size	128MB / 256MB / 512MB	Use this item to set the total size of Memory that must be left to the GFX Engine
IGD - DVMT Pre-Allocated	64M / 96M / 128M / 160M / 192M / 224M / 256M / 288M / 320M / 352M / 384M / 416M / 448M / 480M / 512M	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphic Device
IGD - DVMT Total Gfx Mem	128M / 256M / MAX	Select the size of DVMT (Dynamic Video Memory) 5.0 that the Internal Graphics Device will use
IGD Turbo	Auto / Enabled / Disabled	Enable or Disable IGD Turbo mode
IGD Thermal	Disabled / Enabled	Enabled or disable Thermal Control of IGD
Spread Spectrum clock	Disabled / Enabled	Enable or disable Spread Spectrum Clock on DDI interface
Backlight Control	Auto PWM-Inverted PWM-Normal	Backlight control setting

4.3.8.1 LFP Custom submenu

Using this submenu, it is possible to set all the following parameters to meet the LVDS display requirements.

Menu Item	Options	Description
Pixel Clock / 10000	Any value in range [2500..22400]	Working Frequency in 10kHz units, e.g 6350 → 63.5MHz. Allowed range from 2500 (25MHz) to 22400 (224MHz)
Horizontal Active	Any value in range [1..4095]	Horizontal Addressable Video in pixels, a.k.a. Horizontal resolution (e.g. 1024 on a 1024x768 LFP)
Horizontal Blank	Any value in range [1..4095]	Horizontal Blanking in pixels, equals to Horizontal Total (Horizontal Active + Horizontal Front Porch + Horizontal Black Porch)
Vertical Active	Any value in range [1..4095]	Vertical Addressable Video in pixels, a.k.a. Vertical resolution (e.g. 768 on a 1024x768 LFP)
Vertical Blank	Any value in range [1..4095]	Vertical Blanking in pixels, equals to Vertical Total (Vertical Active + Vertical Front Porch + Vertical Black Porch)
Horizontal Offset	Any value in range [1..1023]	Horizontal Front Porch in pixels
Horizontal Pulse	Any value in range [1..1023]	Horizontal Sync Pulse Width in pixels
Vertical Offset	Any value in range [1..63]	Vertical Front Porch in pixels
Vertical Pulse	Any value in range [1..63]	Vertical Sync Pulse Width in pixels
Horizontal Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)
Vertical Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)

4.3.8.2 LVDS Advanced options submenu

Using this submenu, it is possible to set all the following parameters to meet the LVDS display requirements.

Menu Item	Options	Description
LVDS Spreading Depth	No Spreading / 0.5% / 1.0% / 1.5% / 2.0% / 2.5%	Sets percentage of bandwidth of LVDS clock frequency for spreading spectrum
LVDS Output Swing	150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV / 450 mV	Sets the LVDS differential output swing
T3 Timing	0 ÷ 255	Minimum T3 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 10 (500ms)
T4 Timing	0 ÷ 255	Minimum T4 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 2 (100ms)
T12 Timing	0 ÷ 255	Minimum T12 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 20 (1s)
T2 Delay	Enabled / Disabled	When Enabled, T2 is delayed by 20ms ± 50%
T5 Delay	Enabled / Disabled	When Enabled, T5 is delayed by 20ms ± 50%
P/N Pairs Swapping	Enabled / Disabled	Enable or disable LVDS Differential pairs swapping (Positive ⇔ Negative)
Pairs Order Swapping	Enabled / Disabled	Enable or disable channel differential pairs order swapping (A ⇔ D, B ⇔ CLK, C ⇔ C)
LVDS BUS Swapping	Enabled / Disabled	Enable or disable Bus swapping (Odd ⇔ Even)

4.3.9 Chipset configuration submenu

Menu Item	Options	Description
ISP Enable / Disable	Disabled / Enabled	Enable/Disable ISP PCI Device Selection
ISP PCI Device Selection	Disabled ISP PCI Device as B0D2F0 ISP PCI Device as B0D3F0	Select PCI B0D2F0 for Windows OS. Select B0D3F0 for other OS (Linux)
PCI 64-bit Decode	Enabled / Disabled	Allow system to support 64-bit BAR (Base Address Register) for PCI devices.
CRID	Enabled / Disabled	Enable / Disable CRID (Configured Revision ID) register.

4.3.10 SATA configuration submenu

Menu Item	Options	Description
SATA Controller	Enabled / Disabled	Disabled: Disables SATA Controller. All following items will be disabled Enabled: Enables SATA Controller
Sata Port 0	Enabled / Disabled	Enables or disable SATA Port #0
Sata Port 1	Enabled / Disabled	Enables or disable SATA Port #1
Chipset SATA Mode	IDE AHCI	Set SATA Configuration type With AHCI, is not possible to install/boot UEFI O.S., only Legacy OS can be installed (a simpler driver is required). Setting to IDE, the controller is managed as a PCI device, so addresses reallocation and INT line sharing is possible.
SATA Speed	Gen1 / Gen2	Select SATA speed
SATA Port 0 Hot Plug Capability SATA Port 1 Hot Plug Capability	Enabled / Disabled	These items will be available only when “Chipset SATA Mode” is set to AHCI. If enabled, SATA port will be reported as Hot Plug Capable
IDE Max Transfer Mode	Auto Ultra ATA/100 Ultra ATA/66 Ultra ATA/33 PIO Mode	This item will be available only when “Chipset SATA Mode” is set to IDE. Sets the IDE Interfaces’ maximum Transfer Rate
IDE Mode	Native IDE Legacy IDE	This item will be available only when “Chipset SATA Mode” is set to IDE. Sets the IDE Working Mode
Serial ATA Port 0 / 1		Shows information related to eventual devices connected to SATA ports 0 or 1

4.3.11 Console Redirection submenu

Menu Item	Options	Description
Console Serial Redirect	Enabled / Disabled	Enable or disable Console redirection. When enabled, all the submenus of the following paragraph will appear
Terminal Type	VT_100 / VT_100+ / VT_UTF8 / PC_ANSI	Set Console Redirection terminal type
Baud rate	115200 / 57600 / 38400 / 19200 / 9600 / 4800 / 2400 / 1200	Set Console Redirection baud rate
Data Bits	7 bits / 8 bits	Set Console Redirection data bits
Parity	None / Even / Odd	Set Console Redirection parity bits
Stop Bits	1 bit / 2 bits	Set Console Redirection stop bits
Flow Control	None RTS/CTS XON/XOFF	Set Console Redirection flow control type
Information Wait Time	0 Seconds / 2 Seconds / 5 Seconds / 10 Seconds / 30 Seconds	Set Console Redirection port information display time
C.R. After Post	Yes / No	Console Redirection continues to work even after Bios POST.
AutoRefresh	Enabled / Disabled	When this feature is enabled, the screen will auto refresh once after detecting the connection of a remote terminal
FailSafeBaudRate		This feature will auto detect remote terminal baud rate and connect C.R serial device with detected baud rate
ACPI SPCR Table	Enabled / Disabled	Serial Port Console Redirection Table. When this feature is enabled, the SPCR table will be add-into ACPI tables.
Serial Port 0 - *Addr* IRQy Serial Port 1 - *Addr* IRQy Serial Port 2 - *Addr* IRQy Serial Port 3 - *Addr* IRQy	See following menu items	These voices will be available only when Console Serial Redirect is Enabled and if at least one LPC Super I/O is present on the carrier board. Depending on the SuperI/O(s) found on the carrier board, this item will show the serial ports that are available, with their address and IRQ (assigned). For each port it will be possible to set the paramters shown in the following lines
PortEnable	Enable / Disabled	Enable / Disable single serial Port x for the console redirection
UseGlobalSetting	Enable / Disaled	Use or not global settings for Serial Port x for the console Redirection

Terminal Type	VT_100 / VT_100+ / VT_UTF8 / PC_ANSI	Set Console Redirection terminal type
Baud rate	115200 / 57600 / 38400 / 19200 / 9600 / 4800 / 2400 / 1200	Set Console Redirection baud rate
Data Bits	7 bits / 8 bits	Set Console Redirection data bits
Parity	None / Even / Odd	Set Console Redirection parity bits
Stop Bits	1 bit / 2 bits	Set Console Redirection stop bits
Flow Control	None RTS/CTS XON/XOFF	Set Console Redirection flow control type

4.3.12 ACPI Table/features submenu

Menu Item	Options	Description
FACP - RTC S4 wakeup	Enabled / Disabled	Enable or disable FACP (Fixed ACPI Description Table) support for S4 wakeup from RTC
FACP - Sleep Button	Enabled / Disabled	Enable or disable the FACP flag for the Sleep Button.
DSDT - ACPI S3	Enabled / Disabled	Enable or disable DSDT (Differentiated System Description Table) support for ACPI S3 State
DSDT - ACPI S4	Enabled / Disabled	Enable or disable DSDT (Differentiated System Description Table) support for ACPI S4 State
BGRT - ACPI BGRT	Enabled / Disabled	Enable or disable the support for ACPI Boot Graphics Resource Table

4.3.13 SuperI/O configuration submenu

Menu Item	Options	Description
Name of the SuperI/O found		This menu item will show the name of all the Super I/Os that are found on the carrier board. By selecting the adequate SuperI/O, it will be possible to set the serial ports and possibly other parameters as shown in the following menu items. If no Super I/O is available on the Carrier Board, this menu will not be available.
Keyboard Controller	Enabled / Disabled	Enable / disable the Keyboard Controller (if the SuperI/O supports it, otherwise this item will not be available).
Serial Port 1 / Serial Port 2 / Serial Port 3 / Serial Port 4	Enabled / Disabled	Enable or Disable single serial port #1, #2, #3 or #4 (the number of serial ports depends on the Super I/O).
Address	0x3F8 / 0x2F8 / 0x3E8 / 0x2E8 / 0x3E0 / 0x2E0 / 0x338 / 0x238 / 0x220 / 0x228	Select the Base address for each Serial Port, if enabled.
IRQ	3 / 4 / 5 / 6 / 7 / 10 / 11 / 14 / 15	Select the IRQ line to assign to each Serial Port, if enabled.
Floppy Disk Controller	Enabled / Disabled	Enable / disable the Floppy Disk Controller, if the SuperI/O supports it
Parallel Port Mode	Parallel Port / External FDC	Configure the Parallel Port mode of working, if the SuperI/O supports it
LPT Port	Enabled / Disabled	When the previous item is set to “Parallel Port”, this item will allow to enable or disable the LPT port.
LPT Mode	SPP / EPP 1.9 and SPP / ECP / ECP-EPP 1.9 / Printer Mode / EPP 1.7 and SPP / ECP-EPP 1.7	When the LPT port is enabled, this item will allow to configure the LPT protocol
LPT Irq	Disabled / 5 / 7	When the LPT port is enabled, this item will allow to configure the LPT IRQ
Hardware Monitor	Enabled / Disabled	Enable or disable the Super I/O Hardware monitor (if it is supported by the Super I/O)
Watchdog	Disabled / 1 Minute / 2 Minutes / 3 Minutes	Enable or Configure the Super I/O Watchdog (if the Super I/O Used supports it, otherwise this item will not be available)

4.3.14 Virtual SuperI/O configuration submenu

Menu Item	Options	Description
Address	Disabled / 0x3F8 / 0x2F8 / 0x3E8 / 0x2E8 / 0x3E0 / 0x2E0 / 0x338 / 0x238 / 0x220 / 0x228	Select the Base address for each virtual Serial Port, or disable it
IRQ	Disabled / 3 / 4 / 5 / 6 / 7 / 10 / 11 / 14 / 15	Select the IRQ line to assign to each Serial Port, if enabled.

4.3.15 INT/IRQ configuration submenu

Menu Item	Options	Description
INT A Irq / INT B Irq / INT C Irq / INT D Irq / INT E Irq / INT F Irq / INT G Irq / INT H Irq	3 / 4 / 5 / 6 / 7 / 10 / 11 / 14 / 15	Allows the selection of the IRQ o be assigned to single PCI INT lines

4.4 Security menu

Menu Item	Options	Description
Select TPM Device	Disabled TPM 1.2 TPM 2.0	Allow to disable or configure properly optional external TPM devices interfaced to LPC Bus on the Carrier Board
Set Supervisor Password		Install or Change the password for supervisor. Length of password must be greater than one character.
Power on Password	Enabled / Disabled	Available only when Supervisor Password has been set. Enabled: System will ask to input a password during P.O.S.T. phase. Disabled: system will ask to input a password only for entering Setup utility
User Access Level	Full View Only	View Only: Access to BIOS Setup allowed but the fields cannot be changed. Full: Any Field can be changed except the Supervisor Password
Set User Password		Install or Change the password for the users. Length of password must be greater than one character.
USB Disks Signature Option	See Submenu	Allow to enable or disable USB boot from signed USB disks only

4.4.1 USB Disk Signature Option submenu

Menu Item	Options	Description
USB Disks Signature Check	Enabled / Disabled	Enable the USB disk signature check. When enabled, if the USB disk used is not signed it will be removed from the boot devices list.
One Time Signature Check Disable	Enabled / Disabled	USB disk signature check one-time disable. When enabled, for the next boot (and only for that) the USB disk signature check will be automatically disabled.
Signature Byte 0 / Signature Byte 1 / Signature Byte 2 / Signature Byte 3	0 ÷ 255	Set the value for byte 0 / 1 / 2 / 3 of USB disks signature. The disk's signature check is always on 4 bytes.
USB Password	State Unknown / Installed / Not Installed	This item shows the state of USB Disk Password for Boot
Set USB Disks Password		When a USB Disk password is set, the system will first check if the USB disk is signed. If it is not signed, then the system will ask for a password, in order to continue booting from the USB disk.

4.5 Power menu

Menu Item	Options	Description
Advanced CPU Control	See submenu	These items control various CPU parameters
EC Watchdog configuration	See submenu	Embedded Controller Watchdog Configuration Settings
Thermal Zone configuration	See submenu	Thermal Zone Configuration: Active and Passive Cooling Settings.
Wake on PME	Enabled / Disabled	Determines whether the system must wake up or not when the system power is off and occurs a PCI Power Management Enable wake-up event (e.g. to enable Wake on LAN feature).
Auto Wake on S5	Disabled By Every Day By Day of Month	Auto Wake from Soft Off State. It can be set to wake every day at the same hour, or only a precise Day of Month
Wake from S5 time	hh:mm:ss	Only available when Auto Wake on S5 is not set to disabled. Allows selecting the exact hour, minute and seconds for the automatic wake of the board
Day of Month	0 ÷ 31	Only available when Auto Wake on S5 is set to By Day of Month. Allows selecting the day of month when the automatic wake must occur
LID_BTN# Configuration	Force Open Force Closed Normal Polarity Inverted Polarity	Configure LID_BTN# Signal as always open or closed (i.e., Force Open / Force Closed), no matter the pin level, or configures the signal polarity: “Normal Polarity” means the signal goes High when open, “Inverted Polarity” means the signal goes Low when open
LID_BTN# Wake Configuration	No Wake Only From S3 Wake From S3/S4/S5	This item can be changed only when “LID_BTN# Configuration” is not set to Force Open or Force Closed. Configure LID_BTN# Wake capability. According to the pin configuration, when the LID is open it can cause a system wake from a sleep state
SMB_ALERT# wake	Enabled / Disabled	Enable the wake from S3 on SM Bus Alert# activation
Power Fail Resume Type	Always ON Always OFF Last State	Determine the System Behavior after a power failure event. In case the option is “Always ON”, the board will start every time the power supply is present. When the option is “Always OFF”, the board will not start automatically when the power supply returns. Finally, if this option is set to “Last State”, the board will remember the state it had when the power supply went down: so, if the board was on, it will start again when the power returns, and will remain off if the board was in this state when the power went down.
ACPI Power off management	Enabled / Disabled	When enabled, the board will automatically switch itself to S5 state after OS shutdown. When disabled, a manual Power off is required

4.5.1 Advanced CPU control submenu

Menu Item	Options	Description
Use XD Capability	Enabled / Disabled	Enable or disable processor XD (Execute Disable) capability, it allows to enable or disable the hardware feature needed for data execution prevention
Limit CPUID Max Value	Enabled / Disabled	Set this option to enabled for use with older O.S. that are not able to manage the CPUID value higher than 03h, which was typical for Intel® Pentium 4 with Hyper Threading Technology Leave disabled for newer O.S. able to manage actual CPUID value.
Bi-Directional PROCHOT#	Enabled / Disabled	PROCHOT# is the signal used to start thermal throttling. This signal can be driven by any processor cores' to signal that the processor will begin thermal throttling. If bi-directional signaling is enabled, then external components can also drive PROCHOT# signal in order to start throttling.
VTX-2	Enabled / Disabled	Enable or Disable Intel® Virtualization Technology, allowing hardware-assisted virtual machine management.
TM1 and TM2	Enabled / Disabled	Enable or Disable TM1 and TM2 Thermal management modes.
AESNI Feature	Enabled / Disabled	Enable or Disable AESNI (Advanced Encryption Standard New Instructions) set of instructions, which are used to improve the speed of applications performing encryption and decryption using the Advanced Encryption Standard (AES).
Active Processor Cores	1 / 2/ 3 / ALL	Number of cores to enable in each processor package. 1 means that multicore processing is disabled.
P-States (IST)	Enabled / Disabled	Enable or disable processor management of performance states (P-states)
Boot Performance Mode	Max Performance Low Power	Only available when P-states are enabled Allows to select which performance state must be set by BIOS before starting OS loading.
Turbo Mode	Auto / Enabled / Disabled	Only available when P-states are enabled Enable processor Turbo Mode
Force CPU Speed	Disabled *List of speeds supported by the SoC used*	Only available when P-states are enabled Force CPU speed After boot. When this feature is enabled, P-State APCI Table will be disabled. The list of the speeds shown depends on the SoC mounted on the module
C-States	Enabled / Disabled	Enable processor idle power saving states (C-States).
Max C-States	C1 / C6 / C7	Allows selection of the maximum C-State that must be supported by the OS.

4.5.2 EC Watchdog Configuration submenu

Menu Item	Options	Description
Watchdog	Enabled / Disabled	Enable or Disable the Watchdog
Watchdog Action	System reset Power Button 1s Power Button 4s (shutdown)	This submenu is available only when “Watchdog” is set to Enabled. Specifies the action that must be performed when Watchdog timeout occurs. With System Reset, the module will reset itself With “Power Button 1s”, the system will simulate the pressure for 1 sec. of Power button, which will lead the O.S. to close all his tasks then shutdown. With “Power Button 4s”, the system will simulate the pressure for 4 secs. of Power button, which will lead to the immediate shutdown of the module
Delay to start (sec.)	0 ÷ 600	This item can be changed only when “Watchdog” is enabled. Seconds of delay before the watchdog timer starts counting
Timeout (sec.)	20 ÷ 600	This item can be changed only when “Watchdog” is enabled. Watchdog Timeout.

4.5.3 Thermal Zone configuration (TjMax = 110 °C) submenu

Menu Item	Options	Description
Critical temperature (°C)	95 / 100 / 105 / 110 / 115	Use this item to set the maximum temperature that the CPU can reach. Above this temperature value, the system will perform a critical shutdown
Passive Cooling temperature (°C)	70 / 75 / 80 / 85 / 90	Use this item to set the temperature threshold for the CPU. Above this threshold, an ACPI aware OS will start to lower the CPU frequency.
AC0 Temperature (°C)	50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100 / 105 / 110 / 115	Select the highest temperature above which the onboard fan must work always at Full Speed
AC1 Temperature (°C)	25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100 / 105 / 110 / 115	Select the lowest temperature under which the onboard fan must be OFF.
FAN Duty Cycle (%) Above AC1	50 / 75 / 100	Use this item to set the Duty Cycle for the fan when the CPU temperature is between AC1 and AC0 threshold. Above AC0, the fan will run at full speed.

4.6 Boot menu

Menu Item	Options	Description
Boot type	Dual boot Type Legacy Boot Type UEFI Boot Type	Allows to select if the OS must be booted using Legacy Boot Mode, UEFI Boot mode or indifferently using both modalities (depending on the OS)
Quick Boot	Enabled / Disabled	Skip certain tests while booting. This will decrease the time needed to boot the system.
Quiet Boot	Enabled / Disabled	Disables or enables booting in Text Mode.
Display ESC Key Strings	Enabled / Disabled	Display or Hide the “ESC key” strings during the BIOS boot. Disabling this configuration, no information on how to enter Setup Configuration Utility will be displayed.
Display Boot Logo	Enabled / Disabled	Enable or display the visualization of a logo during Boot phase
Logo persistence Time (s)	0 ÷ 10	This submenu is available only when “Display Boot Logo” is set to Enabled. Forced wait time in seconds during the boot logo visualization. 0 means boot as fast as possible. Even with 0 wait time. UEFI OSes supporting BGRT table will display the logo while booting.
Network Stack	Enabled / Disabled	This submenu is available only when “Boot Type” is set to “UEFI Boot type” or “Dual Boot type”. When enabled, this option will make available the following Network Stack services: UEFI IPv4 PXE Legacy PXE OpROM
PXE Boot Capability	Disabled UEFI: IPv4 Legacy	This submenu is available only when “Network Stack” is Enabled Specifies the PXE (Preboot Execution Environment) Boot possibilities. When Disabled, Network Stack is supported For UEFI, it supports IPv4 In Legacy mode, only Legacy PXE OpROM is supported
PXE Boot to LAN	Enabled / Disabled	This submenu is available only when “Boot Type” is set to “Legacy Boot type”. Disables or enables the possibility for the PXE to perform the boot from LAN.
Power Up in Standby Support	Enabled / Disabled	Disable or enable Power Up in Standby Support. The PUIS feature set allows devices to be powered-up in the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.
Add Boot options	First / Last / Auto	Specifies the position in Boot Order for Shell, Network and Removable Disks
ACPI selection	Acpi1.0B / Acpi3.0 / Acpi4.0 / Acpi5.0	Using this menu item is possible to select to which specifications release the ACPI tables must be compliant.

CD/DVD Rom Boot	Enabled / Disabled	Disables or enables booting from CD/DVD
Floppy Disk Boot	Enabled / Disabled	Disables or enables booting from Floppy Disks.
USB Boot	Enabled / Disabled	Disables or enables booting from USB boot devices.
EFI/Legacy Device Order	EFI device first Legacy device first Smart Mode	This submenu is available only when “Boot Type” is set to Dual Boot Type. Determine if boot must happen first through EFI devices or through legacy devices, or in Smart Mode.
Windows® 8 Fast Boot	Enabled / Disabled	This submenu is available only when “Boot Type” is set to UEFI Boot Type. If enabled, the system firmware does not initialize keyboard and check for firmware menu key.
USB Hot Key Support	Enabled / Disabled	Available only when “Boot Type” is set to UEFI Boot Type and “Windows® 8 Fast Boot” is Enabled. Enable or disable the support for USB HotKeys while booting. This will decrease the time needed to boot the system
Timeout	0 ÷ 60	The number of seconds that the firmware will wait before booting the original default boot selection.
Reset On No Boot Device Found	Enabled / Disabled	When this option is enabled, the system will reset itself each time that doesn’t find any valid boot device, instead of waiting indefinitely that a Boot device is plugged.
Touch Controller To Enter SCU	Enabled / Disabled	When this option is enabled, it will be possible to use a Touch screen to enter the Setup Configuration Utility, avoiding using additional external keyboard. The Touch detection will be used as hotkey
Legacy Device Fixed Order	Enabled / Disabled	Disable or enable fixed boot order for physical devices. Takes effect at the next boot of the board
Fixed Legacy Boot Order Settings	See Submenu	This submenu is available only when “Legacy Device Fixed Order” is enabled. Allows fixing the boot order by physical devices.
EFI	See Submenu	This submenu is available only when “Boot Type” is not set to “Legacy Boot type”. The submenu will show a list of EFI boot devices. Use F5 and F6 key to change order for boot priority.
Legacy	See Submenu	This submenu is available only when “Boot Type” is not set to “UEFI Boot type”. Allows setting of Legacy Boot Order

4.6.1 Fixed Legacy Boot Order submenu

Menu Item	Options	Description
First / Second / Third / Fourth / Fifth / Sixth / Seventh	LAN / EHCI / XHCI / SATA0 / SATA1 / eMMC / SD / NONE	Allows selecting the boot order of the possible boot devices. If it is necessary to force the boot from a specific device only, please set is as a first boot device, and set to NONE all other devices.

4.6.2 Legacy submenu

Menu Item	Options	Description
Boot Menu	Normal / Advance	When set to Normal, this submenu will allow configuring all possible options for Legacy boot. When set to Advance, it will be possible to configure Boot Order only for bootable devices found in the system
Boot Type Order	Floppy Drive / Hard Disk Drive CD/DVD-ROM Drive / USB / Other	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will allows selecting the boot from different devices. Use the + and - Keys to change the boot order priority
Hard Disk Drive	*List of HD Drives found connected*	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will show different Disk drives found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority
USB	*List of USB Disks found connected*	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will show different USB disks found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority

4.7 Exit menu

Menu Item	Options	Description
Exit Saving Changes		Exit system setup after saving the changes. F10 key can be used for this operation.
Save Change Without Exit		Save all changes made, but doesn't exit from setup utility.
Exit Discarding Changes		Exit system setup without saving any changes. ESC key can be used for this operation.
Load Optimal Defaults		Load Optimal Default values for all the setup items. F9 key can be used for this operation.
Load Custom Defaults		Load Custom Default values for all the setup items.
Save Custom Defaults		Save Custom Default values for all the setup items.
Discard Changes		Discard Changes but doesn't exit from setup utility.

Chapter 5.
Appendices

- Thermal Design

5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like Q7-A36 module, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

Qseven® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the Qseven® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsinks in some situation can represent the cooling solution. Indeed, when using Q7-A36 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide Q7-A36 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
QA36-DISS-1-PK	Q7-A36 Heat Spreader (Passive)
QA36-DISS-2-PK	Q7-A36 Heatsink (Passive)
QA36-DISS-3-PK	Q7-A36 Active Heatsink with FAN

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