Qseven

User Manual

Q7-928

Qseven® Rel. 2.0 Compliant
Module with NXP i.MX6 Processor

SECO

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	16th November 2012	First Release	SB
1.1	7th May 2013	Introduction and Technical features revised; Block Diagram updated Power consumption added; Qseven® golden finger pinout updated	SB
2.0	30th September 2013	New manual release	SB
2.1	22nd November 2013	Minor corrections; Technical features updated: number of independent displays and LVDS max resolutions updated; Supported Operating Systems added. Limitation about PCI express support added. Pull-up resistors indicated on signals UART0_RX and UART0_CTS#. Corrected pull-up to pull-down on WDOUT signal description	SB
2.2	14th January 2014	LVDS resolution combinations corrected (par. 3.2.3.8)	SB
2.3	6th May 2014	µSD card slot warning added (par 3.2.2); LVDS resolution combinations corrected (par. 3.2.3.8); SUS_S4# signal name changed to SUS_S5# SDIO_PWR Signal added in Qseven golden card edge connector's pinout Minor corrections about signal names in paragraph 3.2.3.15	SB
2.4	10th July 2014	Added I2C table in par. 3.2.3.14	SB
2.5	30th July 2014	Heatspreader and heatsink description updated in par. 4.1	SB
2.6	29th May 2015	Qseven® connector's pins 125, 127 description corrected	SB
2.7	29th October 2015	UART0_RTS# and UART0_CTS# signals removed from Qseven® connector's pins 172, 178. Paragraph 3.2.3.2 updated consequently	SB
3.0	26th January 2016	Product Name change	SB

Every effort has been made to ensure the accuracy of this manual. However, SECO S.r.l. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.r.l. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist you.

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INTRODUCTION

- Warranty
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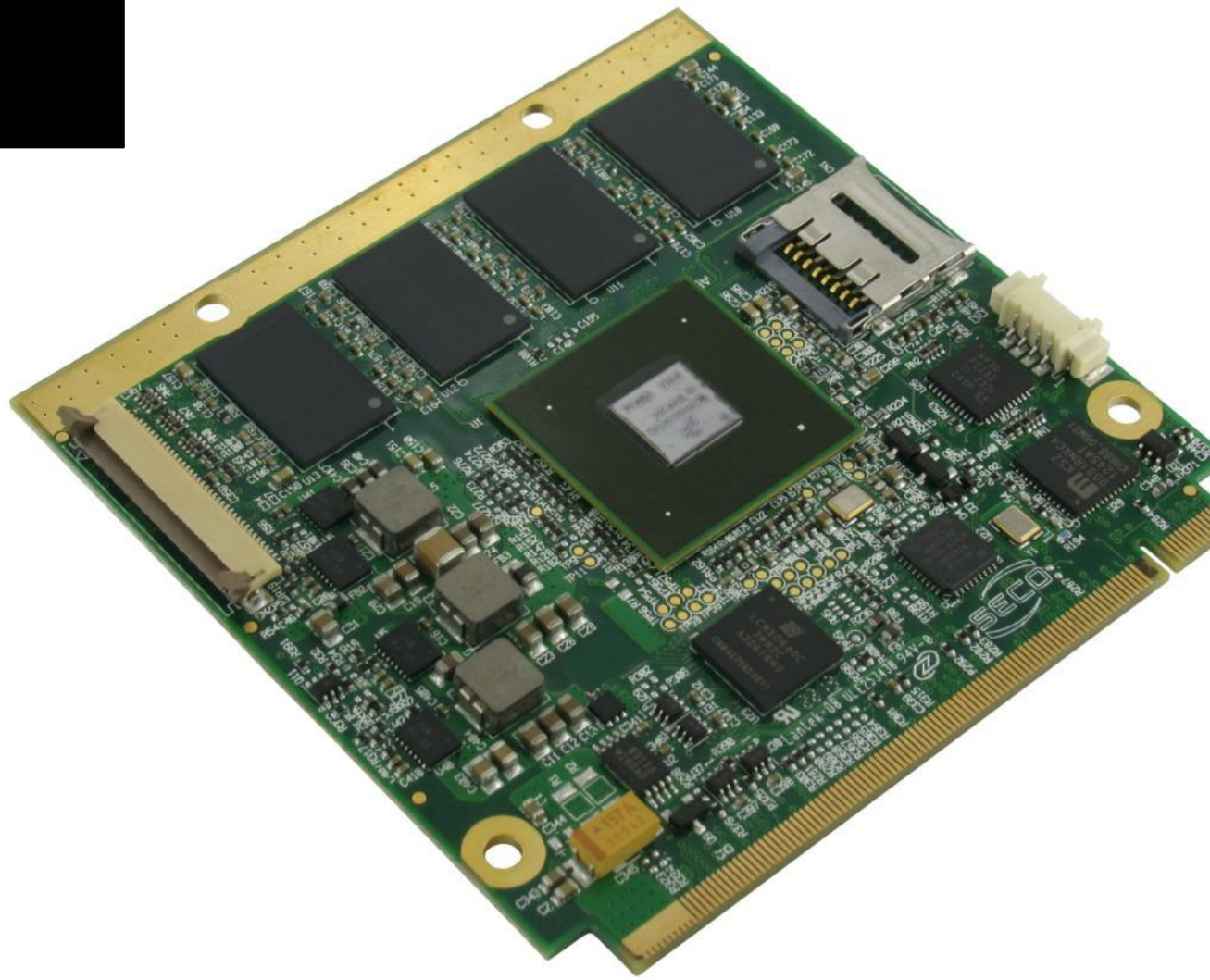


1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.r.l. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.r.l. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The Q7-928 module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!**
>
> Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.
>
> Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The Q7-928 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!**
>
> Whenever handling a Q7-928 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The Q7-928 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

AC'97	Audio Codec'97, a standard for audio hardware codecs developed by Intel® in 1997
ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management.
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control.
CPLD	Complex Programmable Logic Device, a type of programmable logical device with complexity lower than that of FPGAs
CSI2	MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host processor
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
DDR3	DDR, 3rd generation
DVI	Digital Visual interface, a type of display video interface
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
FPGA	Field-programmable gate array, a device designed to be fully programmed by customers in order to implement different functionalities.
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
JTAG	Joint Test Action Group, common name of IEEE1149.1 standard for testing printed circuit boards and integrated circuits through the Debug port.
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals like PS/2, LPT and COM ports
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
MAC	Medium Access Controller, the hardware implementing the Data Link Layer of ISO/OSI-7 model for communication systems
Mbps	Megabits per second

MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenCL	Open Computing Language, a software library based on C99 programming language, conceived explicitly to realise parallel computing using Graphics Processing Units (GPU)
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port.
PCI-e	Peripheral Component Interface Express
PHY	Abbreviation of Physical, it is the device implementing the Physical Layer of ISO/OSI-7 model for communication systems
PWM	Pulse Width Modulation
PWR	Power
RGMII	Reduced Gigabit Media Independent Interface, a particular interface defining the communication between an Ethernet MAC and a PHY
SATA	Serial Advance Technology Attachment, a differential full duplex serial interface for Hard Disks.
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
USB	Universal Serial Bus
uSDHC	Ultra Secure Digital Host Controller
V_REF	Voltage reference Pin

1.8 Reference specifications

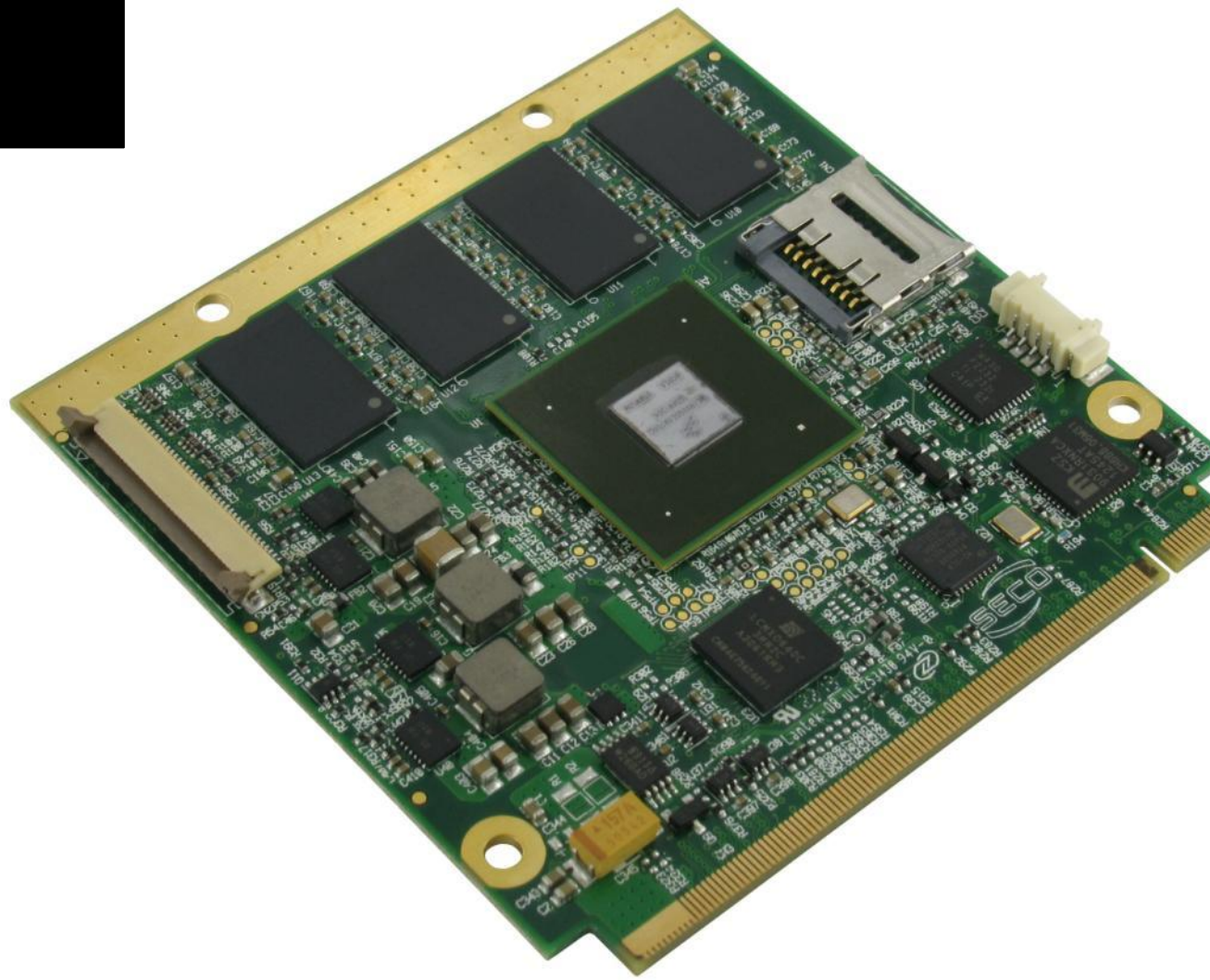
Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
AC'97	http://download.intel.com/support/motherboards/desktop/sb/ac97_r23.pdf
ACPI	http://www.acpi.info
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
CSI	http://www.mipi.org/specifications/camera-interface
DDC	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
JTAG	http://standards.ieee.org/develop/wg/Boundary_Scan_Architecture.html
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
OpenCL	http://www.khronos.org/opencl
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
Qseven® Design Guide	http://www.sget.org/uploads/media/Qseven_Design_Guide_2_0.pdf
Qseven® specifications	http://www.sget.org/uploads/media/Qseven-Spec_2.0_SGET.pdf
SATA	https://www.sata-io.org

SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
USB	http://www.usb.org/developers/docs/usb_20_070113.zip
NXP i.MX6 processor	http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/i.mx-applications-processors-based-on-arm-cores/i.mx-6-processors:IMX6X_SERIES

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram



2.1 Introduction

Q7-928 is a CPU module, in Qseven® format, based on embedded NXP i.MX6 processor, an ARM® Cortex®-A9 processor, Single-, Dual- and Quad-Core, with frequencies up to 1.2GHz, which is ideal for applications requiring multimedia capabilities and/or high levels of parallel computing.

Along with programmable CPLD Lattice LCMXO640, the board offers a very high level of integration, both for all most common used peripherals in ARM world and for bus interfaces normally used in x86 world, like PCI-Express and S-ATA.

All this comes out in the extremely reduced space offered by Qseven® boards, which offers all functionalities of standard boards in just 70x70mm.

This solution allows combining the advantages of a standard, ready-to-use board, like Qseven® boards are, with all advantages offered by ARM application specific processors like NXP i.MX6 processor, in its different versions (Single Core, Dual Core, Dual Core Lite, Quad Core)

Moreover, NXP i.MX6 processors integrates three separated accelerators for 2D, OpenGL® ES2.0 3D and OpenVG™, giving the processor incredible graphical performances (OpenVG™ accelerator is not available with i.MX6 Solo and Dual Lite processors).

The board is completed with up to 4GB DDR3 (up to 2GB with i.MX6 Solo) directly soldered on board, and one eMMC Flash Disk, directly accessible like any standard Hard Disk, with up to 32GB of capacity.

The board can support up to three independent displays using dedicated video interfaces of the module: the first one, is a 24 bit Single/Dual Channel LVDS interface, which can be configured to work as two independent 24 bit Single Channel interfaces. The other display interface is i.MX6's native HDMI port. Please be aware that using i.MX6 Solo and i.MX6 Dual Lite processors, only two independent displays at a time are supported.

HW video decoding, in the most common video coding standards (i.e., H.264, MPEG2, MPEG4, DivX, RealVideo and other), is supported.

Many other features available through the standard Qseven® connector are native for i.MX6 processor: CAN Interface, UART interfaces, SD/SDIO/MMC interface, PCI-Express x1, SATA (not available with i.MX6 Solo and Dual Lite), 2 x PWM Channels, Audio, GPI/Os, one USB OTG port.

USB Hi-Speed interface drives an SMSC USB2514 USB2.0 Hi-Speed USB Hub Controller, which allows the board to have 4 USB 2.0 Host Ports.

RGMII i.MX6 native interface is internally carried to a Micrel KSZ9031RN Ethernet Transceiver, allowing the implementation of a Gigabit Ethernet interface

The Lattice CPLD mounted on board, makes available LPC Bus, one additional PWM Channel and one Timer input.

For external interfacing to standard devices, a carrier board with a 230-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as integration of other peripherals/devices not already included in Q7-928 CPU module.

Furthermore, an FFC/FPC connector is provided to give access to Image Processing Unit of i.MX6 processor, which supports multiple formats and can be connected to a wide variety of image sensors for video-preview, video-record and frame grabbing applications. Interfacing is possible using the direct parallel interface or the integrated MIPI/CSI interface (both available on the same connector).

2.2 Technical Specifications

Processors

NXP i.MX6 Family, based on ARM® CORTEX-A9 processors
- i.MX6S Solo - Single core up to 1GHz
- i.MX6D Dual - Dual core up to 1.2GHz per core
- i.MX6DL Dual Lite - Dual core up to 1GHz per core
- i.MX6Q Quad - Quad core up to 1.2GHz per core

Memory

Up to 4GB DDR3 onboard (up to 2GB with i.MX6S)

Graphics

Dedicated 2D Hardware accelerator
Dedicated 3D Hardware accelerator, supports OpenGL® ES2.0 3D
Dedicated Vector Graphics accelerator supports OpenVG™ (only i.MX6D and i.MX6Q)
Supports up to 3 independent displays with i.MX6D and i.MX6Q
Supports 2 independent displays with i.MX6DL and i.MX6S

Video Interface

1 x LVDS Dual Channel or 2 x LVDS Single Channel 18/24 bit interface
HDMI Interface
Video Input Port / Camera Connector

Video Resolution

LVDS, up to 1920x1200
HDMI, up to 1080p

Mass Storage

Onboard eMMC Disk, up to 32 GB *
SD/MMC/SDIO interface
1 x µSD Card Slot onboard
1 x External S-ATA Channel (only available with i.MX6D and i.MX6Q)

** Please consider that for HDD and Flash Disk manufacturers, 1GB = 10^9 Byte. Some OS (like, for example, Windows) intends 1GB = 1024^3 byte, so global capacity shown for Disk Properties will be less than expected. Please also consider that a portion of disk capacity will be used by internal Flash Controller for Disk management, so final capacity will be lower.*

USB

1 x USB OTG interface
4 x USB2.0 Host interfaces

Networking

Gigabit Ethernet interface

Audio

AC'97 Audio interface

PCI Express

1 x PCI-e x1 lane (only PCI-e 1.1 and Gen2 are supported)

Serial Ports

2 x Serial ports (TTL interface)
CAN port interface

Other Interfaces

I2C bus

LPC Bus

SM Bus

Power Management Signals

Power supply voltage: $+5V_{DC}$ ± 5%

Operating temperature: 0°C ÷ +60°C (commercial version) **
-40°C ÷ +85°C (industrial version) **

Dimensions: 70 x70 mm (2.76" x 2.76")

Supported Operating Systems: Linux
Android
Windows Embedded Compact 7

! *** Temperatures indicated are the maximum temperature that the heatspreader / heatsink can reach in any of its parts. This means that it is customer's responsibility to use any passive cooling solution along with an application-dependent cooling system, capable to ensure that the heatspreader / heatsink temperature remains in the range above indicated. Please also check paragraph 4.1*

2.3 Electrical Specifications

According to Qseven® specifications, Q7-928 board needs to be supplied only with an external +5V_{DC} power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from +5V_S power rail.

2.3.1 Power Consumption

Q7-928 module, like all Qseven® modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Anyway, it has been possible to measure power consumption directly on +5V_S power rail that supplies the board.

Status	Processor			
	i.MX6S	i.MX6DL	i.MX6D	i.MX6Q 2GB RAM OS Ubuntu 12.04
idle at login, output on serial port, no video	TBM	TBM	TBM	1.7W
idle at login, HDMI display connected, full HD resolution	TBM	TBM	TBM	1.8W
idle at login, HDMI display connected, full HD resolution, USB Disk connected	TBM	TBM	TBM	1.9W
With one core at 100% load	TBM	TBM	TBM	2.7W
With 2 cores at 100% load	---	TBM	TBM	3.3W
With 3 cores at 100% load	---	---	---	3.9W
With 4 cores at 100% load	---	---	---	4.6W

Please consider that power consumption is strongly dependent on the board's configuration, on number of processor cores active and from the interfaces that are SW enabled. PCI-express and SATA interface are particularly significant for power consumption, so it is strongly recommended to disable them (via SW) if they are not used.

2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_S: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_S, +5V_S.

_A: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_A, +3.3V_A.

Other suffixes are used for application specific power rails, which are usually derived from same value of voltage, switched rails (for example, +3.3V_CAM is derived from +3.3V_S, and so on).

2.3.3 Inrush current

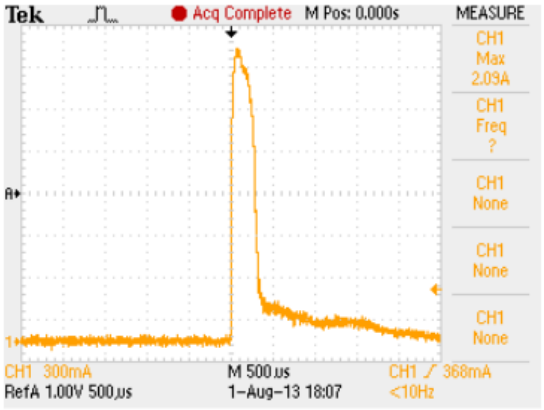
In the following pictures are shown the inrush current relative to the total current drawn by Q7-928 module (with the only exception of the battery absorbed by the battery, drawn from VCC_RTC pin).

Measurements have been made on all modules of Qseven i.MX6 family, no significant differences exist between various modules. For this reason, only graphs related to i.MX6 Solo equipped with 512MB of DRAM and i.MX6 Quad with 4GB of DRAM are shown.

Current measurements are made using a Current Probe Chauvin Arnoux E3N 10-100A/V and an Oscilloscope Tektronix TDS2022C

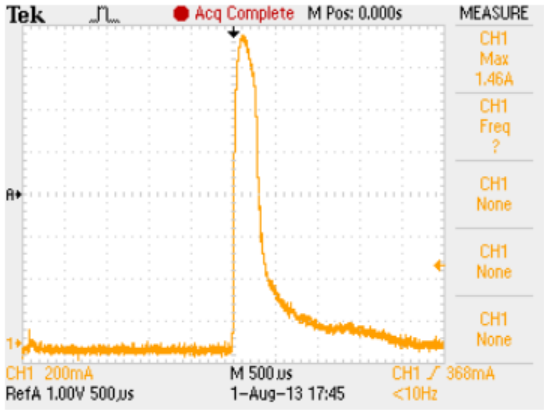
I_{VCC} current drawn from +5V_S power rail on MXM connector

I_{SB} current drawn from +5V_A power rail on MXM connector



SOLO 512MB

Fig. 1 – I_{VCC} + I_{VSB} Current consumption i.MX6 Solo 512MB DDR3



SOLO 512MB

Fig. 2 – I_{VCC} Current consumption i.MX6 Solo 512MB DDR3

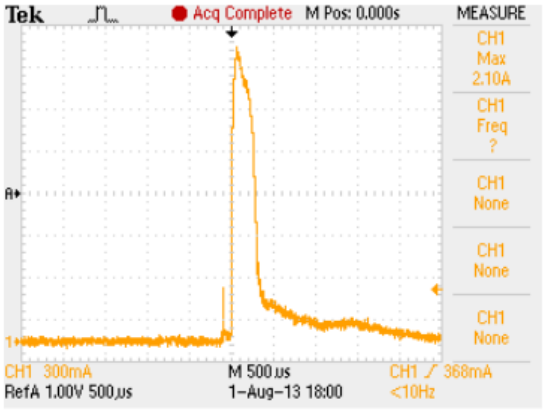


Fig. 3 – I_{VCC} + I_{VSB} Current consumption i.MX6 QUAD 4GB LDDR3

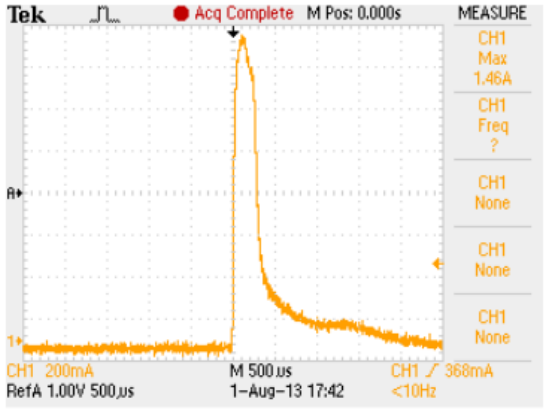
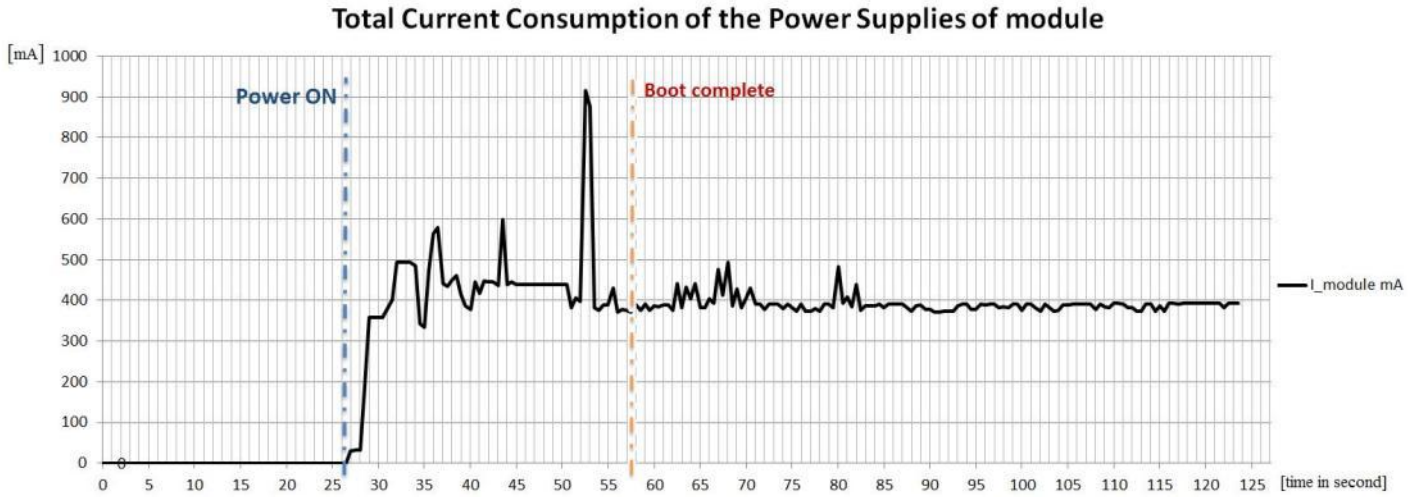


Fig. 4 – I_{VCC} Current consumption i.MX6 QUAD 4GB LDDR3

2.3.4 Current consumption during boot phase

The graphs below show the total current absorbed by the Q7-928 module in the boot phase, from POWER ON moment until the completion of the boot.

The data shown in figure 3 are related to the module Q7-928 with iMX6 Quad Core and 4 GB of LDDR3 RAM. Measurements are made using Digital Multimeter TTi-1705.



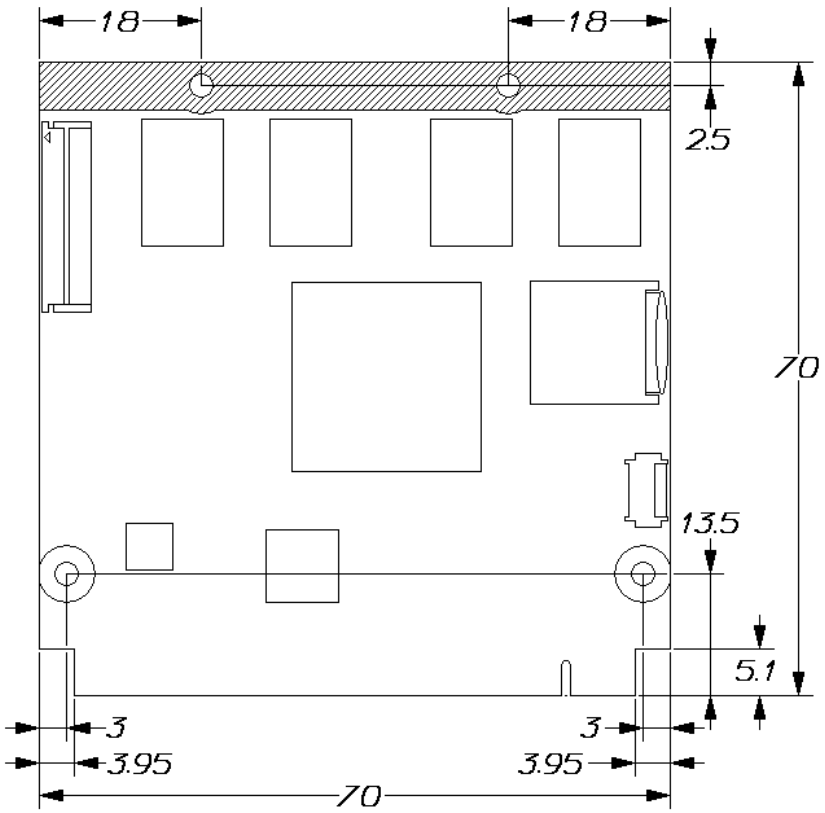
2.4 Mechanical Specifications

According to Qseven® specifications, board dimensions are: 70 x 70 mm (2.76” x 2.76”).

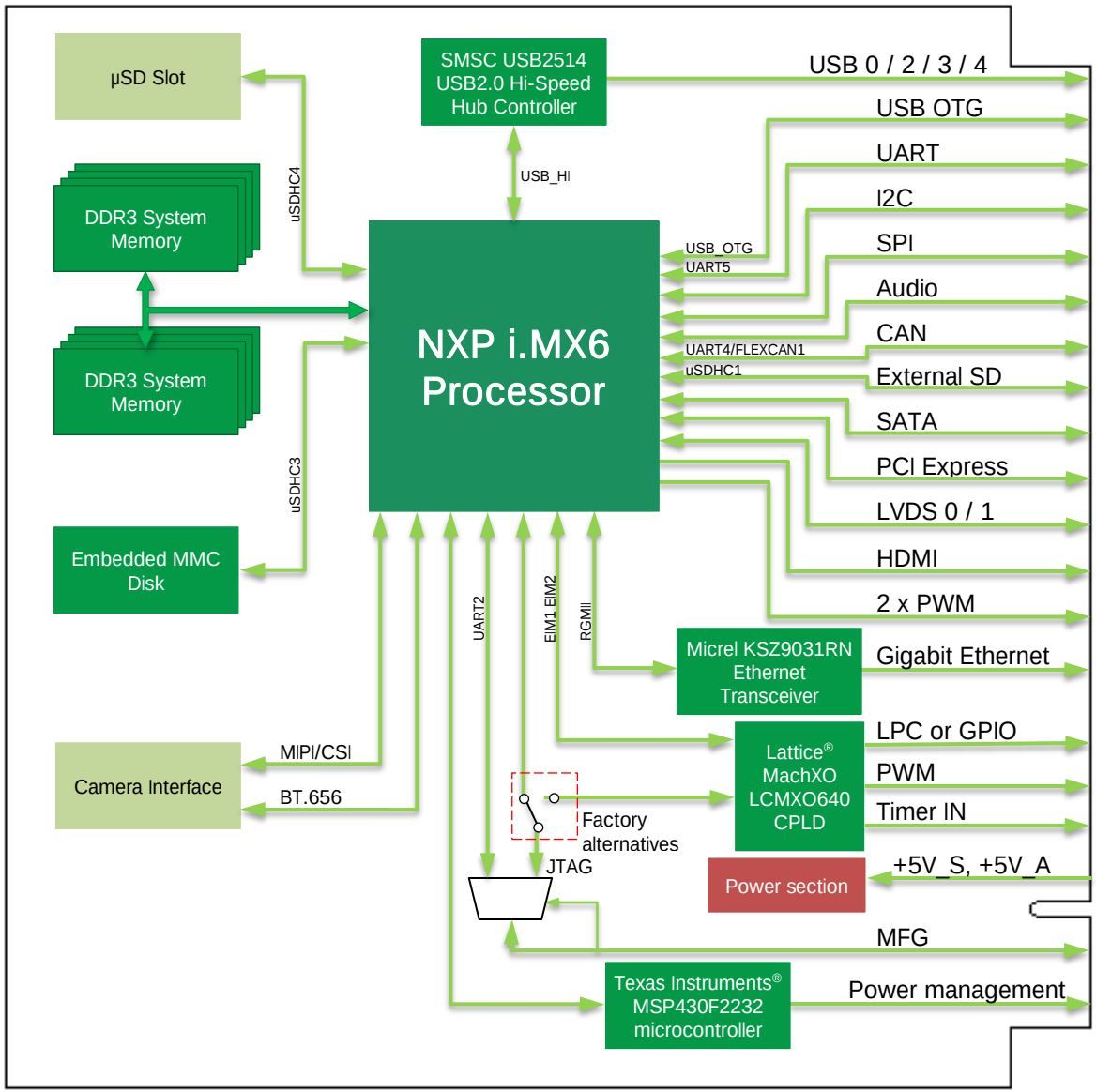
Printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs. Qseven® specification suggests two connector heights, 7.8mm and 7.5mm, but it is also possible to use different connector heights, also remaining compliant to the standard.

When using different connector heights, please consider that, according to Qseven® specifications, components placed on bottom side of Q7-928 will have a maximum height of 2.2mm ± 0.1. Keep this value in mind when choosing the MXM connector’s height, if it is necessary to place components on the carrier board in the zone below the Qseven® module.

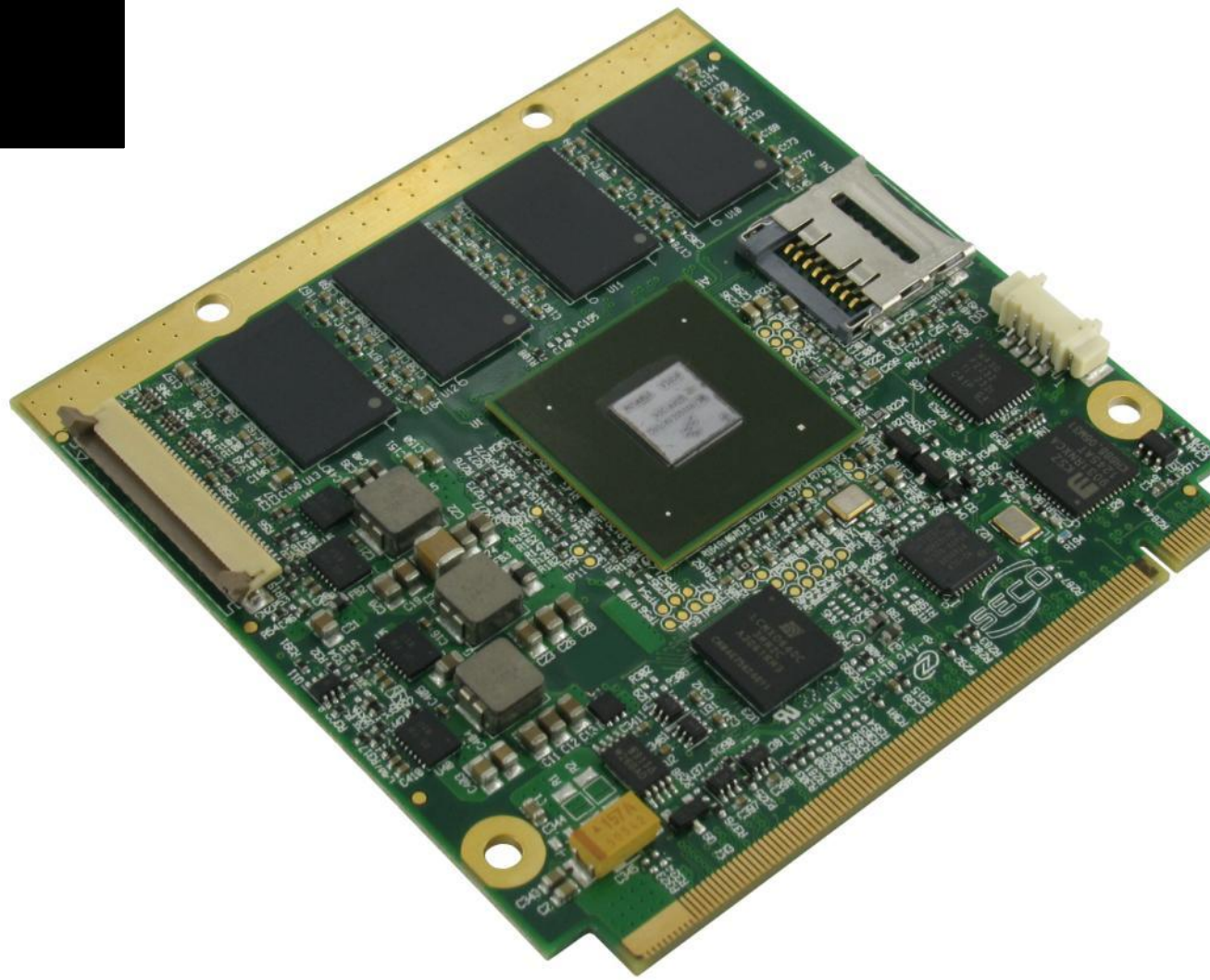


2.5 Block Diagram



Chapter 3.
CONNECTORS

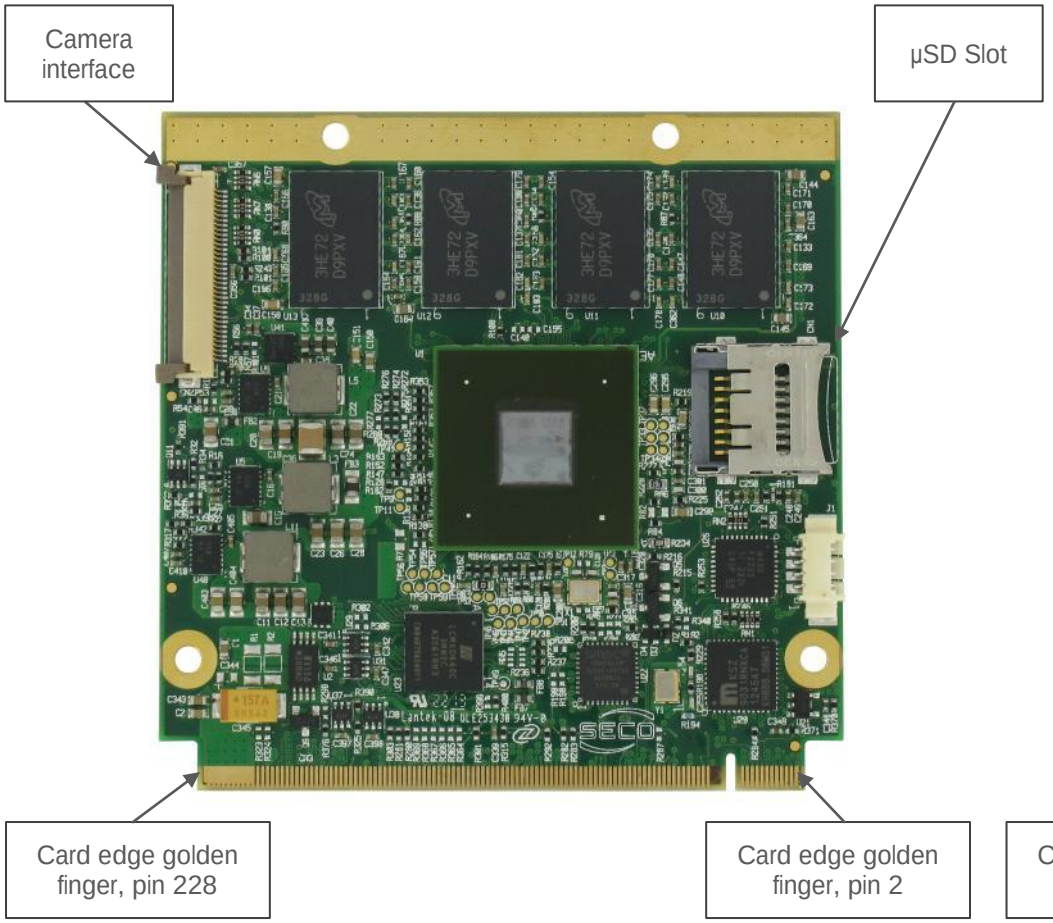
- Introduction
- Connectors description



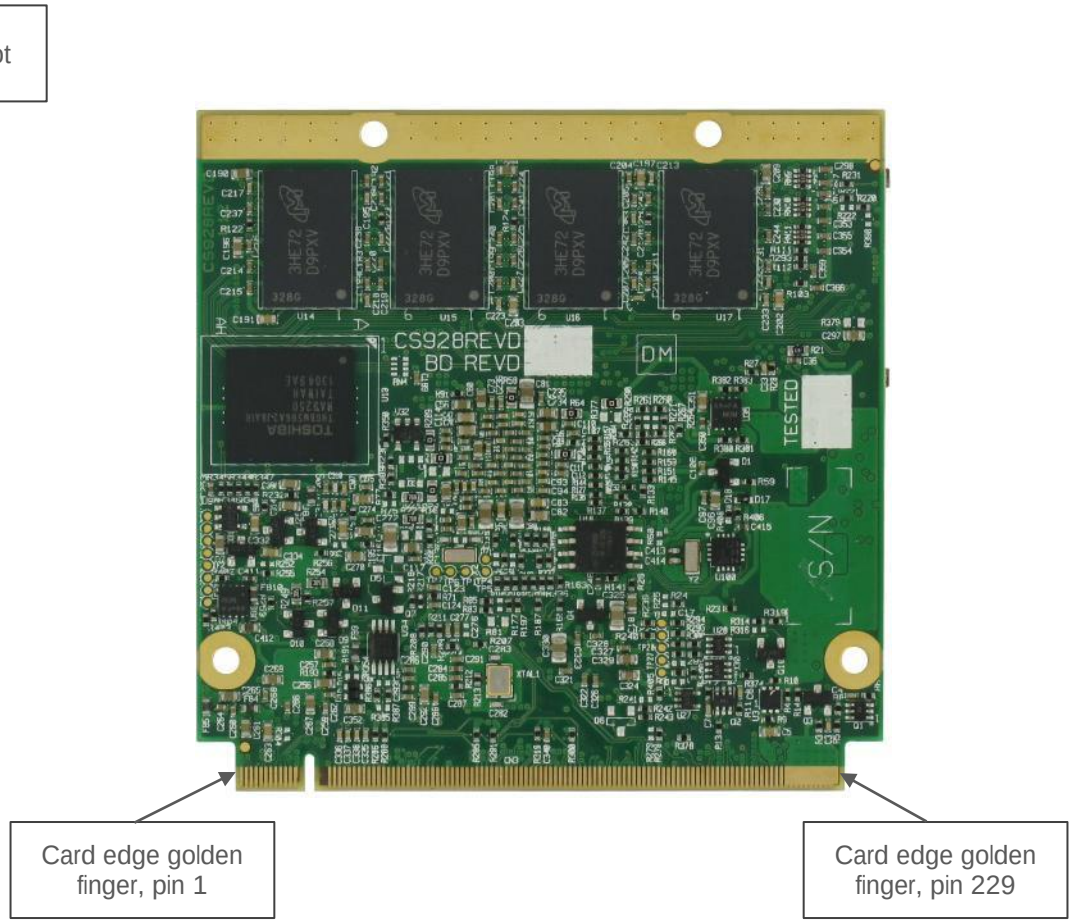
3.1 Introduction

According to Qseven® specifications, all interfaces to the board are available through a single card edge connector. In addition, a camera FFC/FPC connector card slot is present on the side of the board to take advantage of the integrated ISP (Image Signal Processing) subsystem of i.MX6 processor.

TOP SIDE



BOTTOM SIDE



3.2 Connectors description

3.2.1 FFC/FPC Camera Interface

CAMERA CONNECTOR - CN2			
Pin	**Signal**	**Pin**	**Signal**
1	CAM_XCLK_A	19	CSI0_DAT11
2	GND	20	CSI0_D2_DN
3	---	21	CSI0_D2_DP
4	GND	22	CAM_GPIO_A
5	CAM_PCLK	23	GP0_I2C_CLK
6	CAM_VS	24	GP0_I2C_DAT
7	CAM_HS	25	CAM_RESETB
8	CAM_FLD	26	GND
9	GND	27	CSI0_D3_DN
10	CSI0_DAT12	28	CSI0_D3_DP
11	CSI0_DAT13	29	+3.3V_CAM
12	CSI0_DAT14	30	+3.3V_CAM
13	CSI0_DAT15	31	CSI0_CLK0_DN
14	CSI0_DAT16	32	CSI0_CLK0_DP
15	CSI0_DAT17	33	CSI0_D0_DN
16	CSI0_DAT18	34	CSI0_D0_DP
17	CSI0_DAT19	35	CSI0_D1_DN
18	CSI0_DAT10	36	CSI0_D1_DP

NXP i.MX6 Processor includes an Image Processing Subsystem, that can be used for video applications, like video-preview, video recording and frame grabbing.

The access to the video input port comes through an FFC/FPC connector, type HIROSE p/n FH12A-36-S-0.5SH(55), which is able to accept 36 poles 0.5mm pitch FFC cables.

On the same connector are carried:

- a 10-bit parallel port, supporting ITU-R BT.656 and so on, managed by i.MX6 CSI2IPU gasket.
- MIPI CSI (Camera Serial Interface) Port.

Both video inputs can work independently and simultaneously.

For i.MX6 Solo and Dual Lite processors, CSI port is limited to 2 lanes only.

Here following is shown the meaning of various pins of the connector.

Pins[1÷17]: 8-bit parallel format arranged to guarantee 8-bit alignment LSB for ITU BT-656 format; voltage level: +3.3V_CAM.

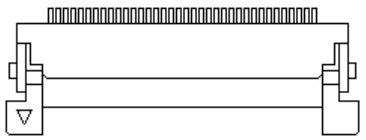
Pins[18÷19]: additional pins for 10-bit format; voltage level: +3.3V_CAM.

Pins[22÷25]: GPIO/CAM I2C; voltage level: +3.3V_CAM

Pins[29÷30]: +3.3V_CAM

Pins [31÷36]: MIPI CSI first channel (Clock+2 lanes)

Pins [20÷21; 27÷28]: MIPI CSI additional lanes (only for i.MX6 Dual and i.MX6 Quad)



3.2.2 µSD Card Slot

NXP i.MX6 processors offer many different SDIO interfaces, that can be used independently one from the other to implement different mass storages media (internal eMMC, internal SD Card, external SDI/O interface).

Of these interfaces, i.MX6 processor's SDI/O port #4 is carried to a standard µSD card slot, soldered on top side of the module.

> **!** Please be aware that the µSD card slot is a flip-top type: this means that, in order to insert / extract / change a µSD card, the heatsink/heatspreader must not be mounted, otherwise it will be impossible to access/open the flip top slot.

3.2.3 Qseven® Connector

According to Qseven® specifications, all interface signals are reported on the card edge connector, which is a 230-pin Card Edge that can be inserted into standard 230 pin MXM connectors, as described in Qseven® specifications.

Not all signals contemplated in Qseven® standard are implemented on MXM connector, due to the functionalities really implemented on Q7-928 CPU module. Therefore, please refer to the following table for a list of effective signals reported on MXM connector.

For accurate signals description, please consult the following paragraphs.

NOTE: Even pins are available on top side of CPU board; odd pins are available on bottom side of CPU board. Please refer to board photos.

Qseven® Golden Finger Connector - CN4

BOTTOM SIDE				TOP SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	1	2	GND	PWR	
GBE	I/O	GBE_MDI3-	3	4	GBE_MDI2-	I/O	GBE
GBE	I/O	GBE_MDI3+	5	6	GBE_MDI2+	I/O	GBE
GBE	O	GBE_LINK100#	7	8	GBE_LINK1000#	O	GBE
GBE	I/O	GBE_MDI1-	9	10	GBE_MDI0-	I/O	GBE
GBE	I/O	GBE_MDI1+	11	12	GBE_MDI0+	I/O	GBE
GBE	O	GBE_LINK#	13	14	GBE_ACT#	O	GBE
	N.A.	N.C.	15	16	SUS_S5#	O	PWR_MGMT
PWR_MGMT	I	WAKE#	17	18	SUS_S3#	O	PWR_MGMT
PWR_MGMT	O	SUS_STAT#	19	20	PWRBTN#	I	PWR_MGMT

PWR_MGMT	I	SLP_BTN#	21	22	LID_BTN#	I	PWR_MGMT
	PWR	GND	23	24	GND	PWR	
	PWR	GND	25	26	PWGIN	I	PWR_MGMT
PWR_MGMT	I	BATLOW#	27	28	RSTBTN#	I	PWR_MGMT
SATA	O	SATA0_TX+	29	30	N.C.	N.A.	
SATA	O	SATA0_TX-	31	32	N.C.	N.A.	
SATA	O	SATA_ACT#	33	34	GND	PWR	
SATA	I	SATA0_RX+	35	36	N.C.	N.A.	
SATA	I	SATA0_RX-	37	38	N.C.	N.A.	
	PWR	GND	39	40	GND	PWR	
MISC	I	BOOT_ALT#	41	42	SDIO_CLK	O	SDIO
SDIO	I/O	SDIO_CD#	43	44	SDIO_LED	O	SDIO
SDIO	O	SDIO_CMD	45	46	SDIO_WP	I/O	SDIO
SDIO	O	SDIO_PWR#	47	48	SDIO_DAT1	I/O	SDIO
SDIO	I/O	SDIO_DAT0	49	50	SDIO_DAT3	I/O	SDIO
SDIO	I/O	SDIO_DAT2	51	52	SDIO_DAT5	I/O	SDIO
SDIO	I/O	SDIO_DAT4	53	54	SDIO_DAT7	I/O	SDIO
SDIO	I/O	SDIO_DAT6	55	56	N.C.	N.A.	
	PWR	GND	57	58	GND	PWR	
AUDIO	O	HDA_SYNC	59	60	SMB_CLK	I/O	MISC
AUDIO	O	HDA_RST#	61	62	SMB_DAT	I/O	MISC
AUDIO	O	HDA_BCLK	63	64	N.C.	N.A.	
AUDIO	I	HDA_SDI	65	66	GP0_I2C_CLK	I/O	MISC
AUDIO	O	HDA_SDO	67	68	GP0_I2C_DAT	I/O	MISC
	N.A.	N.C.	69	70	WDTRIG#	I	MISC
	N.A.	N.C.	71	72	WDOUT	O	MISC
	PWR	GND	73	74	GND	PWR	
	N.A.	N.C.	75	76	N.C.	N.A.	
	N.A.	N.C.	77	78	N.C.	N.A.	
	N.A.	N.C.	79	80	USB_4_5_OC#	I	USB

	N.A.	N.C.	81	82	USB_P4-	I/O	USB
	N.A.	N.C.	83	84	USB_P4+	I/O	USB
USB	I	USB_2_3_OC#	85	86	USB_0_1_OC#	I	USB
USB	I/O	USB_P3-	87	88	USB_P2-	I/O	USB
USB	I/O	USB_P3+	89	90	USB_P2+	I/O	USB
USB	I	USB_CC	91	92	USB_ID	I	USB
USB	I/O	USB_P1-	93	94	USB_P0-	I/O	USB
USB	I/O	USB_P1+	95	96	USB_P0+	I/O	USB
	PWR	GND	97	98	GND	PWR	
LVDS	O	LVDS_A0+	99	100	LVDS_B0+	O	LVDS
LVDS	O	LVDS_A0-	101	102	LVDS_B0-	O	LVDS
LVDS	O	LVDS_A1+	103	104	LVDS_B1+	O	LVDS
LVDS	O	LVDS_A1-	105	106	LVDS_B1-	O	LVDS
LVDS	O	LVDS_A2+	107	108	LVDS_B2+	O	LVDS
LVDS	O	LVDS_A2-	109	110	LVDS_B2-	O	LVDS
LVDS	O	LVDS_PPEN	111	112	LVDS_BLEN	O	LVDS
LVDS	O	LVDS_A3+	113	114	LVDS_B3+	O	LVDS
LVDS	O	LVDS_A3-	115	116	LVDS_B3-	O	LVDS
	PWR	GND	117	118	GND	PWR	
LVDS	O	LVDS_A_CLK+	119	120	LVDS_B_CLK+	O	LVDS
LVDS	O	LVDS_A_CLK-	121	122	LVDS_B_CLK-	O	LVDS
LVDS		LVDS_BLT_CTRL/GP_PWM_OUT0	123	124	HDMI_CEC	I/O	HDMI
MISC	I/O	GPIO_6	125	126	LVDS_BLC_DAT	O	LVDS
MISC	I/O	GPIO_19	127	128	LVDS_BLC_CLK	O	LVDS
CAN	O	CAN0_TX	129	130	CAN0_RX	I	CAN
HDMI	O	TMDS_CLK+	131	132	N.C.	N.A.	
HDMI	O	TMDS_CLK-	133	134	N.C.	N.A.	
	PWR	GND	135	136	GND	PWR	
HDMI	O	TMDS_TX1+	137	138	N.C.	N.A.	
HDMI	O	TMDS_TX1-	139	140	N.C.	N.A.	

	PWR	GND	141	142	GND	PWR	
HDMI	O	TMDS_TX0+	143	144	N.C.	N.A.	
HDMI	O	TMDS_TX0-	145	146	N.C.	N.A.	
	PWR	GND	147	148	GND	PWR	
HDMI	O	TMDS_TX2+	149	150	HDMI_CTRL_DAT	I/O	HDMI
HDMI	O	TMDS_TX2-	151	152	HDMI_CTRL_CLK	I/O	HDMI
HDMI	O	HDMI_HPD#	153	154	N.C.	N.A.	
PCI-E	O	PCIE_CLK_REF+	155	156	PCIE_WAKE#	I	PCI-E
PCI-E	O	PCIE_CLK_REF-	157	158	PCIE_RST#	O	PCI-E
	PWR	GND	159	160	GND	PWR	
	N.A.	N.C.	161	162	N.C.	N.A.	
	N.A.	N.C.	163	164	N.C.	N.A.	
	PWR	GND	165	166	GND	PWR	
	N.A.	N.C.	167	168	N.C.	N.A.	
	N.A.	N.C.	169	170	N.C.	N.A.	
UART	O	UART0_TX	171	172	N.C.	N.A.	
	N.A.	N.C.	173	174	N.C.	N.A.	
	N.A.	N.C.	175	176	N.C.	N.A.	
UART	I	UART0_RX	177	178	N.C.	N.A.	
PCI-E	O	PCIE0_TX+	179	180	PCIE0_RX+	I	PCI-E
PCI-E	O	PCIE0_TX-	181	182	PCIE0_RX-	I	PCI-E
	PWR	GND	183	184	GND	PWR	
LPC/GPIO	I/O	LPC_AD0/GPIO0	185	186	LPC_AD1/GPIO1	I/O	LPC/GPIO
LPC/GPIO	I/O	LPC_AD2/GPIO2	187	188	LPC_AD3/GPIO3	I/O	LPC/GPIO
LPC/GPIO	I/O	LPC_CLK/GPIO4	189	190	LPC_FRAME#/GPIO5	I/O	LPC/GPIO
LPC/GPIO	I/O	SERIRQ/GPIO6	191	192	LPC_LDRQ#/GPIO7	I/O	LPC/GPIO
	PWR	VCC_RTC (+3.3V_A)	193	194	GP_PWM_OUT2	O	MISC
MISC	I	GP_TIMER_IN	195	196	GP_PWM_OUT1	O	MISC
	PWR	GND	197	198	GND	PWR	
SPI	O	SPI_MOSI	199	200	SPI_CS0#	O	SPI

SPI	I	SPI_MISO	201	202	SPI_CS1#	O	SPI
SPI	O	SPI_CLK	203	204	MFG_NC4	N.A.	MFG
	PWR	+5V_A	205	206	+5V_A	PWR	
MFG	N.A.	MFG_NC0	207	208	MFG_NC2	N.A.	MFG
MFG	N.A.	MFG_NC1	209	210	MFG_NC3	N.A.	MFG
	PWR	+5V_S	211	212	+5V_S	PWR	
	PWR	+5V_S	213	214	+5V_S	PWR	
	PWR	+5V_S	215	216	+5V_S	PWR	
	PWR	+5V_S	217	218	+5V_S	PWR	
	PWR	+5V_S	219	220	+5V_S	PWR	
	PWR	+5V_S	221	222	+5V_S	PWR	
	PWR	+5V_S	223	224	+5V_S	PWR	
	PWR	+5V_S	225	226	+5V_S	PWR	
	PWR	+5V_S	227	228	+5V_S	PWR	
	PWR	+5V_S	229	230	+5V_S	PWR	

3.2.3.1 PCI Express interface signals

Q7-928 can offer one PCI Express lane, which is directly managed by i.MX6 processor (all versions).

PCI express Gen 2.0 (5Gbps) is supported. Of the previous generation, only PCI express 1.1 is supported.

Here following the signals involved in PCI express management

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE_CLK_REF+ / PCIE_CLK_REF-: PCI Express Reference Clock for lane #0, Differential Pair

PCIE_WAKE#: Qseven® Module's Wake Input, it must be externally driven by devices requiring waking up the system. Since it is an Active-Low Input to the module, this signal is pulled-up with a 10kΩ resistor to +3.3V_A power rail. On the carrier board, connect it directly to the PCI-e/miniPCI-e connector's WAKE# signal, or to WAKE# signal of any eventual PCI-e Controller present on the Carrier Board.

PCIE_RST#: Reset Signal that is sent from Qseven® Module to any PCI-e device available on the carrier board. It is a 3.3V active-low signal, tied to GND via a 47kΩ resistor; it can be used directly to drive externally a single RESET Signal. In case it is necessary to supply Reset signal to multiple devices, provide for a buffer on the carrier board.

3.2.3.2 UART interface signals

According to newest Qseven® Rel. 2.0 specifications, Q7-928 offers one UART interface, directly managed by i.MX6 processor (all versions).

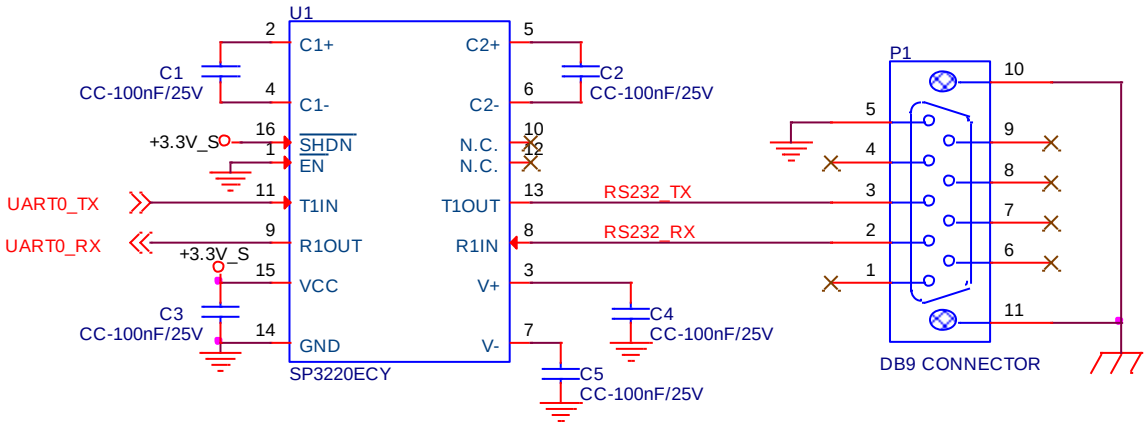
Here following the signals related to UART interface:

UART0_TX: UART Interface, Serial data Transmit (output) line, 3.3V_S electrical level

UART0_RX: UART Interface, Serial data Receive (input) line, 3.3V_S electrical level with 10kΩ pull-up resistor

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it is not explicitly necessary to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The following schematic shows an example of implementation of RS-232 transceiver for the Carrier board



> **!**
>
> All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.r.l. for the sole purpose of supporting the customers' internal development activities.
>
> The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.
>
> The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

3.2.3.3 Gigabit Ethernet signals

Gigabit Ethernet interface is realised, on Q7-928 module, using a Micrel® KSZ9031 Gigabit Ethernet transceiver, which is interfaced to NXP i.MX6 processor through RGMII interface.

Theoretical maximum speed of 1Gbps, however, cannot be reached, due to a known limitation of i.MX6 Gb Ethernet MAC (ENET), which is limited only to 470Mbps (also check NXP® Errata ERR004512 for i.MX6 processors).

Here following the signals involved in PCI express management

GBE_MDI0+/GBE_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE_MDI1+/GBE_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE_MDI2+/GBE_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE_MDI3+/GBE_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE_ACT#: Ethernet controller activity indicator. Active Low Output signal, electrical level +3.3V_S

GBE_LINK#: Ethernet controller link indicator, Active Low Output signal. Electrically tied to GBE_ACT# signal.

GBE_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, electrical level +3.3V_S

GBE_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, electrical level +3.3V_S

Please notice that if in the carrier board is needed just a FastEthernet (i.e. 10/100 Mbps) connection, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected.

3.2.3.4 S-ATA signals

Only one S-ATA interface is available on Q7-928 module. It is managed directly by i.MX6 processor.

Please notice, however, that this SATA interface (which is a SATA II, 3.0 Gbps interface) is available only with i.MX6 Quad and i.MX6 Dual versions, not with i.MX6 Solo or i.MX6 Dual Lite

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair

SATA_ACT#: Serial ATA Activity Led. Open collector output at +3.3V_S voltage. It is driven during SATA drive activity.

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

3.2.3.5 USB interface signals

NXP i.MX6 processor offers four different USB 2.0 controllers.

USB 2.0 controller Core #0 is capable of OTG (On-The-Go) capabilities, capable to work in High Speed (HS), Full Speed (FS) and Low Speed (LS) in Host mode, and HS/FS in peripheral mode. It is carried out directly to the golden finger connector

USB 2.0 controller Core #1 can work only in Host mode, and can work in HS, FS and LS. It is carried, internally to the upstream port of an SMSC USB2514 USB 2.0 Hub controller, which controls four downstream USB 2.0 compliant ports directly available on golden finger connector (referred as USB ports #0, #2, #3 and #4)

i.MX6 processor's USB controller cores #2 and #3 are not used by the module.

Here following the signals related to USB interfaces.

USB_P0+/USB_P0-: Universal Serial Bus Port #0 differential pair (coming out from USB2514 Hub Controller Downstream port #1).

USB_P1+/USB_P1-: Universal Serial Bus Port #1 differential pair (directly managed by i.MX6 USB OTG port).

USB_P2+/USB_P2-: Universal Serial Bus Port #2 differential pair (coming out from USB2514 Hub Controller Downstream port #2)

USB_P3+/USB_P3-: Universal Serial Bus Port #3 differential pair (coming out from USB2514 Hub Controller Downstream port #3)

USB_P4+/USB_P4-: Universal Serial Bus Port #4 differential pair (coming out from USB2514 Hub Controller Downstream port #4).

USB_ID: USB ID Input, electrical level +3.3V_S, 10kΩ pull-up. This signal must be driven as an open collector signal by external circuitry placed on the carrier board. It must be tied to GND when USB Port #1 has to be set to work in Host mode. When not driven, USB Port#1 will work in Client mode.

USB_CC: USB Client Connect Pin, electrical level +3.3V_S, 10kΩ pull-up. When USB Port #1 is set to work in Client mode, then this signal shall be used to inform the USB controller when an external USB Host is connected (signal High) or disconnected (Signal Low).

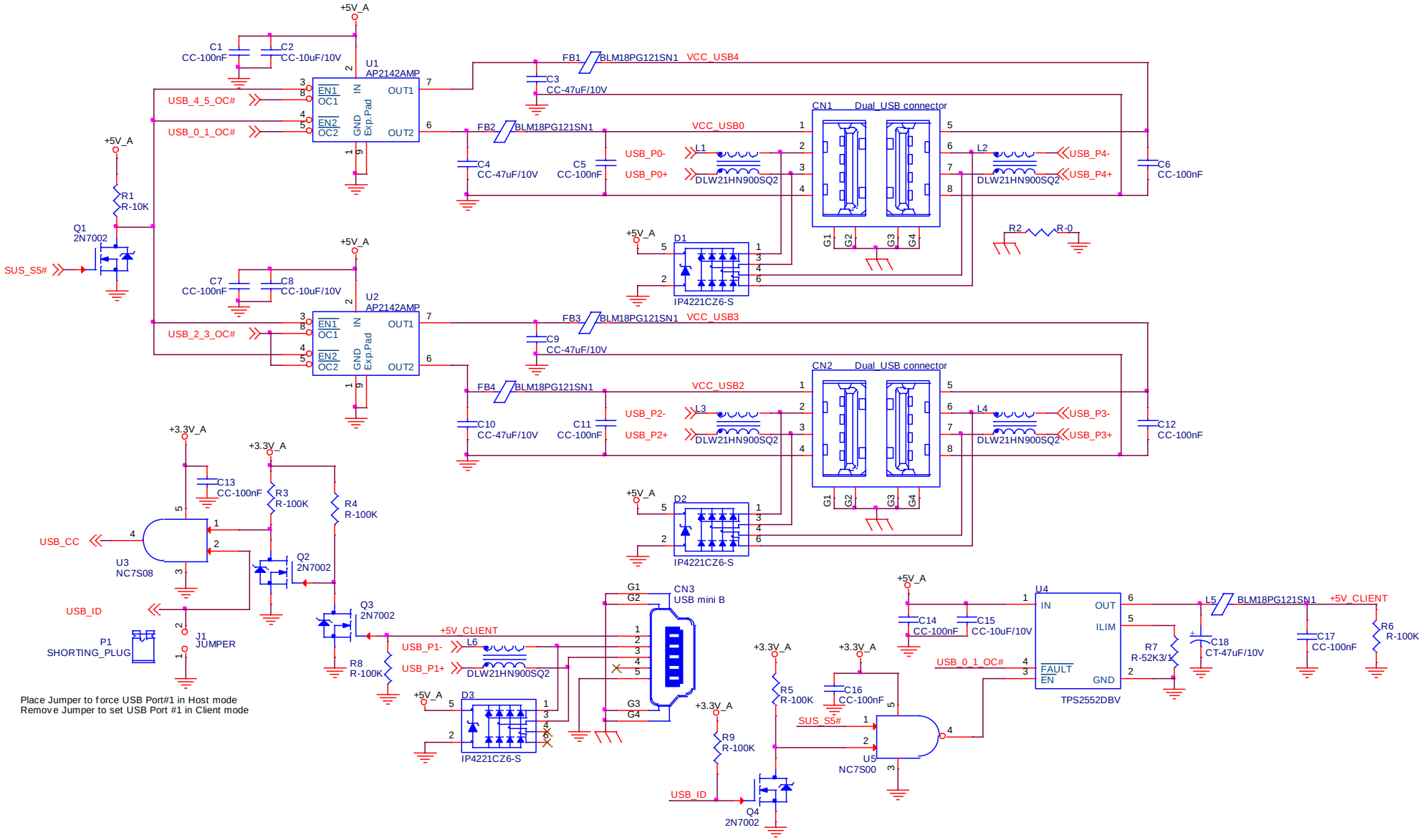
USB_0_1_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_S with 47kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port#0 of Q7-928 module

USB_2_3_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_S with 47kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Ports #2 and #3 of Q7-928 module

USB_4_5_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_S with 47kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #4 of Q7-928 module

Please notice that for correct management of Overcurrent signals, power distribution switches are needed on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed. The schematics in the following page are an example of implementation on the Carrier Board. In these schematics, USB ports #0, #2, #3 and #4 are carried out to standard USB 2.0 Type A receptacles, while USB port #1 implements all the circuitry necessary for USB OTG management.


+5V_A
C1
CC-100nF
C2
CC-10uF/10V
U1
AP2142AMP
EN1
OC1
EN2
OC2
IN
GND
Exp.Pad
OUT1
OUT2
USB_4_5_OC#
USB_0_1_OC#
FB1
BLM18PG121SN1
VCC_USB4
C3
CC-47uF/10V
FB2
VCC_USB0
C4
CC-47uF/10V
C5
CC-100nF
USB_P0-
USB_P0+
L1
DLW21HN900SQ2
CN1
Dual_USB connector
L2
USB_P4-
USB_P4+
C6
CC-100nF
R1
R-10K
Q1
2N7002
SUS_S5#
D1
IP4221CZ6-S
R2
R-0
C7
CC-100nF
C8
CC-10uF/10V
U2
AP2142AMP
USB_2_3_OC#
FB3
VCC_USB3
C9
CC-47uF/10V
FB4
VCC_USB2
C10
CC-47uF/10V
C11
CC-100nF
USB_P2-
USB_P2+
L3
DLW21HN900SQ2
CN2
Dual_USB connector
L4
USB_P3-
USB_P3+
C12
CC-100nF
D2
IP4221CZ6-S
+3.3V_A
C13
CC-100nF
R3
R-100K
R4
R-100K
USB_CC
U3
NC7S08
Q2
2N7002
USB_ID
P1
SHORTING_PLUG
J1
JUMPER
Q3
2N7002
R8
R-100K
+5V_CLIENT
USB_P1-
USB_P1+
L6
DLW21HN900SQ2
CN3
USB mini B
D3
IP4221CZ6-S
R5
R-100K
R9
R-100K
Q4
2N7002
C14
CC-100nF
C15
CC-10uF/10V
U4
IN
OUT
ILIM
FAULT
EN
GND
TPS2552DBV
R7
R-52K3/1
C18
CT-47uF/10V
L5
BLM18PG121SN1
+5V_CLIENT
C17
CC-100nF
R6
R-100K
C16
CC-100nF
U5
NC7S00
Place Jumper to force USB Port#1 in Host mode
Remove Jumper to set USB Port #1 in Client mode

3.2.3.6 SDI/O interface signals

As previously told in paragraph 3.2.2, NXP i.MX6 processors offer many different SDIO interfaces, that can be used independently one from the other to implement different mass storages (internal eMMC, internal SD Card, external SDI/O interface).

Each of the uSDHC controllers complies with:

- SD Host Controller Standard Specification version 3.0
- MMC System Specification version 4.2/4.3/4.4/4.41
- SD Memory Card Specification version 3.0 and supports the Extended Capacity SD Memory Card
- SDIO Card Specification version 3.0

SDI/O port #1 is externally accessible through golden edge finger connector, and can work in 1-bit, 4-bit and 8-bit modes (8-bit mode for MMC support).

Signals involved with SDI/O interface are the following:

SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +3.3V_S with 10kΩ pull-up resistor. This signal must be externally pulled low to signal that a SDIO/MMC Card is present.

SDIO_CLK: Clock Line (output), 52MHz maximum frequency for MMC High Speed Mode, 50 MHz maximum frequency for SD/SDIO High Speed Mode

SDIO_CMD: Command/Response line. Bidirectional signal, electrical level +3.3V_S, used to send command from Host (i.MX6 processor) to the connected card, and to send the response from the card to the Host.

SDIO_LED: LED output signal, electrical level +3.3V_S. It is used to drive an external LED when there are transfers on SD Bus.

SDIO_WP: Write Protect bidirectional signal, electrical level +3.3V_S. It is used to communicate the status of Write Protect switch on external SD/MMC card.

SDIO_PWR#: SD power enable, tied to GND through a 47kΩ pull-down resistor.

SDIO_DAT[0÷7]: SDIO data bus. SDIO_DAT0 signal is used for all communication modes. SDIO_DAT[1÷3] signals are required for 4-bit SD/SDIO/MMC communication modes. SDIO_DAT[4÷7] are used only for 8-bit MMC communication mode.

3.2.3.7 Audio interface signals

Q7-928 module supports AC'97 audio format, thanks to native support offered by the processor to this audio codec standard.

Both AC'97 Fixed and variable mode are supported, min frame rate 8kHz, max Frame rate 48kHz

Here following the signals related to Audio AC'97 interface:

HDA_SYNC: AC'97 Serial Bus Synchronization. Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_RST#: AC'97 Codec Reset. Active Low signal Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_BCLK: AC'97 Serial Bit Clock signal. Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_SDO: AC'97 Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_SDI: AC'97 Serial Data In signal. Input to the module from the Carrier board, electrical level +3.3V_S.

All these signals have to be connected, on the Carrier Board, to an AC'97 Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.3.8 LVDS Flat Panel signals

Embedded into NXP i.MX6 processor there is an LVDS Display Bridge, connected to the Image Processing Unit (IPU), that makes externally available two LVDS channels, each one consisting of 1 clock pair and four data pairs.

It is possible to configure LVDS output so that it can be used as:

- One single channel (18 or 24 bit) output, max resolution supported 1366 x 768 @ 60fps
- One dual channel (18 or 24 bit) output, max resolution supported 1920 x 1200 @ 60fps
- Two identical single channel outputs, max resolution supported 1366 x 768 @ 60fps
- Two independent single channel outputs, max resolution supported 1366 x 768 @ 60fps on each channel

All of these possibilities come by opportunely configuring the O.S. installed on the module.

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Channel #0 differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Channel #0 differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Channel #0 differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Channel #0 differential data pair #3.

LVDS_A_CLK+/LVDS_A_CLK-: LVDS Channel #0 differential Clock.

LVDS_B0+/LVDS_B0-: LVDS Channel #1 differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Channel #1 differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Channel #1 differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Channel #1 differential data pair #3.

LVDS_B_CLK+/LVDS_B_CLK-: LVDS Channel #1 differential Clock

LVDS_PPEN: +3.3V_S electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display.

LVDS_BLEN: +3.3V_S electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display.

LVDS_BLT_CTRL/GP_PWM_OUT0: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. When backlight brightness control via PWM is not required, this signal can be used as a General Purpose PWM output (+3.3V_S electrical level).

LVDS_BLC_DAT: I2C control data line for external Spread Spectrum Control Clock chip. Bidirectional signal, electrical level +3.3V_S with a 4k7Ω pull-up resistor.

LVDS_BLC_CLK: I2C control clock line for external Spread Spectrum Control Clock chip. Bidirectional signal, electrical level +3.3V_S.

3.2.3.9 HDMI interface signals

Besides LVDS interface, NXP i.MX6 processor also has an embedded HDMI Tx module, which provides a HDMI standard interface for HDMI1.4a compliant displays. By using HDMI interface along with two LVDS single channel interfaces, it is possible to drive up to 3 independent displays.

Signals involved in HDMI management are the following:

TMDS_CLK+/TMDS_CLK-: TMDS differential Clock.

TMDS_TX0+/TMDS_TX0-: TMDS differential pair #0

TMDS_TX1+/TMDS_TX1-: TMDS differential pair #1

TMDS_TX2+/TMDS_TX2-: TMDS differential pair #2

HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, electrical level +3.3V_S with a 4k7Ω pull-up resistor.

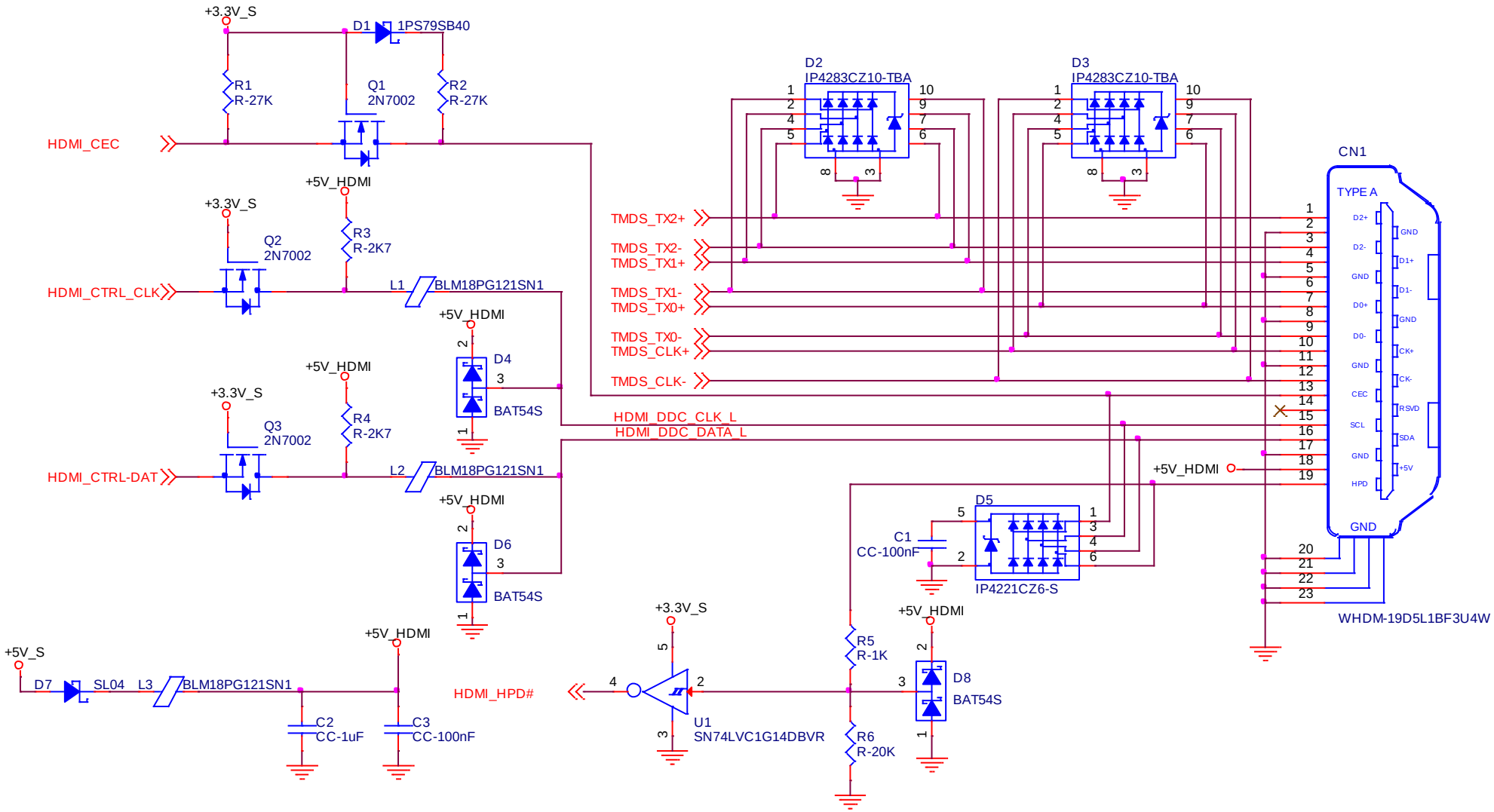
HDMI_CTRL_CLK: DDC Clock line for HDMI panel. Bidirectional signal, electrical level +3.3V_S with a 4k7Ω pull-up resistor.

HDMI_CEC: HDMI Consumer Electronics Control (CEC) Line. Bidirectional signal, electrical level +3.3V_S.

HDMI_HPD#: Hot Plug Detect Input signal. +3.3V_S electrical level signal with 100kΩ pull-down resistor

Since HDMI Tx module is embedded in the i.MX6 processors it is not necessary to implement voltage level shifter for TMDS differential pairs on the Carrier board. It is still necessary, however, to implement voltage level shifters on Control data/Clock signals, as well as for Hot Plug Detect signal.

Please refer to the following schematics as an example of implementation of voltage level shifters on the carrier board.



3.2.3.10 LPC/GPIO interface signals

According to Qseven® specifications rel. 2.0, on the golden edge finger connector there are 8 pins that can be used for implementation of Low Pin Count (LPC) Bus interface or as General Purpose I/Os (GPIO).

> **!** Please consider that LPC interface is not native for i.MX6 processors, it is derived from embedded LCMXO640 CPLD instead. Depending on the firmware programmed on that CPLD, it is possible to have available LPC **or** GPIO interface.
>
> Please take care of specifying if LPC interface or GPIOs are needed, before placing an order of Q7-928 module.

When the Board is programmed for LPC Interface, following signals will be available:

LPC_AD[0÷3]: LPC data bus, bidirectional signal, +3.3V_S electrical level.

LPC_CLK: LPC Clock Output line, +3.3V_S electrical level. Since only a clock line is available, if it is necessary to connect more LPC devices on the carrier board, then provide for a zero-delay clock buffer to connect all clock lines to the single clock output of Qseven® module.

LPC_FRAME#: LPC Frame indicator, active low output line, +3.3V_S electrical level. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

LPC_LDRQ#: LPC DMA request, active low input line, +3.3V_S electrical level. This signal is used only by peripherals requiring DMA or bus mastering

SERIRQ: LPC Serialised IRQ request, bidirectional line, +3.3V_S electrical level. This signal is used only by peripherals requiring Interrupt support.

When the board is programmed for GPIOs, all previous signals are not available and corresponding pins on Qseven® golden finger connector are General Purpose I/Os, bidirectional signals at +3.3V_S electrical level. Programming of these GPIOs can be made using dedicated APIs supplied by SECO, or through Linux File System.

3.2.3.11 SPI interface signals

i.MX6 processors offer up to four Enhanced Configurable Serial Peripheral Interfaces (eCSPIS), which can be used for connection of EEPROMs and Serial Flash devices, which can also be used for serial boot.

SPI interface can support speed up to 20MHz.

Signals involved with SPI management are the following:

SPI_MOSI: SPI Master Out Slave In, Output from Qseven® module to SPI devices embedded on the Carrier Board. Electrical level +3.3V_S

SPI_MISO: SPI Master In Slave Out, Input to Qseven® module from SPI devices embedded on the Carrier Board. Electrical level +3.3V_S

SPI_CLK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +3.3V_S

SPI_CS0#: SPI primary Chip select, active low output signal (+3.3V_S electrical level)

SPI_CS1#: SPI secondary Chip select, active low output signal (+3.3V_S electrical level). This signal must be used only in case there are two SPI devices on the carrier board, and the first chip select signal (SPI_CS0#) has already been used. It must not be used in case there is only one SPI device.

3.2.3.12 CAN interface signals

Since i.MX6 processor includes a Flexible Controller Area Network (FlexCAN), the Q7-928 module can also offer a CAN interface.

This interface is compliant to CAN specifications rel. 2.0 part B.

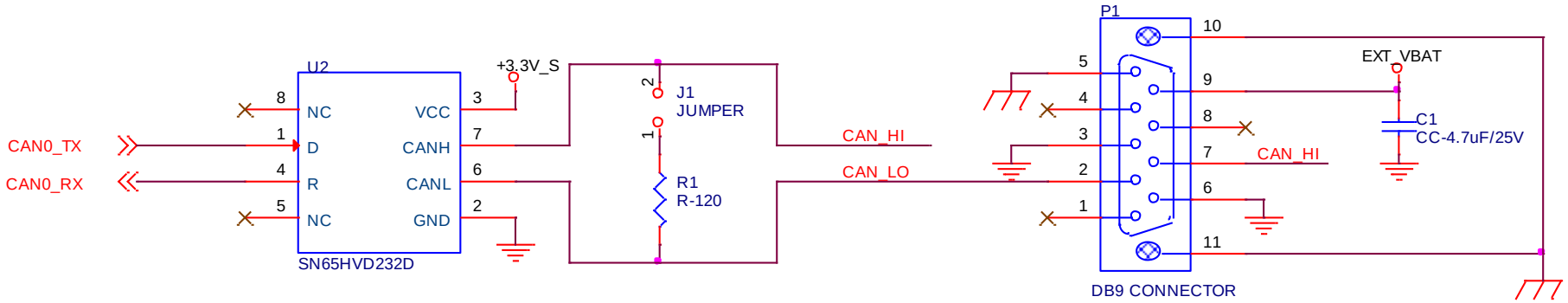
CAN0_TX: CAN Transmit Output for CAN Bus Channel 0. +3.3V_S electrical voltage level signal.

CAN0_RX: CAN Receive Input for CAN Bus Channel 0. +3.3V_S electrical voltage level signal.

Please consider that it is not possible to connect Qseven® CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

The following schematic represents an example of such an implementation.

In the example provided, CAN Bus connection is made through a DB9 connector, with standard CAN pinout for such a connector, where also external battery voltage is connected (+12V_{DC} batteries are considered as a referral for capacitor C1 sizing). 120Ω resistor is placed for line termination, in case that the system is placed to one of the two extremities of CAN Line. If this termination is required, simply plug a jumper in position J1.



3.2.3.13 Power Management signals

According to Qseven® specifications, on the golden edge finger connector there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWGIN: Power Good Input, +5V_S tolerant active high signal. It must be driven on the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

PWRBTN#: Power Button Input, active low +3.3V_A electrical voltage signal, with 10kΩ pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

RSTBTN#: Reset Button Input, active low +3.3V_S electrical voltage signal, with 10kΩ pull-up resistor. This signal can be connected to a momentary push-button:

a pulse to GND of this signal will reset the Qseven® module.

BATLOW#: Battery Low Input, active low +3.3V_A electrical voltage signal, with 10kΩ pull-up resistor. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. Can be left unconnected if not used

WAKE#: Wake Input, active low +3.3V_A electrical voltage signal with 10kΩ pull-up resistor and series Schottky diode. This signal can be driven low, on the carrier board, to report that a Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

SUS_STAT#: Suspend status output, active low +3.3V_A electrical voltage signal, with 10kΩ pull-up resistor. This output can be used to report to the devices on the carrier board that the module is going to enter in one of possible ACPI low-power states.

SUS_S3#: S3 status output, active low +3.3V_A electrical voltage signal, with 10kΩ pull-down resistor. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S5#: S5 status output, active low +3.3V_A electrical voltage signal, with 10kΩ pull-down resistor. This signal is used, on the carrier board, to shut off the power supply to all the devices that must become inactive only during S5 (Soft-Off) power state.

SLP_BTN#: Sleep button Input, active low +3.3V_A electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

LID_BTN#: LID button Input, active low +3.3V_A electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

3.2.3.14 Miscellaneous signals

Here following, a list of signals that complete the features of Q7-928 module.

WDTRIG#: Watchdog Trigger Input. It is an active low signal, +3.3V_S voltage, with 10kΩ pull-up resistor. This signal can be used to reset and restart, via Hardware, the internal Watchdog Timer (which is usually managed via Software using Q7-928 dedicated API - Application Program Interface - libraries).

WDOUT: Watchdog event indicator Output. It is an active high signal, +3.3V_S voltage, with 10kΩ pull-down resistor. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW.

BOOT_ALT#: Boot Alternate Input, active low +3.3V_S voltage signal with 2k2Ω pull-up resistor. When this signal is driven low, then i.MX6 processors starts to work in peripheral mode, i.e. it begins to wait for inputs from an external Host connected to the system. This is used usually when it is necessary to program the module.

GPIO_6: This signal is carried on the pin usually dedicated to LVDS DisplayID DDC Data line. On the Q7-928 module, instead, it can be used as a Generic Purpose I/O, electrical level +3.3V_S with a 4k7Ω pull-up resistor. It is connected to i.MX6 processor's GPIO_6 pad.

GPIO_19: This signal is carried on the pin usually dedicated to LVDS DisplayID DDC Clock line. On the Q7-928 module, instead, it can be used as a Generic Purpose I/O, electrical level +3.3V_S. It is connected to i.MX6 processor's GPIO_19 pad.

GP_TIMER_IN: General Purpose Timer Input. +3.3V_S voltage signal, directly managed by Lattice LCMXO640 CPLD.

GP_PWM_OUT1: General Purpose PWM output, +3.3V_S voltage signal, directly managed by Lattice LCMXO640 CPLD.

GP_PWM_OUT2 General Purpose PWM output, +3.3V_S voltage signal. It is connected to i.MX6 processor PWM2 functional output.

SMB_CLK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_S with a 4k7Ω pull-up resistor. It is managed by i.MX6 processor's I2C1 controller.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_S with a 4k7Ω pull-up resistor. It is managed by i.MX6 processor's I2C1 controller.

GP0_I2C_CLK: general purpose I2C Bus clock line. Bidirectional signal, electrical level +3.3V_S with a 4k7Ω pull-up resistor. It is managed by i.MX6 processor's I2C3 controller.

GP0_I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3.3V_S with a 4k7Ω pull-up resistor. It is managed by i.MX6 processor's I2C3 controller.

Regarding the i.MX6 I2C buses, please refer to the following table.

Bus	Bus Number / device	MXM Pins	Address Locked (@7 bit)
SM Bus	I2C_1/I2C-0	60: SMB_CLK 62: SMB_DAT	0x40
HDMI_DDC	I2C_2/I2C-1	150: HDMI_CTRL_DAT 152: HDMI_CTRL_CLK	0x50 (if HDMI Driver is enabled)
I2C	I2C_3/I2C-2	66: GP0_I2C_CLK 68: GP0_I2C_DAT	0x3C (if MIPI_CSI driver for OV5640 camera is enabled)

3.2.3.15 Manufacturing signals

According to Qseven® Standard specifications, rel. 2.0, on pin designed as MFG_NCx (pins 204, 207÷210) are carried the JTAG signal necessary to program Q7-928 internal FPGA.

Pins 208 and 209 are multiplexed, according to the above mentioned specifications, with NXP i.MX6 Internal UART #3 signals TX and RX.

Selection between JTAG and UART DEBUG signals is made by driving the MFG_NC4 signal carried on pin 204, with the following meaning:

MFG_NC4 signal level	Pin 208 (MFG_NC2) signal	Pin 209 (MFG_NC1) signal
LOW	UART_DEBUG_RX	UART_DEBUG_TX
HIGH	JTAG_TDI	JTAG_TDO

In case MFG_NC4 signal is not driven externally, then an internal pull-down makes available UART_DEBUG_RX and UART_DEBUG_TX signals on pin 208 and 209.

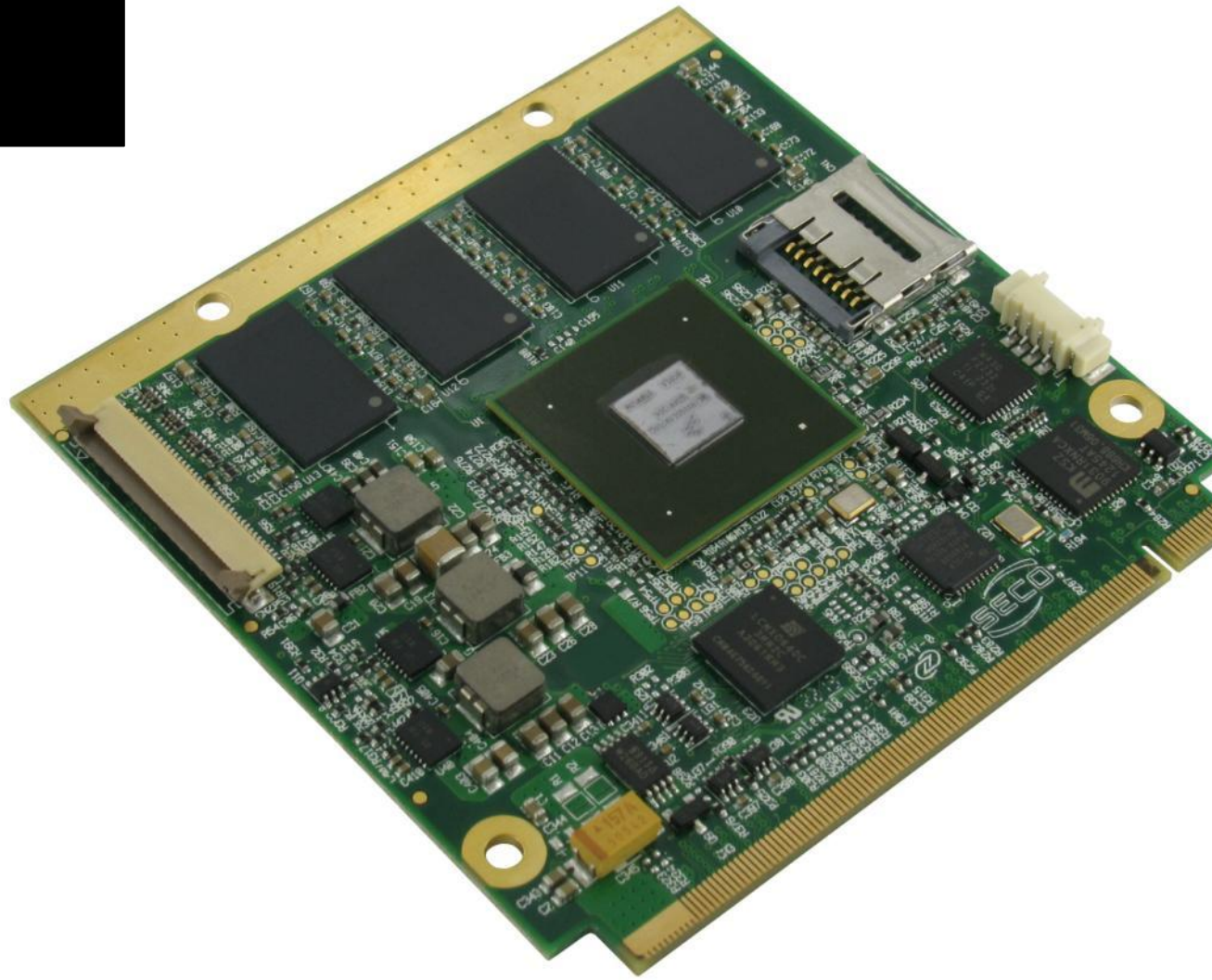
MFG_NC0 is always connected to JTAG_TCK, while MFG_NC3 is always connected to JTAG_TMS.

Please remember that JTAG interface is connected to Q7-928 embedded CPLD, not to the i.MX6 processor's JTAG interface. JTAG interface available on MFG_NCx pins is reserved only for manufacturing phase; **it must not be used by the customer**.

In case it is necessary to trace the software using any JTAG debugger, it is possible to provide Q7-928 module configured with i.MX6 JTAG port accessible on MFG_NCx pins. Please contact your Sales Representative for this.

Chapter 4.
Appendices

- Thermal Design



4.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like Q7-928 module, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

Qseven® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the Qseven® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

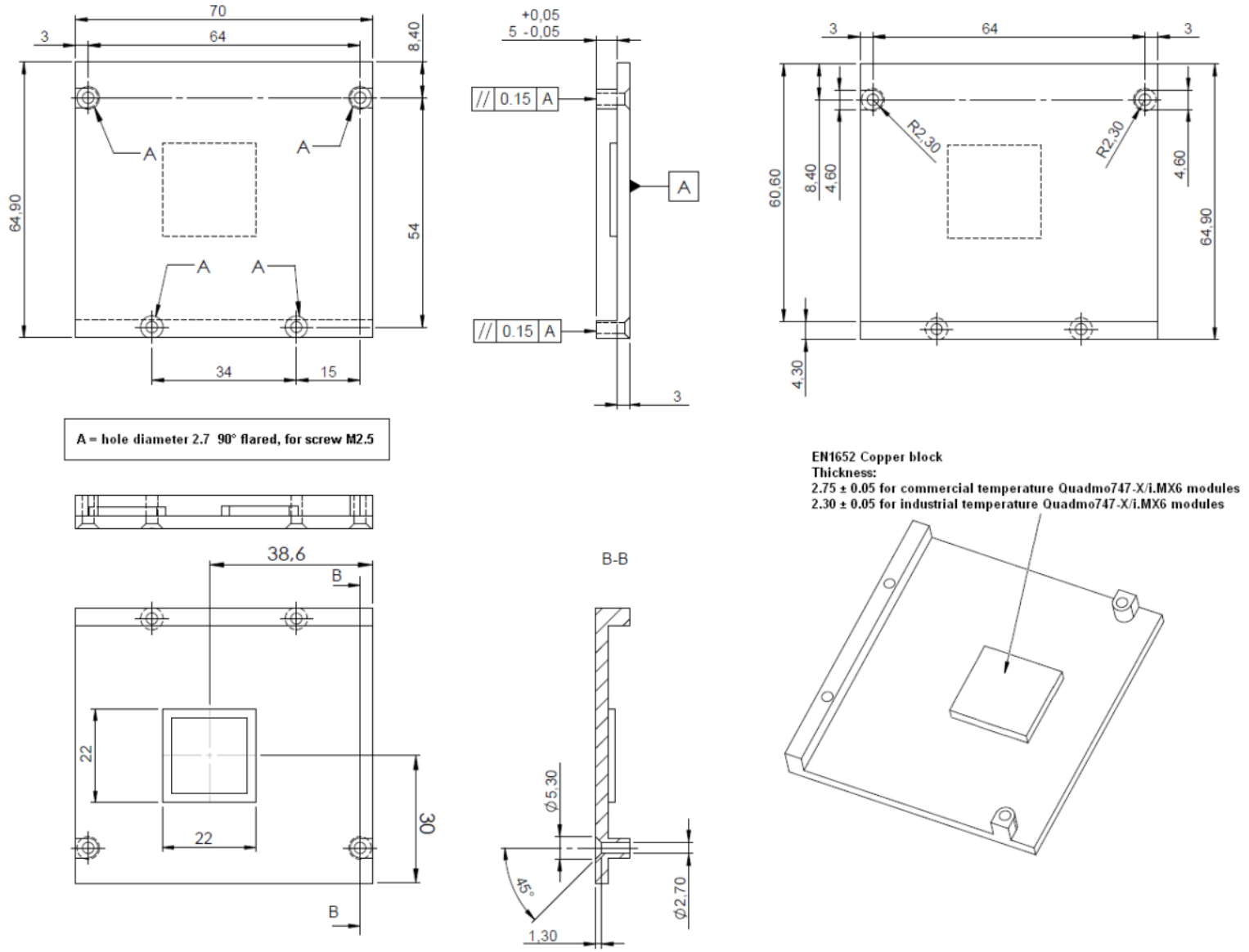
Conversely, heatsinks in some situation can represent the cooling solution. Indeed, when using Q7-928 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink could be sufficient for module's cooling (especially for i.MX6 Solo and Dual Lite versions). Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

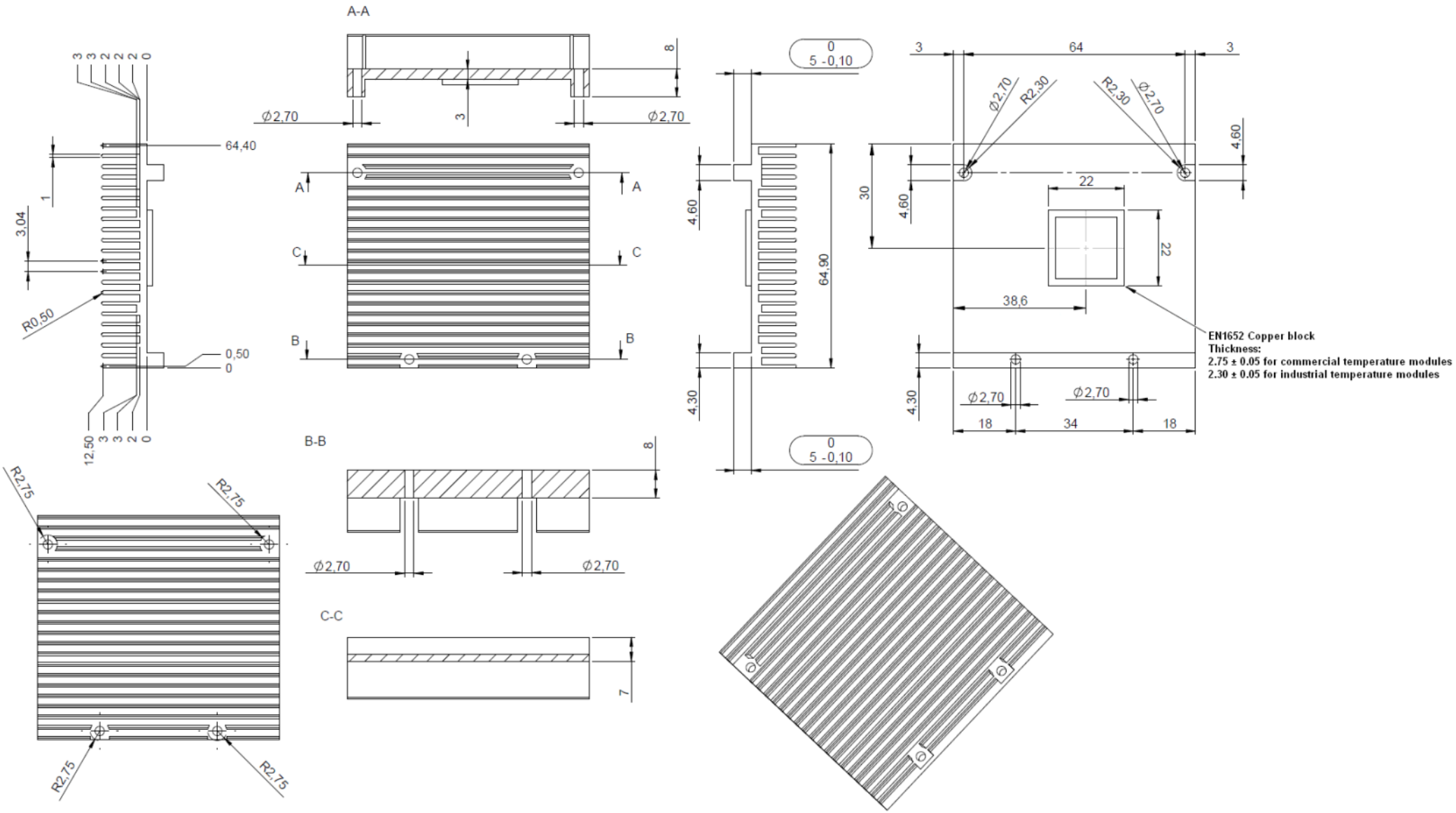
Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide Q7-928 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
Q928-DISS-1-C-PK	Q7-928 Heat Spreader (Passive) for COMMERCIAL VERSION and Solo & DualLite INDUSTRIAL, Packaged
Q928-DISS-1-I-PK	Q7-928 Heat Spreader (Passive) for Dual & Quad (AUTOMOTIVE & INDUSTRIAL), Packaged
Q928-DISS-2-C-PK	Q7-928 HeatSink (Passive) for COMMERCIAL VERSION and Solo & DualLite INDUSTRIAL, Packaged
Q928-DISS-2-I-PK	Q7-928 HeatSink (Passive) for Dual & Quad (AUTOMOTIVE & INDUSTRIAL), Packaged



Standard Heatspreader dimensions



Standard Heatsink dimensions

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