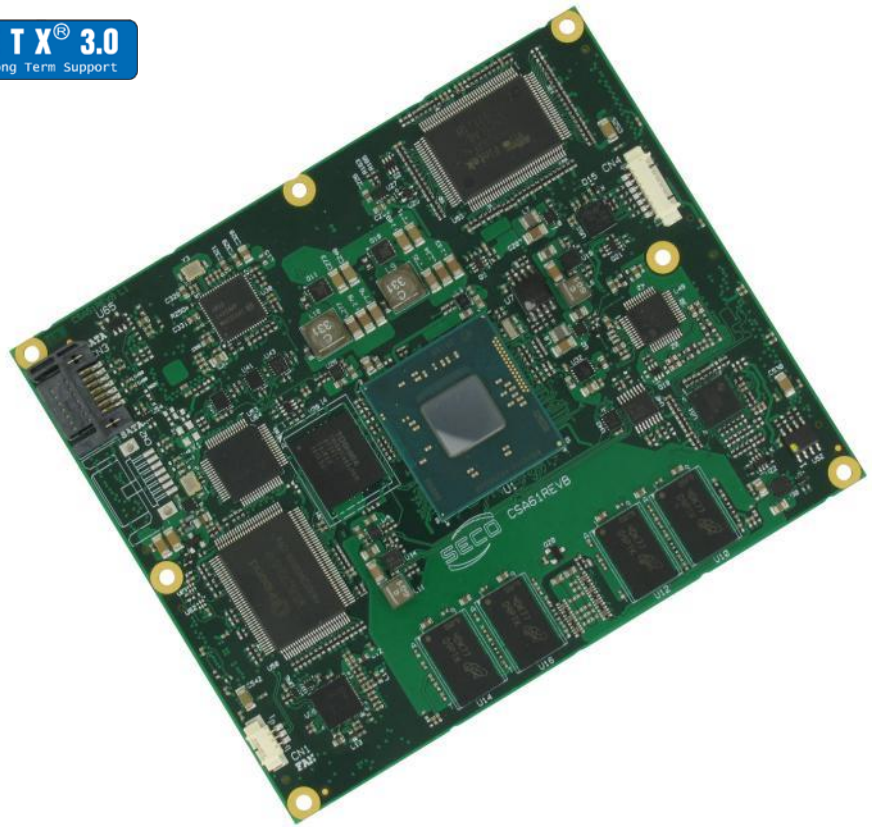
ETX / XTX

User Manual

ETX® 3.0
Long Term Support



ETX-A61

ETX® 3.0 compliant module with the
Intel® Atom™ E3800 and Celeron® Bay Trail family
SOCs

SECO

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	2nd December 2015	First Release	SB
1.1	26th January 2016	Minor corrections BIOS Section updated	SB
1.2	7th September 2017	Industrial temperature removed from Technical features ISA limitations added (par. 3.2.5.4.1) Double PATA configuration reset workaround added (par. 3.2.5.10.1) BIOS Section updated	SB

Every effort has been made to ensure the accuracy of this manual. However, SECO S.r.l. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.r.l. reserves the right to change precise specifications without prior notice to supply the best product possible.

Some of the information found in the BIOS SETUP Chapter has been extracted from the following copyrighted Insyde Software Corp. documents:

- InsydeH2O™ Setup Utility - User Reference Guide

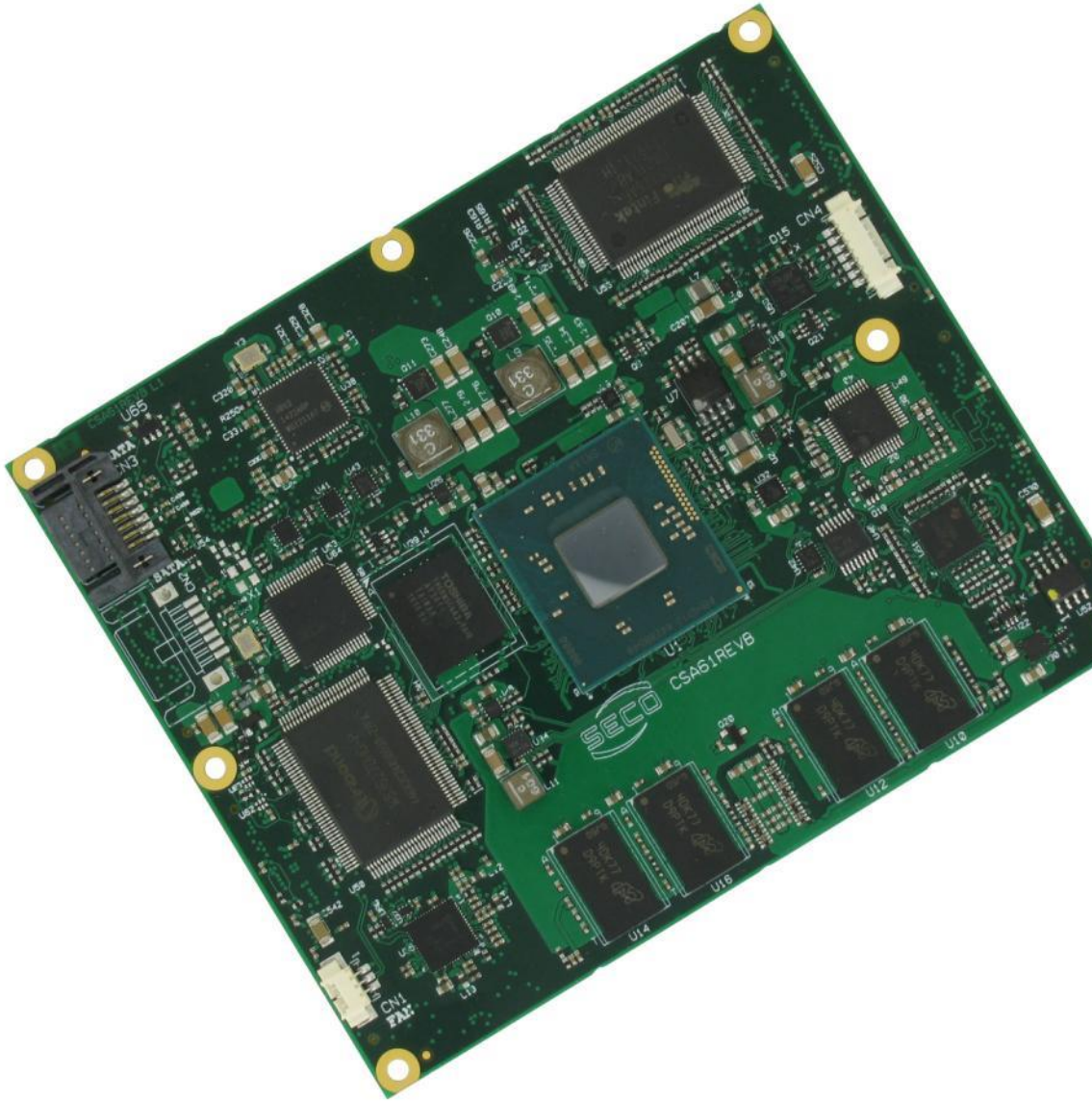
For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is read to assist you.

INDEX

Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.r.l. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.r.l. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434

- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before requesting technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The ETX-A61 module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The ETX-A61 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling an ETX-A61 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The ETX-A61 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operations modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CRT	Cathode Ray Tube. Initially used to indicate a type of monitor, this acronym has been used over time to indicate the analog video interface used to drive them.
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
DDR3	DDR, 3rd generation
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
EHCI	Enhanced Host Controller interface, a high-speed controller for USB ports, able to support USB2.0 standard
GbE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
ISA Bus	Industry Standard Architecture Bus, an old parallel bus for the connection of expansion boards.
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signaling, a standard for transferring data at very high speed using inexpensive twisted pairs copper cables, usually used for video applications
Mbps	Megabits per second
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable

N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OS	Operating System
PCI	Peripheral Component Interconnect, a parallel bus working at 33MHz for the connection of external expansion board
PCI-e	Peripheral Component Interconnect Express
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
PXE	Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like smart batteries and other power supply-related devices
TBM	To be measured
TMDS	Transition-Minimized Differential Signaling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
USB	Universal Serial Bus
V_REF	Voltage reference Pin
VGA	Video Graphics Array. An analog computer display standard, commonly referred to also as CRT.

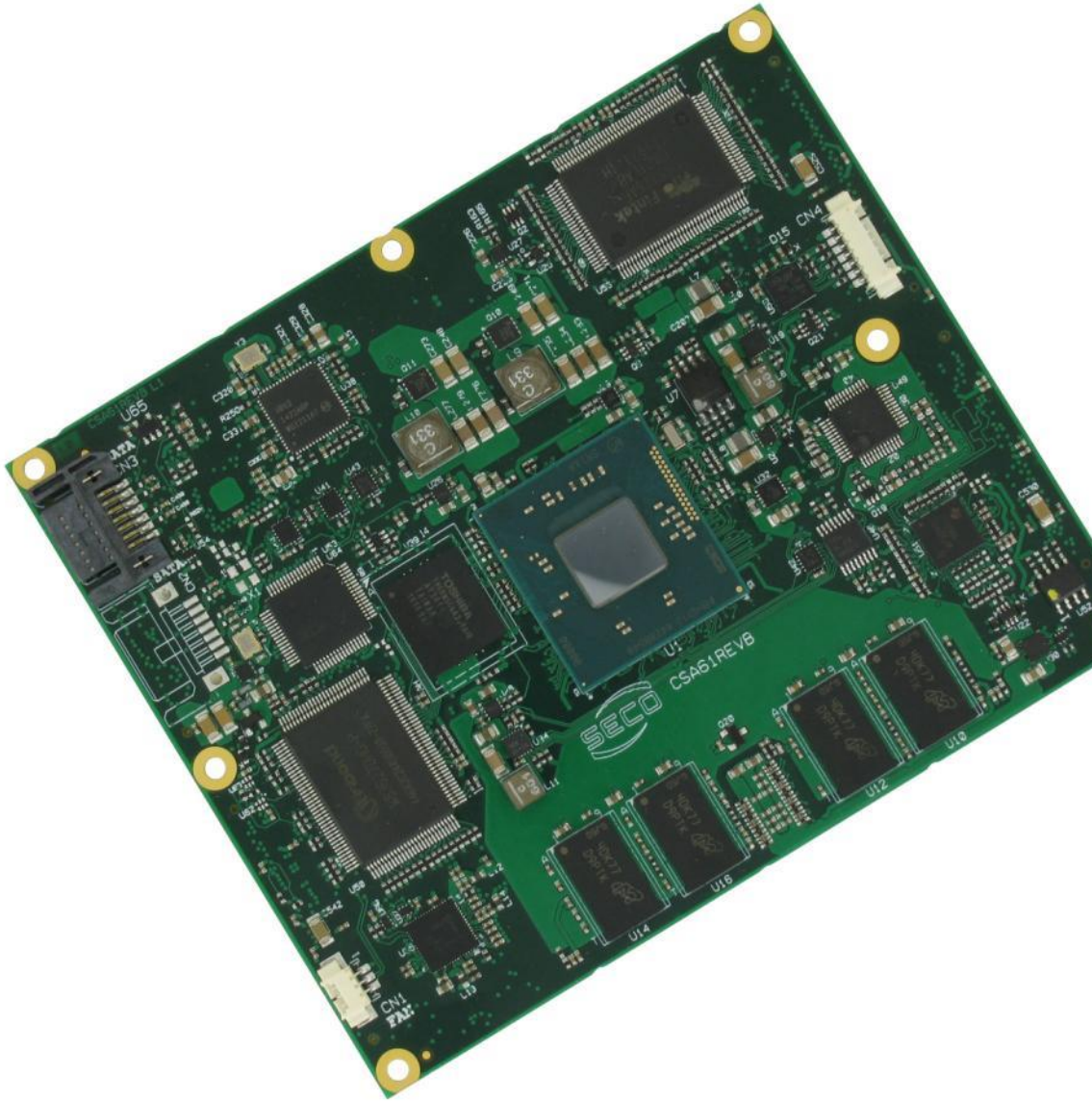
1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
DDC	http://www.vesa.org
ETX	http://www.etx-ig.org/specs/specs.php
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
MMC/eMMC	http://www.jedec.org/committees/jc-649
OpenGL	http://www.opengl.org
PCI	https://www.pcisig.com/specifications/conventional
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SM Bus	http://www.smbus.org/specs
UEFI	http://www.uefi.org
USB 2.0	http://www.usb.org/developers/docs/usb_20_070113.zip
Intel® Bay trail family	http://ark.intel.com/products/codename/55844/Bay-Trail#@Embedded

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram



2.1 Introduction

The ETX-A61 is a ETX® 3.0 compliant module, based on the Intel® family of System-on-Chips (SOCs) formerly coded as Bay Trail, a series of Single/ Dual / Quad Core SOCs with 64-bit instruction set. These SOCs embed all the features usually obtained by combination of CPU + platform Controller hubs, all in one single IC, which allows, therefore, the system minimisation and performance optimisation. A complete list of SOCs available is detailed in the next subchapter.

All the supported SOCs offer a 64-bit Instruction set, and provide direct access to the memory. Frequencies up to 1333MHz are supported, with a maximum capacity up to 8GB. Please notice that total amount of memory available is OS dependant, and depends also on the SOC.

All SOCs integrate an Intel® HD Graphics 4000 Series Controller, which offer high graphical performances, with support for Microsoft® DirectX11, OpenGL 3.0, OpenCL 1.2, OpenGL ES 2.0 and HW acceleration for video decoding of H.264, MPEG2, MVG, VC-1, VP8 and MJPEG video standards (for H.264, MPEG2 and MVG also HW encoding is offered). This embedded GPU is able to drive two independent displays; this can be obtained by exploiting both the native CRT (VGA) interface and the LVDS interface, which is realised through an eDP-to-LVDS bridge placed on one of the native Digital Display Interfaces available on the SOC.

For mass storage, on board it is possible to mount an optional eMMC disk. Furthermore, it is possible to connect external Hard Disk Drives by using the two native SATA channels of the SOC. ETX® specifications foresee the possibilities of having Parallel ATA interface on connector X4 and/or additional SATA connectors on top of the board. For this reason, since SATA channels available are only two, it is possible (as a factory option) to mount onboard one or two SATA-to-PATA bridges. Depending on the configuration purchased, therefore, it will be possible to have modules with two SATA connectors on top, **or** with two PATA interfaces on connector X4, **or** with one PATA interface on X4 and one SATA connector on top of the module.

The native HD Audio interface is connected to a Realtek ALC262 HD Audio Codec, so that it is possible to have analog audio channels (Stereo Output, Stereo auxiliary input and microphone input) on ETX connector X1.

Four USB 2.0 ports are supported directly by the SOC, ad are carried out directly on connector X1.

To complete the functionalities of the module, and make it compliant to ETX specifications, there are onboard a Gigabit Ethernet Controller (Intel® I210/I2111), which makes available the 10/100Mbps Ethernet interface, and a PCI-e-to-PCI bridge, to implement the PCI bus. Both these devices are managed by using two of the PCI-express ports #0 and #1, respectively.

Furthermore, on the LPC bus, are placed a LPC-to-ISA bridge, used to implement the ISA bus which characterize the ETX modules, and a Nuvoton SUperI/O, which makes available two full-modem serial ports, a parallel port shared with Floppy Disk interface, and PS/2 interface for Mouse and Keyboard.

The functionalities of this module are completed by the Real Time Clock, SM Bus, I2C Bus and the Watchdog. Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

The module has a very rugged design, since it is based on soldered down DDR3L memories, ceramic capacitors only and high quality AEC-Q200 grade-1 inductors. The possibility of having an embedded storage device, the eMMC, makes this module particularly suited for applications where vibrations can represent a problem that must be faced.

The product is ETX® Rel.3.0 standard compliant, an industry standard defined specifically for COMs (computer on modules) which require ensuring support for legacy peripherals (like those requiring ISA bus, PCI bus and/or PS/2 interface). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available.

2.2 Technical Specifications

SOC

Intel® Atom™ E3845, Quad Core @1.91GHz, 2MB Cache, 10W TDP
Intel® Atom™ E3827, Dual Core @1.75GHz, 1MB Cache, 8W TDP
Intel® Atom™ E3826, Dual Core @1.46GHz, 1MB Cache, 7W TDP
Intel® Atom™ E3825, Dual Core @1.33GHz, 1MB Cache, 6W TDP
Intel® Atom™ E3815, Single Core @1.46GHz, 512KB Cache, 5W TDP
Intel® Celeron® J1900, Quad Core @2.0GHz, 2MB Cache, 10W TDP
Intel® Celeron® N2930, Quad Core @1.83GHz, 2MB Cache, 7.5W TDP
Intel® Celeron® N2807, Dual Core @1.58GHz, 1MB Cache, 4.3W TDP

Memory

Soldered down DDR3L memory
E3845, E3827, J1900, N2930: up to 8GB Dual-Channel DDR3L 1333MHz
E3826: up to 8GB Dual-Channel DDR3L 1066MHz
N2807: up to 4GB Single-Channel DDR3L 1333MHz
E3825, E3815: up to 4GB Single-Channel DDR3L 1066MHz

Graphics

Integrated Intel® HD Graphics 4000 series controller
Dual independent display support
HW decoding of H.264, MPEG2, MVC, VC1, VP8, MJPEG formats
HW encoding of H.264, MPEG2 and MVC formats

Video Interfaces

VGA standard analog video interface
18/24 bit single/dual channel LVDS interface (VESA and JEIDA color mapping compatible)

Video Resolutions

CRT Interface:	up to 2560 x 1600 @ 60Hz
LVDS interface:	Up to 1920 x 1200 @ 60Hz

Mass Storage

Optional eMMC disk soldered on board
2 x external S-ATA **or** 2 x P-ATA or 1x P-ATA + 1 x S-ATA channels (factory options)
µSD Card Slot

USB

4 x USB 2.0 Host ports

Networking

Gigabit Ethernet controller, makes available a 10/100Mbps Ethernet interface

Audio

HD Audio codec, Realtek ALC262

Serial Ports

2 x Serial ports (TX/RX/RTS/CTS signals, TTL interface)

Other Interfaces

PCI Bus rel. 2.3 compliant, realised using a PCI-e to PCI bridge
ISA Bus, realised using a LPC to ISA bridge
LPT interface shared with Floppy Disk Drive interface
PS/2 mouse and keyboard interface
I2C Bus
SM bus
Watch Dog timer
Power Management Signals

Power supply voltage: +5V_{DC} ± 5% and + 5V_{SB} (optional)

Operating temperature: 0°C ÷ +60°C (commercial version) **

Dimensions: 114 x 95 mm (4.49" x 3.74")

! *** Temperatures indicated are the minimum and maximum temperature that the heatspreader / heatsink can reach in any of its parts. This means that it is customer's responsibility to use any passive cooling solution along with an application-dependent cooling system, capable to ensure that the heatspreader / heatsink temperature remains in the range above indicated. Please also check paragraph 5.1*

2.3 Electrical Specifications

According to ETX® specifications, the ETX-A61 board needs to be supplied only with an external $+5V_{DC}$ ± 5% voltage (+5V_S).

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. It must be provided using pin 8 (BATT) of connector X4 (CN7).

All these voltages are supplied directly through ETX Connectors X1 (CN6), X2 (CN5), X3 (CN8) and X4 (CN7).

All remaining voltages needed for board's working are generated internally from +5V_S power rail.

According to ETX® specifications, the +3.3V_S voltage present on connector X1 pins 12, 16 and 24 is generated internally; therefore, it must be considered as a power output for devices on the carrier board that need this voltage. According to ETX® specifications, maximum external load admitted on +3.3V_S power rail is 500mA.

! Since +3.3V_S is generated internally on ETX-A61 module, do not connect +3.3V_S pins to external 3.3V power supply units.

2.3.1 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_S: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_S, +5V_S.

_A: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_A, +3.3V_A.

_U: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_U.

2.3.2 Power Consumption

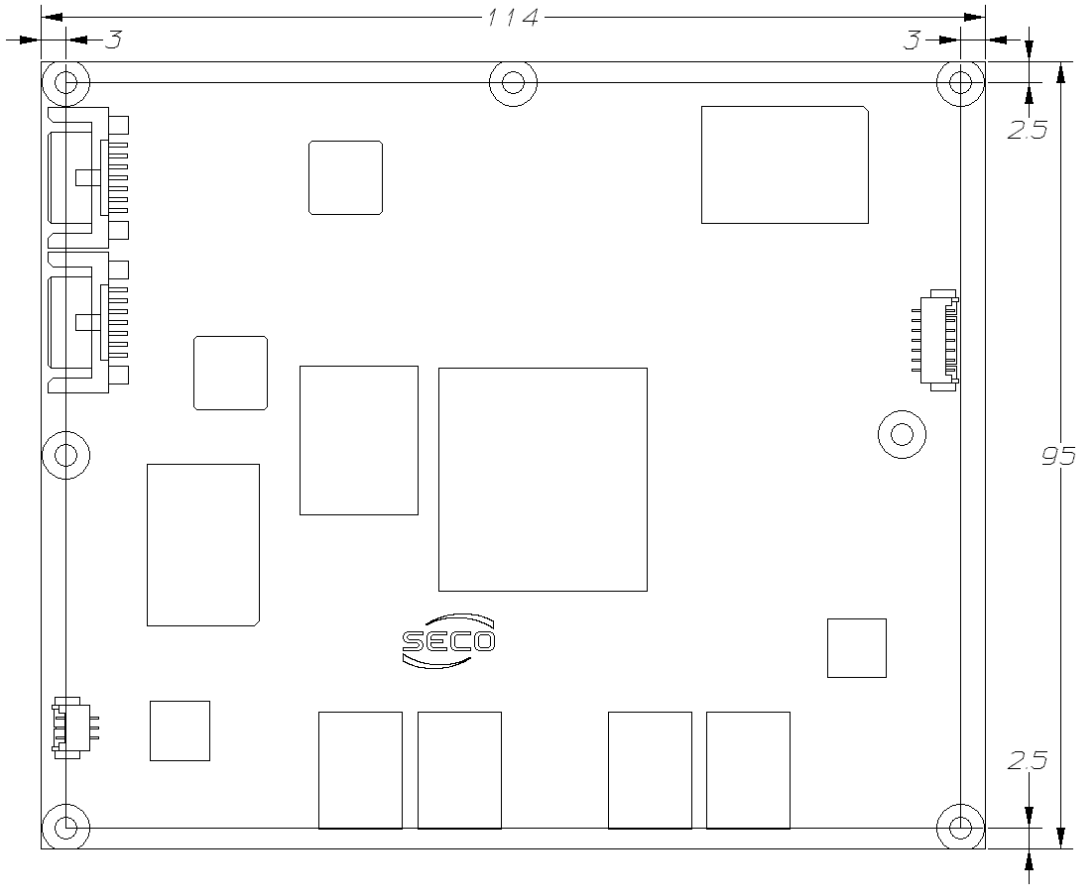
TBM

2.4 Mechanical Specifications

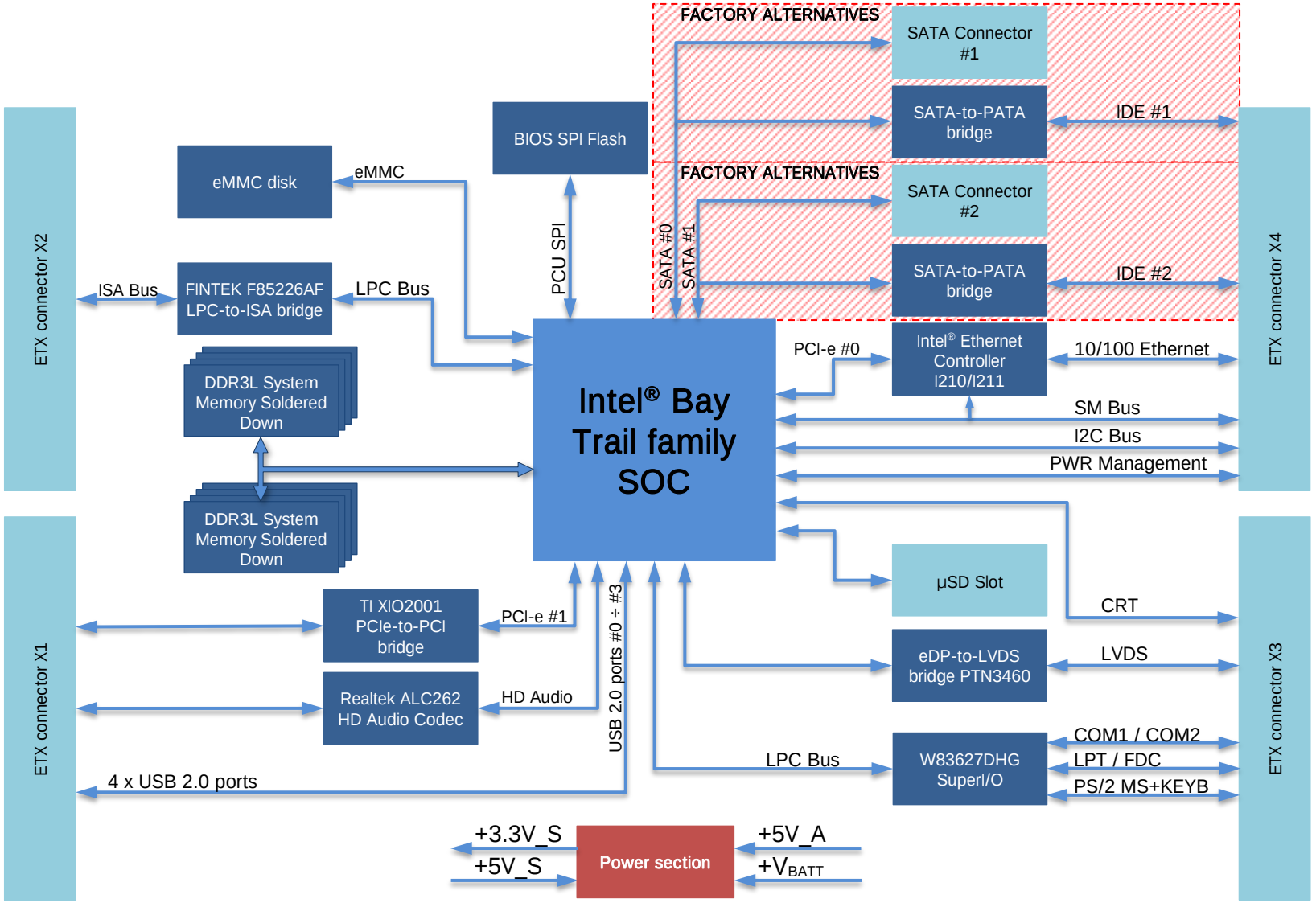
The ETX-A61 is an ETX® 3.0 compliant module; therefore its dimensions are 114 mm x 95 mm (4.49” x 3.74”).

Printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

The ETX plugs used will allow a clearance under the module of about 3mm. Since there are components on the bottom of the module, it is necessary to avoid placing any component on the carrier board in the area under the ETX® module.

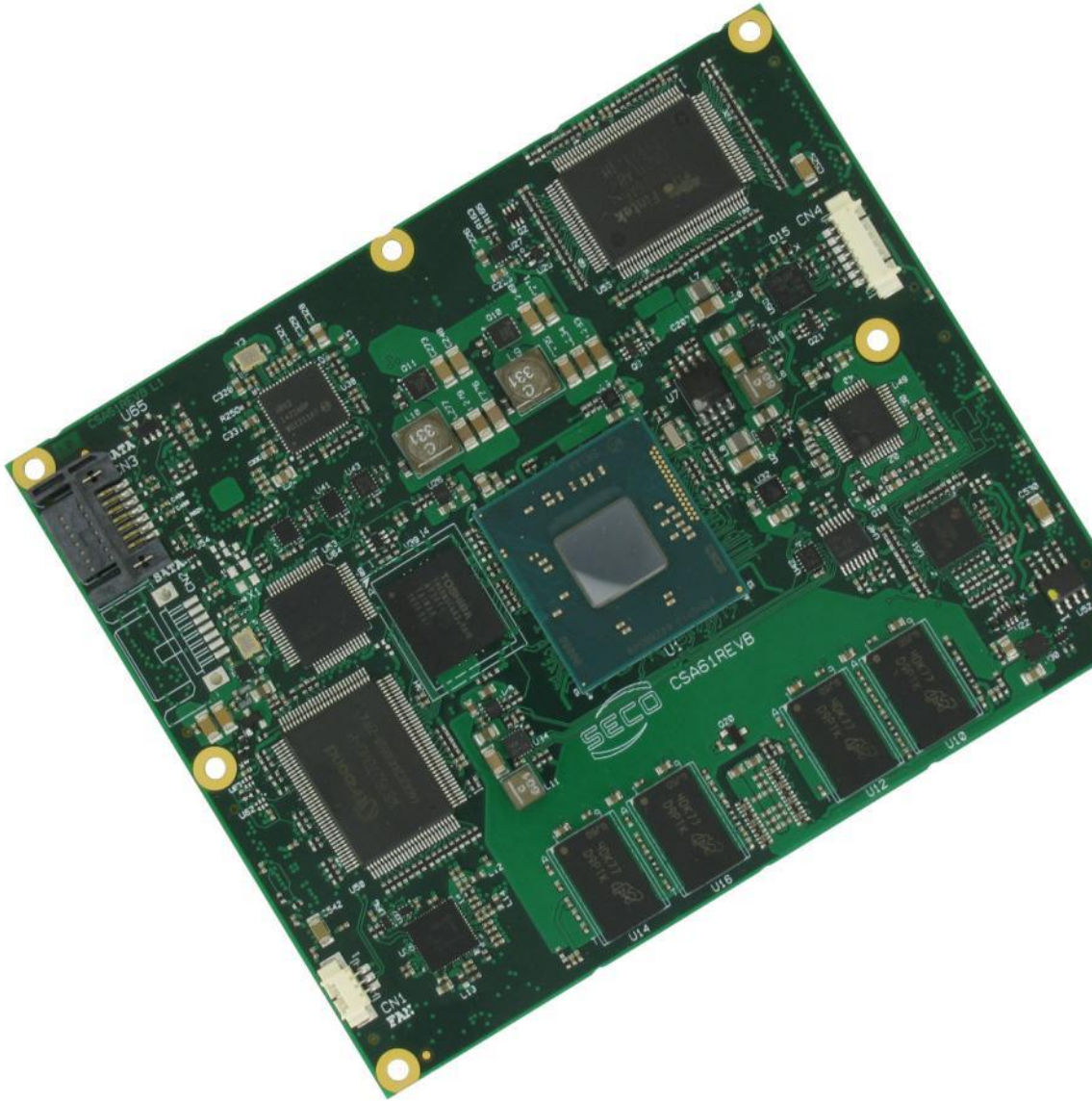


2.5 Block Diagram



Chapter 3.
CONNECTORS

- Introduction
- Connectors description



3.1 Introduction

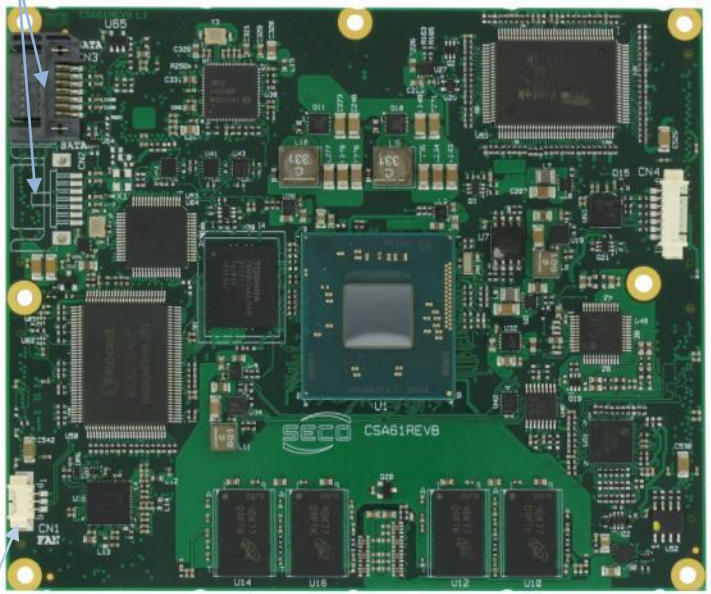
According to ETX® specifications, all interfaces to the board are available through two 220 pin connectors, for a total of 440 pin. Simplifying the terminology in this documentation, the primary connector is called A-B and the secondary C-D, since each one consists of two rows.

In addition, a Fan connector has been placed on one side of the board, in order to allow an easier connection of active heatsinks to the module.

! Please be aware that, depending on the configuration purchased, the appearance of the board could be different from the following pictures.

TOP SIDE

Optional SATA connectors

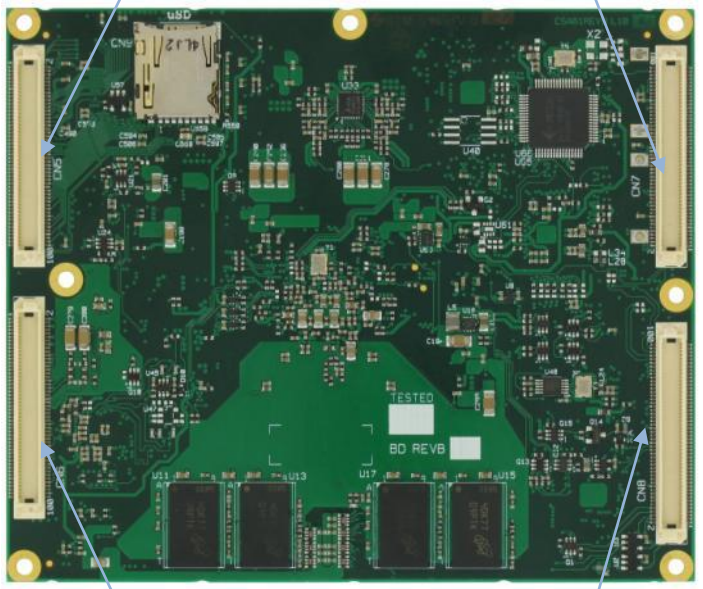


Ext. FAN Connector

BOTTOM SIDE

ETX connector X2

ETX connector X4



ETX connector X1

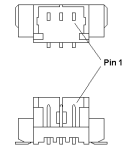
ETX connector X3

3.2 Connectors description

3.2.1 FAN Connector

FAN Connector - CN3	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN

Depending on the usage model of ETX-A61 module, for critical applications/environments on the module itself it is available a 3-pin dedicated connector for an external +5V$_{DC}$ FAN.



FAN Connector is a 3-pin single line SMT connector, type MOLEX 53261-0319 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

Please refer to chapter 5.1 for considerations about thermal dissipation.

FAN_POWER: +5V_S derived power rail for FAN, managed by the embedded microcontroller via PWM signal.

FAN_TACHO_IN: tachometric input from the fan to the embedded microcontroller, +3.3V_S electrical level signal.

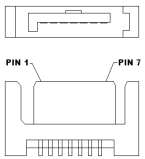
3.2.2 SATA connectors

Optional SATA #0 Connector - CN3	
Pin	**Signal**
1	GND
2	SATA0_TX+
3	SATA0_TX-
4	GND
5	SATA0_RX-
6	SATA0_RX+
7	GND

Optional SATA #1 Connector - CN2	
Pin	**Signal**
1	GND
2	SATA1_TX+
3	SATA1_TX-
4	GND
5	SATA1_RX-
6	SATA1_RX+
7	GND

The SOCs used on ETX-A61 module have an integrated S-ATA controller, which offers a SATA II, 3.0 Gps interface, capable to use up to two independent devices. These two channels can be carried out on externally on connectors CN2 and CN3, which are standard right-angle S-ATA connectors, to be used for connection of external Mass Storage Devices.

Both these connectors are optional, since the two SATA channels can be used (as a factory option) to drive a SATA-to-PATA bridge, which will make available the primary and/or the secondary IDE Channel on ETX connector X4 (CN7).



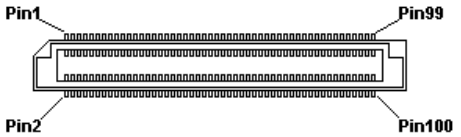
Please also check par. 3.2.5.10.

3.2.3 µSD Card Slot

The SOCs used on ETX-A61 module offer a SD 3.0 compliant interface, that can be used to implement another mass storages media other than the optional internal eMMC and the two SATA/PATA interfaces.

This SD interface is carried to a standard µSD card slot, soldered on top side of the module, push-push type.

3.2.4 ETX® Module connectors



For the connection of ETX® CPU modules, on board there are 4 connectors, type HIROSE FX8-100P-SV(92) (100 pin, ultra slim, 0.6mm pitch, h=2.45mm), according to the ETX® specifications.

The pinout of the module is compliant to ETX® specifications. Not all the signals contemplated in ETX® standard are implemented on the double connector, due to the functionalities really implemented on ETX-A61 board. Therefore, please refer to the following table for a list of effective signals reported on the connector. For accurate signals description, please consult the following paragraphs.

3.2.4.1 X1 CONNECTOR: PCI Bus, USB, Audio

ETX® Connector X1 - CN6							
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	1	2	GND	PWR	
PCI	O	PCICLK3	3	4	PCICLK4	O	PCI
	PWR	GND	5	6	GND	PWR	
PCI	O	PCICLK1	7	8	PCICLK2	O	PCI
PCI	I	REQ3#	9	10	GNT3#	O	PCI
PCI	O	GNT2#	11	12	+3.3V_S	PWR	
PCI	I	REQ2#	13	14	GNT1#	O	PCI
PCI	I	REQ1#	15	16	+3.3V_S	PWR	
PCI	O	GNT0#	17	18	N.C.	N.A.	
	PWR	+5V_S	19	20	+5V_S	PWR	
MISC	I	SERIRQ	21	22	REQ0#	I	PCI
PCI	I/O	AD0	23	24	+3.3V_S	PWR	
PCI	I/O	AD1	25	26	AD2	I/O	PCI
PCI	I/O	AD4	27	28	AD3	I/O	PCI
PCI	I/O	AD6	29	30	AD5	I/O	PCI
PCI	I/O	CBE0#	31	32	AD7	I/O	PCI
PCI	I/O	AD8	33	34	AD9	I/O	PCI
	PWR	GND	35	36	GND	PWR	
PCI	I/O	AD10	37	38	AUXAL	I	AUDIO
PCI	I/O	AD11	39	40	MIC	I	AUDIO

PCI	I/O	AD12	41	42	AUXAR	I	AUDIO
PCI	I/O	AD13	43	44	N.C.	PWR	AUDIO
PCI	I/O	AD14	45	46	SNDL	O	AUDIO
PCI	I/O	AD15	47	48	ASGND	PWR	AUDIO
PCI	I/O	CBE1#	49	50	SNDR	O	AUDIO
	PWR	+5V_S	51	52	+5V_S	PWR	
PCI	I/O	PAR	53	54	SERR#	I/O	PCI
PCI	I/O	GPERR#	55	56	N.C.	N.A.	
PCI	I	PME#	57	58	USB2-	I/O	USB
PCI	I/O	LOCK#	59	60	DEVSEL#	I/O	PCI
PCI	I/O	TRDY#	61	62	USB3-	I/O	USB
PCI	I/O	IRDY#	63	64	STOP#	I/O	PCI
PCI	I/O	FRAME#	65	66	USB2+	I/O	USB
	PWR	GND	67	68	GND	PWR	
PCI	I/O	AD16	69	70	CBE2#	I/O	PCI
PCI	I/O	AD17	71	72	USB3+	I/O	USB
PCI	I/O	AD19	73	74	AD18	I/O	PCI
PCI	I/O	AD20	75	76	USB0-	I/O	USB
PCI	I/O	AD22	77	78	AD21	I/O	PCI
PCI	I/O	AD23	79	80	USB1-	I/O	USB
PCI	I/O	AD24	81	82	CBE3#	I/O	PCI
	PWR	+5V_S	83	84	+5V_S	PWR	
PCI	I/O	AD25	85	86	AD26	I/O	PCI
PCI	I/O	AD28	87	88	USB0+	I/O	USB
PCI	I/O	AD27	89	90	AD29	I/O	PCI
PCI	I/O	AD30	91	92	USB1+	I/O	USB
PCI	O	PCIRST#	93	94	AD31	I/O	PCI
PCI	I	INTC#	95	96	INTD#	I	PCI
PCI	I	INTA#	97	98	INTB#	I	PCI
	PWR	GND	99	100	GND	PWR	

3.2.4.2 X2 CONNECTOR: ISA Bus

ETX® Connector X2 - CN5							
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	1	2	GND	PWR	
ISA	I/O	SD14	3	4	SD15	I/O	ISA
ISA	I/O	SD13	5	6	MASTER#	I	ISA
ISA	I/O	SD12	7	8	DREQ7	I	ISA
ISA	I/O	SD11	9	10	DACK7#	O	ISA
ISA	I/O	SD10	11	12	DREQ6	I	ISA
ISA	I/O	SD9	13	14	DACK6#	O	ISA
ISA	I/O	SD8	15	16	DREQ5	I	ISA
ISA	I/O	MEMW#	17	18	DACK5#	O	ISA
ISA	I/O	MEMR#	19	20	DREQ0	I	ISA
ISA	I/O	LA17	21	22	DACK0#	O	ISA
ISA	I/O	LA18	23	24	IRQ14	I	ISA
ISA	I/O	LA19	25	26	IRQ15	I	ISA
ISA	I/O	LA20	27	28	IRQ12	I	ISA
ISA	I/O	LA21	29	30	IRQ11	I	ISA
ISA	I/O	LA22	31	32	IRQ10	I	ISA
ISA	I/O	LA23	33	34	IO16#	I/O	ISA
	PWR	GND	35	36	GND	PWR	
ISA	I/O	SBHE#	37	38	M16#	I/O	ISA
ISA	I/O	SA0	39	40	OSC	O	ISA
ISA	I/O	SA1	41	42	BALE	I/O	ISA
ISA	I/O	SA2	43	44	TC	O	ISA
ISA	I/O	SA3	45	46	DACK2#	O	ISA
ISA	I/O	SA4	47	48	IRQ3	I	ISA
ISA	I/O	SA5	49	50	IRQ4	I	ISA
	PWR	+5V_S	51	52	+5V_S	PWR	

ISA	I/O	SA6	53	54	IRQ5	I	ISA
ISA	I/O	SA7	55	56	IRQ6	I	ISA
ISA	I/O	SA8	57	58	IRQ7	I	ISA
ISA	I/O	SA9	59	60	SYSCLK	O	ISA
ISA	I/O	SA10	61	62	REFSH#	O	ISA
ISA	I/O	SA11	63	64	DREQ1	I	ISA
ISA	I/O	SA12	65	66	DACK1#	O	ISA
	PWR	GND	67	68	GND	PWR	
ISA	I/O	SA13	69	70	DREQ3	I	ISA
ISA	I/O	SA14	71	72	DACK3#	O	ISA
ISA	I/O	SA15	73	74	IOR#	I/O	ISA
ISA	I/O	SA16	75	76	IOW#	I/O	ISA
ISA	I/O	SA18	77	78	SA17	I/O	ISA
ISA	I/O	SA19	79	80	SMEMR#	O	ISA
ISA	I/O	IOCHRDY	81	82	AEN	O	ISA
	PWR	+5V_S	83	84	+5V_S	PWR	
ISA	I/O	SD0	85	86	SMEMW#	O	ISA
ISA	I/O	SD2	87	88	SD1	I/O	ISA
ISA	I/O	SD3	89	90	NOWS#	I	ISA
ISA	I	DREQ2	91	92	SD4	I/O	ISA
ISA	I/O	SD5	93	94	IRQ9	I	ISA
ISA	I/O	SD6	95	96	SD7	I/O	ISA
ISA	I	IOCHK#	97	98	RSTDRV	O	ISA
	PWR	GND	99	100	GND	PWR	

3.2.4.3 X3 CONNECTOR: VGA, LVDS, COMs, LPT/FLOPPY, PS/2

ETX® Connector X3 - CN8							
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	1	2	GND	PWR	
VGA	O	R	3	4	B	O	VGA
VGA	O	HSY	5	6	G	O	VGA
VGA	O	VSY	7	8	DDCK	O	VGA
	N.A.	N.C.	9	10	DDDA	I/O	VGA
LVDS	O	LVDS_CLK_B-	11	12	LVDS_B3-	O	LVDS
LVDS	O	LVDS_CLK_B+	13	14	LVDS_B3+	O	LVDS
	PWR	GND	15	16	GND	PWR	
LVDS	O	LVDS_B1+	17	18	LVDS_B2+	O	LVDS
LVDS	O	LVDS_B1-	19	20	LVDS_B2-	O	LVDS
	PWR	GND	21	22	GND	PWR	
LVDS	O	LVDS_A3-	23	24	LVDS_B0+	O	LVDS
LVDS	O	LVDS_A3+	25	26	LVDS_B0-	O	LVDS
	PWR	GND	27	28	GND	PWR	
LVDS	O	LVDS_A2-	29	30	LVDS_CLK_A+	O	LVDS
LVDS	O	LVDS_A2+	31	32	LVDS_CLK_A-	O	LVDS
	PWR	GND	33	34	GND	PWR	
LVDS	O	LVDS_A0+	35	36	LVDS_A1+	O	LVDS
LVDS	O	LVDS_A0-	37	38	LVDS_A1-	O	LVDS
	PWR	+5V_S	39	40	+5V_S	PWR	
LVDS	I/O	JILI_DAT	41	42	LVDS_BLT_CTRL	O	LVDS
LVDS	I/O	JILI_CLK	43	44	BLON#	O	LVDS
LVDS	O	BIASON	45	46	DIGON	O	LVDS
	N.A.	N.C.	47	48	N.C.	N.A.	
	N.A.	N.C.	49	50	N.C.	N.A.	
PARALLEL	I	LPT/FLPY#	51	52	N.C.	N.A.	

	PWR	+5V_S	53	54	GND	PWR		
	O ---	STB# / ---	55	56	AFD# / DENSEL	O	O	PARALLEL
	N.A.	N.C.	57	58	PD7 / ---	I/O		PARALLEL
SERIAL	I	IRRX	59	60	ERR# / HDSEL#	I	O	PARALLEL
SERIAL	O	IRTX	61	62	PD6 / ---	I/O		PARALLEL
SERIAL	I	RXD2	63	64	INIT# / DIR#	O	O	PARALLEL
	PWR	GND	65	66	GND	PWR		
SERIAL	O	RTS2#	67	68	PD5 / ---	I/O		PARALLEL
SERIAL	O	DTR2#	69	70	SLIN# / STEP#	O	O	PARALLEL
SERIAL	I	DCD2#	71	72	PD4 / DSKCHG #	I/O	I	PARALLEL
SERIAL	I	DSR2#	73	74	PD3 / RDATA#	I/O	I	PARALLEL
SERIAL	I	CTS2#	75	76	PD2 / WP#	I/O	I	PARALLEL
SERIAL	O	TXD2#	77	78	PD1 /TRK0#	I/O	I	PARALLEL
SERIAL	I	RI2#	79	80	PD0 / INDEX#	I/O	I	PARALLEL
	PWR	GND	81	82	GND	PWR		
SERIAL	I	RXD1	83	84	ACK# / DRV#	I	O	PARALLEL
SERIAL	O	RTS1#	85	86	BUSY / MOT#	I	O	PARALLEL
SERIAL	O	DTR1#	87	88	PE / WDATA #	I	O	PARALLEL
SERIAL	I	DCD1#	89	90	SLCT / WGATE#	I	O	PARALLEL
SERIAL	I	DSR1#	91	92	MSCLK	I/OO		PS/2
SERIAL	I	CTS1#	93	94	MSDAT	I/O		PS/2
SERIAL	O	TXD1	95	96	KBCLK	I/O		PS/2
SERIAL	I	RI1#	97	98	KBDAT	I/O		PS/2
	PWR	GND	99	100	GND	PWR		

3.2.4.4 X4 CONNECTOR: IDE, ETHERNET, MISCELLANEOUS

ETX® Connector X4 - CN7							
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	1	2	GND	PWR	
	PWR	+5V_A	3	4	PWGIN	I	PWR_CTRL
PWR_CTRL	O	PS_ON#	5	6	SPEAKER	O	MISC
PWR_CTRL	I	PWRBTN#	7	8	BATT	PWR	
MISC	I	KBINH#	9	10	LILED#	O	ETHERNET
PWR_MGMT	I	RSMRST#	11	12	ACTLED#	O	ETHERNET
	N.A.	N.C.	13	14	SPEEDLED#	O	ETHERNET
	N.A.	N.C.	15	16	I2CLK	I/O	MISC
	PWR	+5V_S	17	18	+5V_S	PWR	
USB	I	OVCR#	19	20	GPCS#	O	MISC
PWR_MGMT	I	EXTSMI#	21	22	I2DAT	I/O	MISC
MISC	I/O	SMBCLK	23	24	SMBDATA	I/O	MISC
IDE	O	SIDE_CS3#	25	26	SMBALRT#	I	PWR_MGMT
IDE	O	SIDE_CS1#	27	28	N.C.	N.A.	
IDE	I/O	SIDE_A2	29	30	PIDE_CS3#	O	IDE
IDE	I/O	SIDE_A0	31	32	PIDE_CS1#	O	IDE
	PWR	GND	33	34	GND	PWR	
	N.A.	N.C.	35	36	PIDE_A2	I/O	IDE
IDE	I/O	SIDE_A1	37	38	PIDE_A0	I/O	IDE
IDE	I	SIDE_INTRQ	39	40	PIDE_A1	I/O	IDE
PWR_MGMT	I	BATLOW#	41	42	GPE1#	I	PWR_MGMT
IDE	O	SIDE_AK#	43	44	PIDE_INTRQ	I	IDE
IDE	I	SIDE_RDY	45	46	PIDE_AK#	O	IDE
IDE	O	SIDE_IOR#	47	48	PIDE_RDY	I	IDE
	PWR	+5V_S	49	50	+5V_S	PWR	

IDE	O	SIDE_IOW#	51	52	PIDE_IOR#	O	IDE
IDE	I	SIDE_DRQ	53	54	PIDE_IOW#	O	IDE
IDE	I/O	SIDE_D15	55	56	PIDE_DRQ	I	IDE
IDE	I/O	SIDE_D0	57	58	PIDE_D15	I/O	IDE
IDE	I/O	SIDE_D14	59	60	PIDE_D0	I/O	IDE
IDE	I/O	SIDE_D1	61	62	PIDE_D14	I/O	IDE
IDE	I/O	SIDE_D13	63	64	PIDE_D1	I/O	IDE
	PWR	GND	65	66	GND	PWR	
IDE	I/O	SIDE_D2	67	68	PIDE_D13	I/O	IDE
IDE	I/O	SIDE_D12	69	70	PIDE_D2	I/O	IDE
IDE	I/O	SIDE_D3	71	72	PIDE_D12	I/O	IDE
IDE	I/O	SIDE_D11	73	74	PIDE_D3	I/O	IDE
IDE	I/O	SIDE_D4	75	76	PIDE_D11	I/O	IDE
IDE	I/O	SIDE_D10	77	78	PIDE_D4	I/O	IDE
IDE	I/O	SIDE_D5	79	80	PIDE_D10	I/O	IDE
	PWR	+5V_S	81	82	+5V_S	PWR	
IDE	I/O	SIDE_D9	83	84	PIDE_D5	I/O	IDE
IDE	I/O	SIDE_D6	85	86	PIDE_D9	I/O	IDE
IDE	I/O	SIDE_D8	87	88	PIDE_D6	I/O	IDE
PWR_MGMT	I	GPE2#	89	90	N.C.	N.A.	
ETHERNET	I	RXD-	91	92	PIDE_D8	I/O	IDE
ETHERNET	I	RXD+	93	94	SIDE_D7	I/O	IDE
ETHERNET	O	TXD-	95	96	PIDE_D7	I/O	IDE
ETHERNET	O	TXD+	97	98	HDRST#	O	IDE
	PWR	GND	99	100	GND	PWR	

3.2.5 Signals description

3.2.5.1 PCI Signals (connector X1 - CN6)

Since the SOCs used on ETX-A61 module doesn't offer native support for PCI bus (which is required by ETX® specifications), this kind of interface is realised using a PCI-express to PCI bridge (Texas Instruments® XIO2001). This allows implementing a PCI bus compliant to PCI Local specifications rel. 2.3.

All signals are 3.3V voltage tolerant.

Here following the signals related to the PCI Bus.

PCICLK[1..4]: PCI clock outputs, for driving up to 4 external PCI slots or devices.

REQ[0..3]#: PCI Bus Request, +3.3V_S active low inputs with 10kΩ pull-up resistor. Used by external bus mastering devices to request PCI bus ownership.

GNT[0..3]#: PCI Bus Grant, +3.3V_S active low outputs. Used by the arbiter to grant the ownership of the bus.

AD[0..31]: PCI address and Data Bus lines, +3.3V_S bidirectional signals.

CBE[0..3]#: PCI Bus command and byte enable, +3.3V_S active low bidirectional signals. Multiplexed signals, used during the address phase and during the data phase of a transaction respectively to transfer a command and enable byte lanes.

PAR: PCI bus parity bit, +3.3V_S bidirectional signal.

SERR#: System Error, +3.3V_S active low bidirectional signals with 10kΩ pull-up resistor. Used to signals system errors

GPERR#: PCI bus Parity Error, +3.3V_S active low bidirectional signals with 10kΩ pull-up resistor. Used to report data parity errors during PCI transactions.

PME#: Power Management Event, +3.3V_A active low input signal with 10kΩ pull-up resistor. Used by external devices to request a change in the device or system power states.

LOCK#: Lock Resource, +3.3V_S active low bidirectional signals with 10kΩ pull-up resistor. This signal is used to require exclusive use of the bus to complete an atomic operation that otherwise could require multiple transactions.

DEVSEL#: PCI Device Select, +3.3V_S active low bidirectional signals with 10kΩ pull-up resistor. This signal is driven low by any device that, during a PCI transaction, has decoded its own address as the target of the transaction.

TRDY#: PCI Target Ready, +3.3V_S active low bidirectional signals with 10kΩ pull-up resistor. Used by the targeted device to signal that it is ready to complete the transaction.

IRDY#: PCI Initiator Ready, +3.3V_S active low bidirectional signals with 10kΩ pull-up resistor. Used by the Bus Master to signal that it is ready to complete the transaction.

STOP#: PCI Stop, +3.3V_S active low bidirectional signals with 10kΩ pull-up resistor. Used by the targeted device to request to the bus master to stop the current transaction.

FRAME#: PCI Cycle Frame indicator, +3.3V_S active low bidirectional signals with 10kΩ pull-up resistor. This signal is used by the Bus Master to indicate the beginning of a transaction, and remains low (asserted) until the transaction is finished or in the final phase.

PCIRST#: PCI Reset, +3.3V_S active low output with 10kΩ pull-up resistor. It is driven low during system reset to reset the whole PCI bus

INTA#, INTB#, INTC#, INTD#: PCI interrupt lines, +3.3V_S active low inputs with 10kΩ pull-up resistor.

3.2.5.2 USB interface signals (connector X1 - CN6)

Intel® Bay Trail family of SOCs embeds one EHCI controller, which is able to manage up to four USB 1.x / 2.0 Host ports.

On ETX-A61 module, these four USB 2.0 ports are carried out directly on connector X1 (CN6). All of them are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Via BIOS it is possible to enable or disable singularly each USB port.

Here following the signals related to USB interfaces.

USB0+/USB0-: Universal Serial Bus Port #0 bidirectional differential pair.

USB1+/USB1-: Universal Serial Bus Port #1 bidirectional differential pair.

USB2+/USB2-: Universal Serial Bus Port #2 bidirectional differential pair.

USB3+/USB3-: Universal Serial Bus Port #3 bidirectional differential pair.

OVCR#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin (available on connector X4 - CN7) has to be used for overcurrent detection of USB Ports of ETX-A61 module

Please notice that for correct management of Overcurrent signals, power distribution switches are needed on the carrier board.

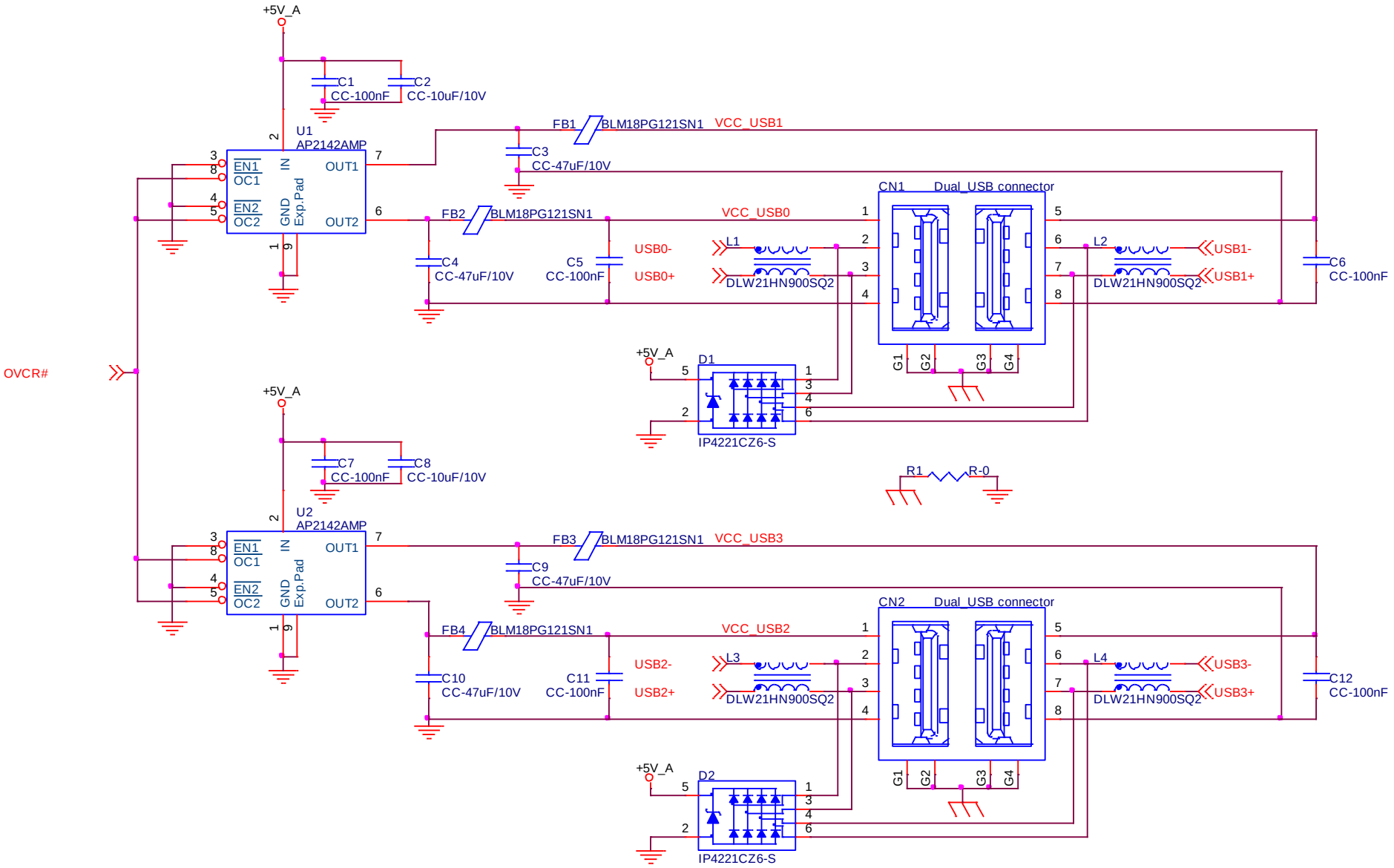
For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

The schematics in the following page show an example of implementation on the Carrier Board. In there, all USB ports #0, #1, #2 and #3 are carried out to standard USB 2.0 Type A receptacles.

All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.r.l. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design


+5V_A
C1
CC-100nF
C2
CC-10uF/10V
U1
AP2142AMP
EN1
OC1
EN2
OC2
IN
GND
Exp.Pad
OUT1
OUT2
FB1
BLM18PG121SN1
VCC_USB1
C3
CC-47uF/10V
FB2
BLM18PG121SN1
VCC_USB0
C4
CC-47uF/10V
C5
CC-100nF
USB0-
USB0+
L1
DLW21HN900SQ2
CN1
Dual_USB connector
L2
DLW21HN900SQ2
USB1-
USB1+
C6
CC-100nF
OVCR#
D1
IP4221CZ6-S
G1
G2
G3
G4
R1
R-0
C7
CC-100nF
C8
CC-10uF/10V
U2
AP2142AMP
FB3
BLM18PG121SN1
VCC_USB3
C9
CC-47uF/10V
FB4
BLM18PG121SN1
VCC_USB2
C10
CC-47uF/10V
C11
CC-100nF
USB2-
USB2+
L3
DLW21HN900SQ2
CN2
Dual_USB connector
L4
DLW21HN900SQ2
USB3-
USB3+
C12
CC-100nF
D2
IP4221CZ6-S

3.2.5.3 Audio interface signals (connector X1 - CN6)

The ETX-A61 module supports HD audio format, thanks to native support offered by the processor to this audio codec standard.

A Realtek ALC262 HD audio coded is embedded onboard. By using this codec, the ETX-A61 module is able to support the following audio signals.

SNDL/SNDR: Left and Right stereo output, ~1Vrms.

AUXAL/AUXAR: Left and Right auxiliary inputs, ~1Vrms

MIC: Microphone Input, ~1Vrms

ASGND: Analog ground reference. To be used on the carrier board for definition of an analog plane where tracing all audio signals.

3.2.5.4 ISA Signals (connector X2 - CN5)

Since the SOCs used on ETX-A61 module doesn't offer native support for ISA bus (which is required by ETX® specifications), this kind of interface is realised using an LPC to ISA bridge (Fintek F85226AF).

All signals are 5V voltage tolerant.

Here following the signals related to the ISA Bus.

SD[0..15]: 16-bit System data bus, TTL bidirectional signals with 8k2Ω pull-up resistor to +5V_S.

SA[0..19]: System address bus, TTL bidirectional signals with 8k2Ω pull-up resistor to +5V_S. This bus allows addressing up to 1MB of ISA I/O space.

LA[17..23]: Latched address bus, TTL bidirectional signals with 8k2Ω pull-up resistor to +5V_S. Along with signals SA[0..16], this bus is used to address memory space up to 16MB.

SBHE#: System Byte High Enable, TTL bidirectional signal. It is asserted when a byte is transferred on data bus SD[8..15].

BALE: Bus Address Latch Enable, TTL bidirectional signal. It indicates that SA[0..19] bus, LA[17..23] bus and SBHE# signal are valid.

AEN: Address Enable, +5V tolerant output with 24mA source-sink capability. It indicates that a DMA cycle is currently performed.

MEMR#: Memory Read, TTL bidirectional signal with 8k2Ω pull-up resistor to +5V_S. It is used to indicate that the current cycle is a memory read.

SMEMR#: System Memory Read, TTL output with 1kΩ pull-up resistor at +5V_S. It is used to indicate that the current cycle is a system memory read under 1MB.

MEMW#: Memory Write, TTL bidirectional signal with 8k2Ω pull-up resistor to +5V_S. It is used to indicate that the current cycle is a memory write.

SMEMW#: System Memory Write, TTL output with 1kΩ pull-up resistor at +5V_S. It is used to indicate that the current cycle is a system memory write access under 1MB.

IOR#: I/O Read, TTL bidirectional signal with 8k2Ω pull-up resistor to +5V_S. It is asserted to request an ISA I/O slave to drive data onto the data bus.

IOW#: I/O Write, TTL bidirectional signal with 8k2Ω pull-up resistor to +5V_S. It is asserted to request an ISA I/O slave to accept the data currently available on the data bus.

IOCHK#: I/O Check, TTL input and Schmitt Trigger with 4k7Ω pull-up resistor to +5V_S. This signal is driven by the ISA I/O devices to indicate that an error has occurred, therefore requiring a NMI.

IOCHRDY: I/O Check, TTL bidirectional signal with 1kΩ pull-up resistor to +5V_S. When this signal is asserted, it means that an I/O device is requiring additional Wait states to complete its transactions.

M16#: 16-bit Memory Chip Select, TTL bidirectional signal with 1kΩ pull-up resistor to +5V_S. This signal is activated (driven low) each time that the memory slave device supports 16-bit accesses.

IO16#:16-bit I/O Chip Select, TTL bidirectional signal with 1kΩ pull-up resistor to +5V_S. This signal is activated (driven low) each time that the I/O device supports 16-bit I/O cycles.

REFSH#: Refresh Cycle indicator, output signal with 24mA source-sink capability, with 1kΩ pull-up resistor to +5V_S. This signal is driven low each time that a refresh cycle is performed to prevent loss of memory contents.

NOWS#: No Wait States signal, TTL input and Schmitt Trigger with 1kΩ pull-up resistor to +5V_S. This signal is driven by the targeted I/O device each time it wants to signal that it is able to perform the transaction in the current cycle without needing additional wait states.

MASTER#: Master signal, TTL input and Schmitt Trigger with 8k2Ω pull-up resistor to +5V_S. When this input is activated (low), then a ISA bus master is currently driving the ISA bus. This signal is associated to a DREQ line by an ISA master when it wants take the control of the ISA Bus.

SYSCLK: ISA bus reference clock (circa 8MHz), output.

OSC: 14.318 MHz ISA Clock output.

RESETDRV: Reset, output signal with 24mA source-sink capability. It is used to reset external devices connected to ISA bus.

DREQ[0,1,2,3,5,6,7]: DMA request, TTL inputs (5V tolerant) with 8k2Ω pull-down resistors. All of these signals can be driven by external devices when they need DMA access to the memory.

DACK[0,1,2,3,5,6,7]#: DMA request Acknowledge, 5V tolerant outputs with 24mA source-sink capability. These signals are asserted when it has been granted the DMA access on the corresponding DMA channel.

TC: Terminal Count signal, 5V tolerant output with 24mA source-sink capability. It signals the ending of a DMA transfer.

IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15: Interrupt Request lines (inactive high), TTL inputs with 8k2Ω pull-up resistors to +5V_S.

3.2.5.4.1 ISA BUS LIMITATIONS

As already specified in the previous paragraph, the Intel® family of SoCs formerly coded as Bay trail do not support natively the ISA bus, which is required by ETX® specifications.

Therefore, this interface is realised using an LPC to ISA bridge (Fintek F85226AF), which causes the following limitations in using ISA Bus:

- DMA transfers are not supported;
- Memory Accesses are 8-bit at a time;
- It is not possible to access to any area located under 1MB because of Bay Trail's limits;
- Memory access in the 0xF0000000-0xF0FFFFFF window are translated into ISA access in the range 0xF0000000 ÷ 0xF0FFFFFF, which is a 16MB-1 window
- Memory accesses in the area 0xF0000000-0xF00FFFFF, i.e. accesses in the lower 1MB area translated in addressable area, are handled like if the access were above 1MB. This means that signals SMEMR# / SMEMW# will not change, only MEMR# and MEMW# will do.

3.2.5.5 Analog VGA interface (Connector X3 - CN8)

The SOCs used on ETX-A61 module can manage directly one analog display interface, which can be used for the connection of older VGA/CRT displays.

Signals dedicated to VGA interface are the following:

R: SOC's internal DAC's Red Signal video output.

G: SOC's internal DAC's Green Signal video output.

B: SOC's internal DAC's Blue Signal video output.

HSY: SOC's internal DAC's Horizontal Synchronization output signal, electrical level +5V_S.

VSY: SOC's internal DAC's Vertical Synchronization output signal, electrical level +5V_S.

DDCK: internal DAC's DDC Clock line for VGA displays detection. Output signal, electrical level +5V_S with 2K2Ω pull-up resistor.

DDDA: internal DAC's DDC Data line for VGA displays detection. Bidirectional signal, electrical level +5V_S with 2K2Ω pull-up resistor.

Please be aware that for the connection to external VGA displays, on the carrier board it is necessary to provide for filters and ESD protection.

3.2.5.6 LVDS Flat Panel signals (Connector X3 - CN8)

The Intel® Bay Trail family of SOCs offer only two Digital Display Interfaces for the video, and doesn't offer the support for LVDS interface, which is conversely much used in many application fields, and is one of the two possible flat-panel interfaces required by the ETX® specifications.

For this reason, on ETX-A61 there is an eDP-to-LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hz (dual channel mode).

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Channel #A differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Channel #A differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Channel #A differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Channel #A differential data pair #3.

LVDS_CLK_A+/LVDS_CLK_A-: LVDS Channel #A differential clock.

LVDS_B0+/LVDS_B0-: LVDS Channel #B differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Channel #B differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Channel #B differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Channel #B differential data pair #3.

LVDS_CLK_B+/LVDS_CLK_B-: LVDS Channel #B differential Clock

BIASON: Analog Dimming, +5V signal, derived from the PWM signal LVDS_BLT_CTRL coming from COM Express module, for direct analogic control of backlights not supporting PWM.

DIGON: +3.3V_S electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display.

BLON#: +3.3V_S electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display.

LVDS_BLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

JILI_DAT: DisplayID DDC Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

JILI_CLK: DisplayID DDC Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

3.2.5.7 Serial port interface signals (Connector X3 - CN8)

According to ETX® Rel. 3.0 specifications, the ETX-A61 module offers two UART interfaces, which are managed by the LPC Super I/O Nuvoton W83627DHG.

Here following the signals related to UART interfaces:

DTR1#, DTR2#: Data Terminal Ready active low outputs, 3.3V_S electrical level. This is a handshake signal used to notify to the DCE (Data Communication Equipment) that the DTE (Data Terminal Equipment) is ready to establish a data-communication link.

RI1#, RI2#: Ring Indicator active low inputs, 3.3V_S electrical level. This is a handshake signal that the DCE uses to signal to the DTE that a telephone ring has been detected.

TXD1, TX2: Serial Data Transmitter outputs, 3.3V_S electrical level.

RXD1, RXD2: Serial Data Receiver inputs, 3.3V_S electrical level.

CTS1#, CTS2#: Clear To Send active low inputs, 3.3V_S electrical level. This handshake signal is used to notify to the DTE that the DCE is ready to receive data-

RTS1#, RTS2#: Request to Send active low outputs, 3.3V_S electrical level. These handshake signals are used to notify to the DCE that the DTE is ready to transmit data.

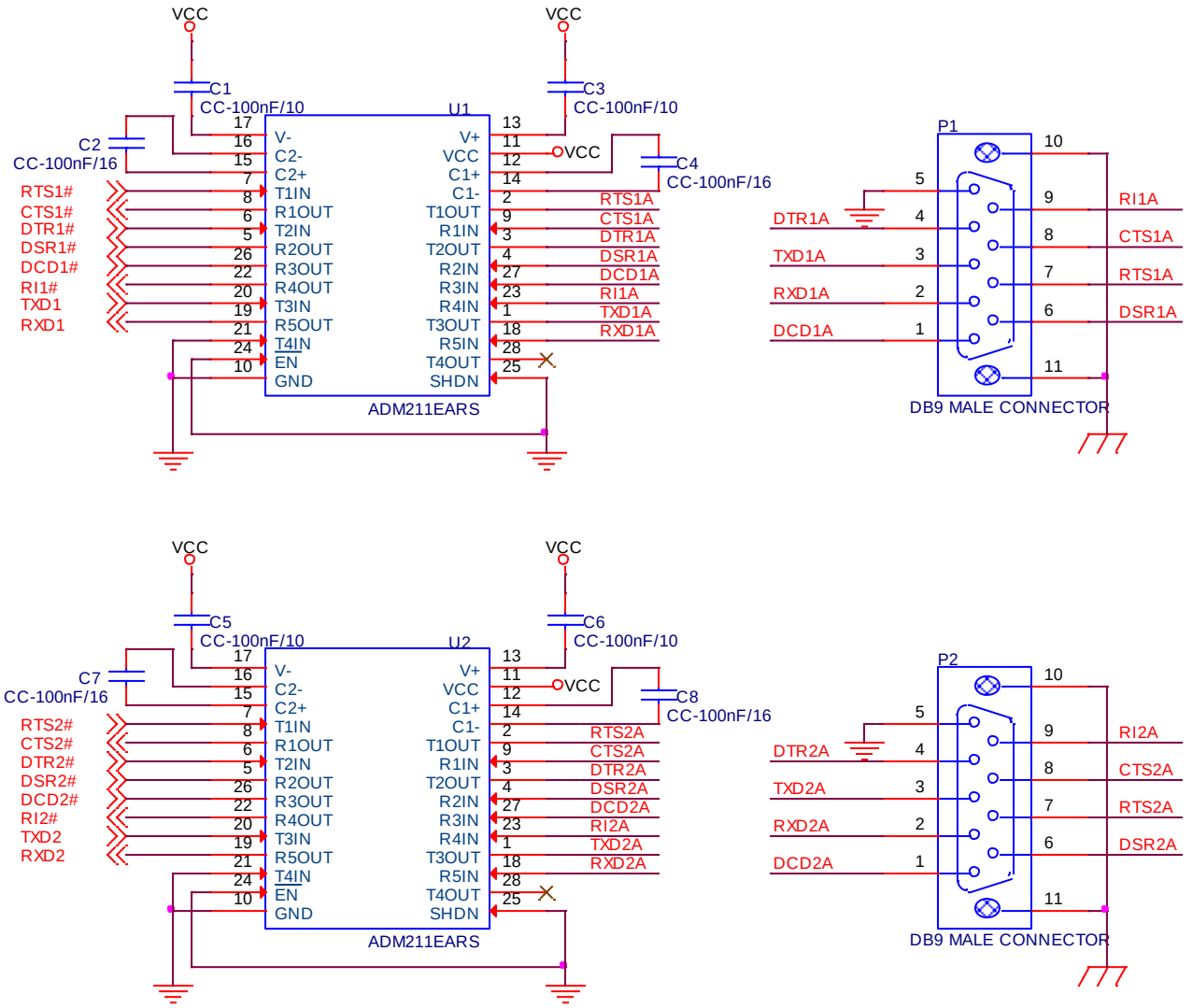
DCD1#, DCD2#: Data Carrier Detect active low inputs, 3.3V_S electrical level. Handshake signal used to notify to the DTE that a carrier signal has been detected by the DCE.

DSR1#, DSR2#: Data Set Ready active low inputs, 3.3V_S electrical level. Handshake signal used to notify to the DTE that the DCE is ready to establish a data-communication link.

IRRX, IRTX: Infrared receive and transmit Data. These two signals are not a different serial port. Instead, they are hardwired, respectively, to RXD2 and TXD2 signals.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it is not necessary to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The schematic in the next page shows an example of implementation of RS-232 transceiver for the Carrier board.


VCC
C1
CC-100nF/10
C2
CC-100nF/16
U1
ADM211EARS
V-
C2-
C2+
T1IN
R1OUT
T2IN
R2OUT
R3OUT
R4OUT
T3IN
R5OUT
T4IN
EN
GND
V+
VCC
C1+
C1-
T1OUT
R1IN
T2OUT
R2IN
R3IN
R4IN
T3OUT
R5IN
T4OUT
SHDN
C3
C4
RTS1#
CTS1#
DTR1#
DSR1#
DCD1#
RI1#
TXD1
RXD1
RTS1A
CTS1A
DTR1A
DSR1A
DCD1A
RI1A
TXD1A
RXD1A
P1
DB9 MALE CONNECTOR
C5
C6
C7
C8
U2
RTS2#
CTS2#
DTR2#
DSR2#
DCD2#
RI2#
TXD2
RXD2
RTS2A
CTS2A
DTR2A
DSR2A
DCD2A
RI2A
TXD2A
RXD2A
P2

3.2.5.8 PS/2 interface signals (Connector X3 - CN8)

The LPC Super I/O Nuvoton W83627DHG manages also a PS/2 interface, which is available on connector X3 - CN8.

Here following the signals related to PS/2 interface:

KBDAT: PS/2 Keyboard Data, +5V_A bidirectional signal with 4K7Ω pull-up resistor.

KBCLK: PS/2 Keyboard Clock, +5V_A bidirectional signal with 4K7Ω pull-up resistor.

MSDAT: PS/2 Mouse Data, +5V_A bidirectional signal with 4K7Ω pull-up resistor.

MSCLK: PS/2 Mouse Clock, +5V_A bidirectional signal with 4K7Ω pull-up resistor.

3.2.5.9 Parallel port /Floppy Disk interface signals (Connector X3 - CN8)

According to ETX® Rel. 3.0 specifications, the ETX-A61 module offers also a Parallel Port interface. The pins used for this interface are also shared with Floppy Disk Controller interface. Both these interfaces are managed by the LPC Super I/O Nuvoton W83627DHG.

Selection between these two interfaces is made using signal LPT/FLPY#, which is a +3.3V_S input with 10KΩ pull-up resistor. When this signal is high (or not driven), then Parallel Port interface is available. Instead, when the signal is low, then Floppy Disk Interface will be available

Parallel Port mode signals:

STB# Strobe, active-low open drain output. This signal is used to let the printer to latch the data available on parallel data bus.

AFD#: AutoFeed, active low open drain output. This signal commands to the printer to add automatically a line after that one line has been printed.

PD[0..7]: 8-bit bidirectional parallel data bus, TTL level. It is used to transfer data between the CPU and the printer.

ERR#: Error, active-low input, TTL level. This signals reports that an error has occurred with the printer.

INIT#: Initialization, active-low open drain output. When asserted, this signal commands the initialization of the printer.

SLIN#: Selection, active-low open drain output. It is used to select the printer

ACK#: Acknowledge, active-low input, TTL level. When this signal is asserted, it means that the printer and received all previous data and it is ready to receive new data.

BUSY: Busy input, TTL level. This signal reports that the printer is not ready to receive new data.

PE: Paper End, TTL level input. It is used to signal to the CPU that the printer ran out of paper.

SLCT: Select, TTL level input. When this signal is high (asserted), it reports that the printer is on and it has been selected.

Floppy Disk Mode signals:

DENSEL: Drive Density Select, open drain output. It is used to enable low density operations (250Kbps/300Kbps) or high density operations (500Kbps/1000Kbs).

INDEX#: Index signal active-low, TTL level Schmitt Trigger input. It is activated by the disk drive each time that it is sensed the diskette index hole.

TRK0#: Track 0, active-low, TTL level Schmitt Trigger input. This signal is driven low by the Disk Drive when the head is positioned over the outermost track.

WP#: Write Protected, active low TTL level Schmitt Trigger input. It is asserted by the disk drive when it reveals a disk protected from writing.

RDATA#: Read data, TTL level Schmitt Trigger input. This signal is used to carry the data read from the disk drive.

DSKCHG#: Diskette change, TTL level Schmitt Trigger input. This signal is used to report to the CPU that the diskette has been removed (the drive door has been opened).

DRV#: Drive Select, open drain active low output. This signal is used to activate the floppy drive.

MOT#: Motor On, open drain active low output. This signal is used to activate the motor of the selected floppy drive.

HDSEL#: Head Select, open drain output used to determine which disk drive head is active. When the signal is low, then Head 0 is selected. When it is High (open), then Head 1 is selected.

DIR#: Direction, open drain output used to set the direction of the head movement. When the signal is low, the head moves inwards, when it is high it moves outwards.

STEP#: Step output pulse, open drain active low output. This signal is pulsed each time it is necessary to move the head to another track during a seek operation.

WDATA#: Write Data, open drain active low output. This signal is used to transfer a pre-compensation serialised data stream to the selected disk drive.

WGATE#: Write Enable, open drain active low output. This signal enables the write circuitry of the selected disk drive.

3.2.5.10 IDE signals (Connector X4 - CN7)

ETX® specifications foresee the presence of two IDE channels on connector X4 (CN7), and also the possibility of having two additional SATA connectors on the board's side. However, the SOCs used on ETX-A61 only offer support to two S-ATA channels, and not to P-ATA.

For this reason, it is possible to equip the board with up to two SATA to PATA bridges; each of them can make available one PATA interface, at the expenses of one of the external SATA connectors.

> **!** Since the P-ATA interface is derived from a SATA channel, then it will support only one device per channel. Only Master is supported. It is also recommended to configure the IDE device as a Master.

Here following the signals related to PATA interfaces (effective availability of them depends on the module's configuration purchased):

PIDE_D[0..15]/SIDE_D[0..15]: Primary / Secondary IDE 16-bit data bus, +3.3V_S bidirectional signals.

PIDE_A[0..2]/SIDE_A[0..2]: Primary / Secondary IDE address bus, +3.3V_S bidirectional signals.

PIDE_CS1#/SIDE_CS1#: Primary / Secondary IDE Chip Select 1#, +3.3V_S active low output. They are used to select the Command Block registers on the device found connected.

PIDE_CS3#/SIDE_CS3#: Primary / Secondary IDE Chip Select 3#, +3.3V_S active low output. They are used to select the Control Block registers on the device found connected.

PIDE_DRQ/SIDE_DRQ: Primary/Secondary IDE DMA request, +3.3V_S inputs. These signals are used by the IDE devices in order to request a DMA transfer

PIDE_AK#/SIDE_AK#: Primary/Secondary IDE DMA Acknowledge, +3.3V_S active low outputs. These signals are used to confirm that the DMA request has been received and that the DMA transfer has been granted.

PIDE_RDY/SIDE_RDY: Primary/Secondary IDE Ready, +3.3V_S input. These signals are driven by the external IDE devices to report if they are ready to fulfil a data transfer request.

PIDE_IOR#/SIDE_IOR#: Primary/Secondary IDE I/O Read Command, active low +3.3V_S output. These signals are asserted by the bridge each time it tries to access to the disk in Read Mode.

PIDE_IOW#/SIDE_IOW#: Primary/Secondary IDE I/O Write Command, +3.3V_S active low output. These signals are asserted by the bridge each time it tries to access to the disk in Write Mode.

PIDE_INTRQ/SIDE_INTRQ: Primary/Secondary IDE Interrupt request, +3.3V_S inputs

HDRST#: IDE devices reset, active-low +3.3V_S output. This signal is used to reset the Disk Drives connected to IDE interface. Please check also the following chapter

On the carrier board, these signals can be carried out directly to the IDE (P-ATA) connectors.

> **!** If the module purchased is in dual P-ATA configurations, then consider that each IDE (P-ATA) slot should be occupied, i.e. connected to a mass storage device. Indeed, if at least one of the two slots is left empty, then BIOS boot will last around 30 seconds, while the OS may take some minutes to complete the boot phase.
> Moreover, it is not possible to disable the empty channel only. When disabling PATA, both the channels will be disabled

3.2.5.10.1 Double PATA configuration's reset workaround

In the ETX standard there is only one Hard Disk Reset signal, while each SATA-to-IDE bridge has its own reset output signal.

This can cause problems with the BIOS; which could not detect correctly the Disk Drives, and with the OS boot.

There are two possible solutions to this issue:

1. Enable the board reset when boot drives are not detected. To do this, enable the "Reset On No Boot Device Found" item in the "Boot" page of Setup Utility (see par. 4.6)
2. As an alternative (or along with the previous solution), it is possible to enable the Watchdog in the Setup Utility, disabling then it in the OS by using the EAPI libraries.

These solutions can be applied also in TA61 Single PATA configuration modules.

3.2.5.11 Ethernet signals (Connector X4 - CN7)

The Ethernet interface is realised, on ETX-A61 module, using an Intel® I211 Gigabit Ethernet controller, which is interfaced to the SOC through PCI-express lane #0.

Since ETX® specifications doesn't support Gigabit Ethernet interface, only signals related to 10/100Mbps interface are carried out on connector X4 (CN7)

Here following the signals involved in Gigabit Ethernet management

RXD-/RXD+: Ethernet receiving differential pair.

TXD-/TXD+: Ethernet Transmitting differential pair.

ACTLED#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_A.

LILED#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_A.

SPEEDLED#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_A.

These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

LED signals, if not necessary, can be left floating on the carrier board.

3.2.5.12 Power Control and Management signals (Connector X4 - CN7)

According to ETX® specifications, on the connector X4 (CN7) there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWGIN: Power Good Input, active high +3.3V_S input. This signal is used by the carrier board to report to the module that the power supply is good.

PS_ON#: Power On Signal, active low +5V_A output with 100KΩ pull-up resistor. This signal is used to turn on an external ATX power supply unit. For proper working, it is necessary that external +5V_A voltage is supplied to the module through pin 3 of ETX connector X4 (CN7).

PWRBTN#. Power Button Input, active low +3.3V_A input with 10KΩ pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

RSMRST#: Resume Reset, active low +3.3V_A input with 10KΩ pull-up resistor. This signal is needed internally for correct power sequencing of the board. It can be externally driven to command a reset of the power management logic.

SMBALERT#: System Management Bus Alert, active low +3.3V_A input with 10KΩ pull-up resistor. Any device placed on the SM Bus can drive this signal low to signal an event on the bus itself.

BATLOW#: Battery Low, active low +3.3V_A input with 10KΩ pull-up resistor. This signal is driven by external circuitry to report that the system battery is going out of charge, or other power related events.

GPE1#: General Purpose Event #1, active low +3.3V_A input with 10KΩ pull-up resistor. According to ETX® specifications, this signal can be used as a LID#

signal, which is driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

GPE2#: General Purpose Event #2, active low +3.3V_A input with 10KΩ pull-up resistor.

EXTSMI#: System Management Interrupt, active low +3.3V_A input with 10KΩ pull-up resistor.

3.2.5.13 Miscellaneous signals (Connector X4 - CN7)

Here following, a list of ETX® compliant signals that complete the features of ETX-A61 module.

SPEAKER: Speaker output, +3.3V_S voltage signal, managed by SOC's embedded counter.

I2CLK, I2DAT: general purpose I2C Bus clock and data line. The I2C interface is managed by the SOC's embedded Serial IO (SIO).

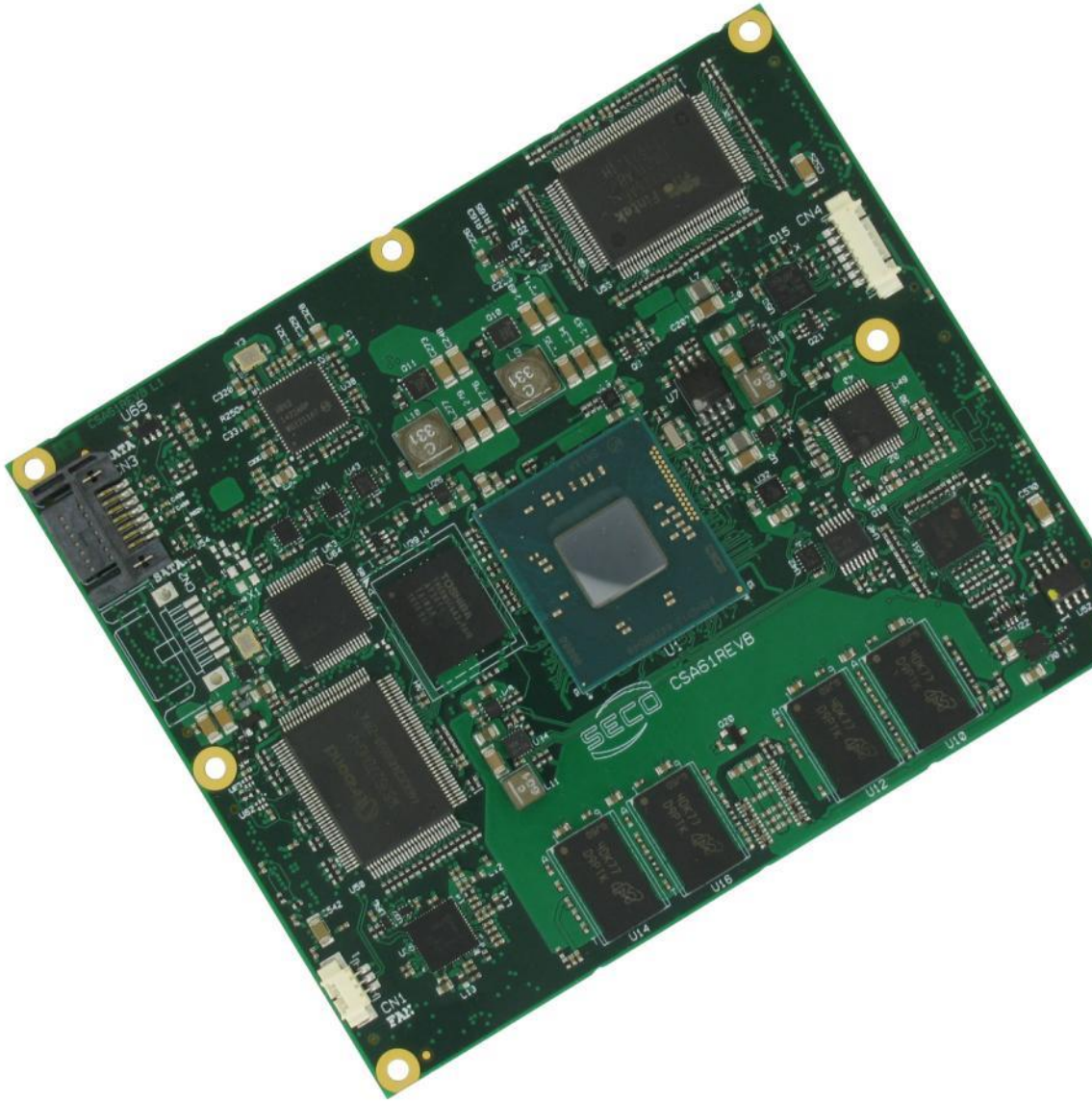
SMBCLK, SMBDATA: SM Bus control clock and control data lines for System Management. Bidirectional signals, electrical level +3.3V_A with 4k7Ω pull-up resistors. It is managed by the SOC's embedded Platform Control Unit (PCU) System Management Bus 2.0 Host Controller

KBINH#: Keyboard Inhibit, +3.3V_S bidirectional signal with 10KΩ pull-up resistor. This signal on ETX modules could be used to disable data input from the keyboard. On ETX-A61, however, it is connected to a General Purpose I/O pin.

SERIRQ: LPC Serialised IRQ request, bidirectional line, +3.3V_S electrical level. This signal can be used by peripherals requiring Interrupt support.

Chapter 4.
BIOS SETUP

- InsydeH2O setup Utility
- Main setup menu
- Advanced menu
- Security menu
- Power menu
- Boot menu
- Exit menu



4.1 InsydeH2O setup Utility

Basic setup of the board can be done using Insyde Software Corp. “InsydeH2O Setup Utility”, that is stored inside an onboard SPI Serial Flash.

It is possible to access to InsydeH2O Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select “SCU” icon.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
<F5> / <F6>	<F5> and <F6> keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows displaying the General Help screen.
<F9>	<F9> key allows loading Setup Defaults for the board. After pressing <F9> BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<F10>	<F10> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows discarding any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow displaying the setup sub- screens.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

4.2.1 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Boot Configuration	See submenu	Configures settings for Boot Phase
PCI Express Configuration	See submenu	PCI Express Configuration Settings
USB Configuration	See submenu	Configures USB Section
Audio Configuration	See submenu	Configures Audio Section
LPSS & SCC Configuration	See submenu	Configures LPSS (Low-Power Sub-System, i.e. DMA, PWM, UART and I2C interfaces) and SCC (Storage Control Cluster) devices
Miscellaneous Configuration	See submenu	Enable / Disable Misc. features
Security configuration (TXE)	See submenu	Trusted Execution Environment Security Configurations
Video Configuration	See submenu	Configures the options for video section
Chipset Configuration	See submenu	Configure Chipset's parameters
SATA Configuration	See submenu	Select the SATA controller and hard disk drive type installed in the system
Console redirection	See submenu	Console redirection settings
ACPI Table / Features Control	See submenu	Configures the parameters for ACPI management
Super I/O Configuration	See submenu	Super I/O Setup Configuration Utility
Virtual Super I/O Configuration	See submenu	Install legacy UARTs on ACPI aware OS
INT/IRQ Configuration	See submenu	INT/IRQ Configuration
LPC to ISA Bridge Configuration	See submenu	LPC to ISA Bridge Configuration

4.3.1 Boot configuration submenu

Menu Item	Options	Description
Numlock	On / Off	Allows to choose whether NumLock Key at system boot must be turned On or Off

4.3.2 PCI Express configuration submenu

Menu Item	Options	Description
PCI Express Root Port 0 (Internal LAN) PCI Express Root Port 1(PCIE-to-PCI Bridge)	See submenu	

4.3.2.1 PCI Express Root Port #x configuration submenus

Menu Item	Options	Description
PCI Express Root Port #x	Disabled / Enabled	Enable or Disable single PCI Express Root Port #x. PCI Express Root Port#0 is internally connected to Intel® Gigabit Ethernet Controller I211. Disabling this port will result in disabling Ethernet interface. PCI Express Root Port#1 is internally connected to the Texas Instruments® XIO2001 PCI-express to PCI bridge. Disabling this port will result in disabling PCI interface.
PCIE Port 1 Speed	Auto / Gen1 / Gen2	This menu item is available only for PCI Express Root Port #1 when it is set to Enabled. Set PCI-e ports link speed/capability. Not available for PCI Express Root Port #0
PCIE Port 1 ASPM	Disabled / L0s / L1 / L0s & L1 / Auto	This menu item is available only for PCI Express Root Port #1 when it is set to Enabled. Manages PCI Express L0s and L1 power states, for OSs able to handle Active State Power Management (ASPM). Not available for PCI Express Root Port #0

4.3.3 USB configuration submenu

Menu Item	Options	Description
USB BIOS Support	Disabled / Enabled / UEFI Only	Enable/Disable the support for USB keyboard / mouse / storage in UEFI and DOS environment. When it is set to UEFI only, then DOS environment will not support such USB devices.
xHCI Mode	Disabled Enabled Auto Smart Auto Best Auto	Mode of operation of xHCI controller Disabled: USB 3.0 functionalities are always disabled, USB 3.0 devices will work in High Speed Mode Enabled: USB 3.0 functionalities are available both in BIOS and in OS (also for booting, provided that the xHCI driver is installed). Auto: USB 3.0 devices will work only when OS has started, provided that hcSwitch and xHCI drivers are installed. In BIOS and during boot USB 3.0 devices will work in High Speed mode Smart Auto: when starting from a Mechanical Off (G3) state, USB 3.0 functionalities are available both in BIOS and in OS (also for booting, provided that the hcSwitch and xHCI driver is installed). When the system boots from a different ACPI state, USB 3.0 devices will be managed by xHCI or EHCI controller depending on the last used configuration. Best Auto: always route to xHCI
xHCI Controller	Disabled / Enabled	Enable/Disable xHCI Controller
USB2 Link Power Management	Disabled / Enabled	Can be changed only when "xHCI Controller" is Enabled Enable/Disable the USB2 Link Power Management, i.e. the management of different Link Power (Lx) States of connected USB devices depending on the workload of the device itself.
xHCI Streams	Disabled / Enabled	Can be changed only when "xHCI Controller" is Enabled Enable/Disable the xHCI Stream Support.
EHCI Controller	Disabled / Enabled	Controls the USB EHCI (USB 2.0) functionalities. One EHCI controller must always be enabled.
USB EHCI debug	Disabled / Enabled	Enable / Disable PCH EHCI debug capability
USB Per-Port Control	Disabled / Enabled	Allows to enable / disable singularly each of USB ports #0 ÷ #3
USB Port #0 / USB Port #1 / USB Port #2 / USB Port #3	Disabled / Enabled	Available only when "USB Per-Port Control" is Enabled Allows to enable / disable the USB port
USB Ignore Settings	See Submenu	Allows excluding BIOS support for single USB Devices/Ports/Hosts.
USB Ignore Request Timeout (sec.)	0÷30	When enabled (i.e., timeout greater than zero), for each USB bootable device it is required the user confirmation. Without any action, when the timeout expires the USB device is ignored. If the timeout is set to zero, it means that this feature is disabled, and the boot sequence works in the standard way. When enabled, the Confirm Dialog Box is displayed only for disks with a valid MBR.
Display USB Device's Name	Disabled / Enabled	Available only when "USB Ignore request Timeout (Sec.)" is Set. Allows enabling / disabling the disabling of USB Device's name in the timeout string.

4.3.3.1 USB Ignore Settings submenu

It is possible to define up to four (4) rules for the USB ports to be ignored from BIOS support, if desired. Each rule will offer the following options:

Menu Item	Options	Description
Host Controller	None / All / Int. xHCI (Usb3.0) / Int. EHCI (Usb2.0)	Select the Host Controller to ignore
Port	None / All / Port 0 / Port 1 / Port 2 / Port 3	Select the USB Port to ignore
USB Class	None / All / Hid / Mass Storage	Select the USB Class of Devices to ignore. HID: Touch Controllers, Mouses Keyboards Mass Storage: USB disks, CD/DVD, Floppy Disks
Vendor ID	0x0001 ÷ 0 x FFFE	Specify the Vendor ID to ignore. 0xFFFF = Ignore All 0xFFFE = Ignore None
Device ID	0x0001 ÷ 0 x FFFE	Specify the Device ID to ignore. 0xFFFF = Ignore All 0xFFFE = Ignore None

! If the BIOS support is excluded for all ports and/or all HID devices, it will be impossible to enter in the Setup Configuration utility using USB keyboards.
Please be careful before changing these settings.

4.3.4 Audio configuration submenu

Menu Item	Options	Description
Audio Controller	Disabled / Enabled	Controls the detection of the Azalia Audio Controller Disabled: the Audio controller will be unconditionally Disabled Enabled: the Audio controller will be unconditionally Enabled
VC1 Enable	Disabled / Enabled	Available only when “Audio Controller” is Enabled Enable or Disable Virtual Channel 1 of Audio Controller
Mic	Disabled / Enabled	Enable or Disable ETX Mic Input
Line Out	Disabled / Enabled	Enable or Disable ETX Line Out output
Line In	Disabled / Enabled	Enable or Disable ETX Line In input

4.3.5 LPSS & SCC configuration submenu

Menu Item	Options	Description
LPSS & SCC Devices Mode	ACPI Mode PCI Mode	Allows setting the Working mode of LPSS (Low-Power Sub-System) and SCC (Storage Control Cluster) devices. Use PCI mode for Windows® 7, use ACPI mode for Android and Windows® 8
LPSS & SCC Auto Switch	Disabled / Enabled	Only available when "LPSS & SCC Devices Mode" is set to ACPI Mode. Auto switches LPSS & SCC devices from ACPI mode to PCI mode when the O.S. does not support the ACPI mode
Hide Unsupported LPSS Devices	Disabled / Enabled	Only available when "LPSS & SCC Devices Mode" is set to ACPI Mode. Hide the unsupported LPSS devices
SCC eMMC Boot Controller	Disable / Enable	Disable or enable the eMMC Boot controller
eMMC Secure Erase	Disable / Enable	Can be changed only when "SCC eMMC Boot Controller" is Enabled. Disable or enable the eMMC Secure Erase. When enabled, all the data on the eMMC will be erased
DDR50 Capability Support	Disable / Enable	Can be changed only when "SCC eMMC Boot Controller" is Enabled. Enable or disable the DDR50 support for eMMC 4.5
HS200 Capability Support	Disable / Enable	Can be changed only when "SCC eMMC Boot Controller" is Enabled. Enable or disable the HS200 support for eMMC 4.5
Re Tune Timer Value	0 / 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8 / 9 / 10 / 11 / 12 / 13 / 14 / 15	Can be changed only when "SCC eMMC Boot Controller" is Enabled and "DDR 50 Capability Support" is Disabled. Sets the retune timer value
SCC SD Card Support	Disabled / Enabled	Enable/ Disable SD Card Support
LPSS DMA #2 Support	Disabled / Enabled	Allows to enable second DMA Channel, which onboard is used to support the I2C Channel
LPSS I2C #1 Support	Disabled / Enabled	Enable / Disable the I2C Bus available on ETX connector X4 (CN7)
I2C Device Configuration	See Submenu	Allows the installation of I2C Devices on ACPI aware OS

4.3.5.1 I2C Device Configuration submenu

Menu Item	Options	Description
Device Type	Disabled / 7bits / 10 bits	Select the I2C device address format
Address	0x0 ÷ 0xF (7 bit mode) 0x0 ÷ 0xFF (10 bit mode)	Can be changed only when "Device Type" is not Disabled. Select I2C device address
Speed	Standard mode (100 Kb/s) Fast mode (400 Kb/s)	Can be changed only when "Device Type" is not Disabled. Configure I2C Bus Speed

4.3.6 Miscellaneous Configuration submenu

Menu Item	Options	Description
HPET - HPET Support	Enabled / Disabled	High Precision Event Timer is supported in Windows Vista or above. HPET controller should not been seen in Windows XP, no matter if enabled/disabled in SCU. If this feature is enabled, the HPET table will be added into ACPI Tables.
Clock Spread Spectrum	Enabled / Disabled	Allows enabling Clock Chip's Spread Spectrum feature
BIOS Lock	Enabled / Disabled	Enable or disable BIOS SPI region write protect
PCI MMIO Size	0.75GB 1.5GB 2GB	Setup PCI Memory Mapped IO Space, 0.75GB, 1.5GB or 2GB. Note: to avoid system hangs caused by insufficient memory allocation, reducing this value may lead to the reduction of the IGD aperture size selected in Advanced Menu → Video Configuration submenu.
Memory optimization for 32-bit Windows OS	Enabled / Disabled	When using Windows 32-bit versions, enabling this feature will allow a better memory resource allocation.
PCI Express Dynamic Clock Gating	Enabled / Disabled	Enable or Disable PCI Express Dynamic Clock Gating
Force Legacy free	Enabled / Disabled	Forces Legacy free mode when enabled (it forces the disable of KBC)
Serial IRQ	Enabled / Disabled	Enable or Disable the Serial IRQ
Serial IRQ Mode	Quiet Mode / Continuous Mode	Select the Serial IRQ Mode. In "Quiet Mode", the host continually generates SERIRQ frames to check for device interrupts. In "Continuous Mode", the Host waits for a Serial IRQ slave to generate a request by asserting the SERIRQ signal
Intel I210/I211 Led1	Default Activity	Intel® I210/I211 Gb Ethernet controller LED1 behaviour. Default setting makes LED1 active on link. Setting to "Activity" makes LED1 active only when network traffic is present
Memory Scrambler	Enabled / Disabled	Enable or disable the memory scrambler feature. Please be aware that WEC7 requires the memory scrambler enabled, while Linux requires that it is disabled.

4.3.7 Security configuration submenu

Menu Item	Options	Description
TXE	Disabled / Enabled	Enable or Disable the Intel® Trusted Execution Engine (TXE, available only on Celeron CPUs)
TXE HMRFP0	Disabled / Enabled	Enable this option to remove temporarily the flash protection, in order to program the Intel® TXE region
TXE Firmware update	Disabled / Enabled	Enable this option to require a re-flashing of TXE Firmware Image
TXE EOP Message	Disabled / Enabled	Send EOP (End of POST) Message before entering OS
TXE Unconfiguration Perform	Yes / No	Only selectable on CPUs with the TXE feature. Allows to revert TXE settings to the factory defaults

4.3.8 Video configuration submenu

Menu Item	Options	Description
VBIOS Selection	Default / Intel ISG Optimized	Allows loading an optimized VBIOS to solve an issue of Linux Kernels (video configuration wrong detection).
CRT	Disabled / Enabled	Enables or disables the CRT Video Output
DDI1	Disabled / Enabled	Enables or disables the DDI1 Video Output, which manages the eDP to LVDS bridge. Disabling this video output will result in disabling the LVDS output
Primary Display	CRT / DDI1 / None	Select the Primary Display for the use in WEC7 operating System
Secondary Display	CRT / DDI1 / None	Select the Secondary Display for the use in WEC7 operating System
Display Mode	Single / Extended / Extended Vertical / Clone	Select the Display Mode for the use in WEC7 operating System
LFP	Custom / 640x480 / 800x480 / 800x600 / 1024x600 / 1024x768 / 1280x720 / 1280x800 / 1280x1024 / 1366x768 / 1400x900 / 1600x900 / 1680x1050 / 1920x1080	Select a software resolution (EDID settings) to be used for the internal flat panel.
LFP Custom parameters	See submenu	Only available when “LFP” is set to Custom. Select Detailed Timing Descriptor Parameters
LFP Color Mode	VESA 24bpp / JEIDA 24bpp / 18 bpp	Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.

LFP Interface	Single Channel Dual Channel	Allows configuration of LVDS interface in Single or Dual channel mode
LVDS Advanced Options	See Submenu	LVDS Advanced Options Configurations
LFP Default Brightness (%)	0 ÷ 100	LFP Default brightness percentage. Valid values are in the range 0-100, where 0 means backlight OFF. This setup configuration, during the BIOS boot, is valid only with a single LFP connected (no multi-monitor).
LFP Max ACPI Brightness (%)	0 ÷ 100	Maximum ACPI brightness percentage allowed with an ACPI aware OS
Integrated Graphics Device	Disabled / Enabled	Enabled: enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disabled: always disable IGD
Primary Display	Auto / IGD / PCIe	Select which of IGD or external PCI Graphic Controller should be the Primary display (please notice that the external PCI bus is managed by the Bay Trail's PCIe interface, hence the meaning of the menu options)
RC6(Render Standby)	Disabled / Enabled	Permits to enable the render standby features, which allows the onboard graphics entering in standby mode to decrease power consumption
PAVC	Disabled / LITE Mode / SERPENT Mode	Allows enabling the hardware acceleration of decoding of Protected Audio Video streams. When LITE is Control, choosing is LITE encryption or SERPENT encryption has to be used.
Power Management Lock	Disabled / Enabled	Enable / Disable Power Management Lock
DOP CG	Disabled / Enabled	Enable / Disable DOP Clock Gating
GTT Size	1MB / 2MB	Select the GTT (Graphics Translation Table) Size
Aperture Size	128MB / 256MB / 512MB	Use this item to set the total size of Memory that must be left to the GFX Engine
IGD - DVMT Pre-Allocated	64M / 96M / 128M / 160M / 192M / 224M / 256M / 288M / 320M / 352M / 384M / 416M / 448M / 480M / 512M	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphic Device
IGD - DVMT Total Gfx Mem	128M / 256M / MAX	Select the size of DVMT (Dynamic Video Memory) 5.0 that the Internal Graphics Device will use
IGD Turbo	Auto / Enabled / Disabled	Enable or Disable IGD Turbo mode
IGD Thermal	Disabled / Enabled	Enabled or disable Thermal Control of IGD
Spread Spectrum clock	Disabled / Enabled	Enable or disable LVDS Spread Spectrum Clock
Backlight Control	Auto PWM- Inverted PWM-Normal	Backlight control setting

4.3.8.1 LFP Custom submenu

Using this submenu, it is possible to set all the following parameters to meet the LVDS display requirements.

Menu Item	Options	Description
Pixel Clock / 10000	Any value in range [2500..22400]	Working Frequency in 10kHz units, e.g 6350 → 63.5MHz. Allowed range from 2500 (25MHz) to 22400 (224MHz)
Horizontal Active	Any value in range [1..4095]	Horizontal Addressable Video in pixels, a.k.a. Horizontal resolution (e.g. 1024 on a 1024x768 LFP)
Horizontal Blank	Any value in range [1..4095]	Horizontal Blanking in pixels, equals to Horizontal Total (Horizontal Active + Horizontal Front Porch + Horizontal Black Porch)
Vertical Active	Any value in range [1..4095]	Vertical Addressable Video in pixels, a.k.a. Vertical resolution (e.g. 768 on a 1024x768 LFP)
Vertical Blank	Any value in range [1..4095]	Vertical Blanking in pixels, equals to Vertical Total (Vertical Active + Vertical Front Porch + Vertical Black Porch)
Horizontal Offset	Any value in range [1..1023]	Horizontal Front Porch in pixels
Horizontal Pulse	Any value in range [1..1023]	Horizontal Sync Pulse Width in pixels
Vertical Offset	Any value in range [1..63]	Vertical Front Porch in pixels
Vertical Pulse	Any value in range [1..63]	Vertical Sync Pulse Width in pixels
Horizontal Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)
Vertical Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)

4.3.8.2 LVDS Advanced options submenu

Using this submenu, it is possible to set all the following parameters to meet the LVDS display requirements.

Menu Item	Options	Description
LVDS Spreading Depth	No Spreading / 0.5% / 1.0% / 1.5% / 2.0% / 2.5%	Sets percentage of bandwidth of LVDS clock frequency for spreading spectrum
LVDS Output Swing	150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV / 450 mV	Sets the LVDS differential output swing
T3 Timing	0 ÷ 255	Minimum T3 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 10 (500ms)
T4 Timing	0 ÷ 255	Minimum T4 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 2 (100ms)
T12 Timing	0 ÷ 255	Minimum T12 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 20 (1s)
T2 Delay	Enabled / Disabled	When Enabled, T2 is delayed by 20ms ± 50%
T5 Delay	Enabled / Disabled	When Enabled, T5 is delayed by 20ms ± 50%
P/N Pairs Swapping	Enabled / Disabled	Enable or disable LVDS Differential pairs swapping (Positive ⇔ Negative)
Pairs Order Swapping	Enabled / Disabled	Enable or disable channel differential pairs order swapping (A ⇔ D, B ⇔ CLK, C ⇔ C)
LVDS BUS Swapping	Enabled / Disabled	Enable or disable Bus swapping (Odd ⇔ Even)

4.3.9 Chipset configuration submenu

Menu Item	Options	Description
PCI 64-bit Decode	Enabled / Disabled	Allow the system to support 64-bit BAR (Base Address Register) for PCI devices.
CRID	Enabled / Disabled	Enable or disable the Compatibility Revision ID (CRID) feature

4.3.10 SATA configuration submenu

Menu Item	Options	Description
SATA Controller	Enabled / Disabled	Disabled: Disables SATA Controller. All following menu items will be grayed out (i.e., they cannot be changed). Enabled: Enables SATA Controller
SATA Port 0 SATA Port 1	Enabled / Disabled	Individually enables or disables SATA Port 0 / SATA Port 1
Chipset SATA Mode	IDE AHCI	Set SATA Configuration type With AHCI, is not possible to install/boot UEFI O.S., only Legacy OS can be installed (a simpler driver is required). Setting to IDE, the controller is managed as a PCI device, so addresses reallocation and INT line sharing is possible.
SATA Speed	Gen 1 / Gen2	Select SATA Speed
SATA Port 0 Hot Plug Capability SATA Port 1 Hot Plug Capability	Enabled / Disabled	These items will be available only when “Chipset SATA Mode” is set to AHCI. If enabled, SATA port will be reported as Hot Plug Capable
IDE Max Transfer Mode	Auto Ultra ATA/100 Ultra ATA/66 Ultra ATA/33 PIO Mode	This item will be available only when “Chipset SATA Mode” is set to IDE. Sets the IDE Interfaces’ maximum Transfer Rate
IDE Mode	Native IDE Legacy IDE	This item will be available only when “Chipset SATA Mode” is set to IDE. Sets the IDE Working Mode
Serial ATA Port 0 / 1		Shows information related to eventual devices connected to SATA ports 0 or 1

!

It is strongly recommended to disable SATA Port #0 in case there isn’t any device connected at it (both in case the module is configured with SATA connector or with Primary IDE interface).

This will result in a much faster boot of the O.S.

4.3.11 Console Redirection submenu

Menu Item	Options	Description
Console Serial Redirect	Enabled / Disabled	Enables or Disabled the ridirection of video output on serial ports.
Terminal Type	VT-100 / VT_100+ / VT_UTF8 / PC_ANSI	This item will be available only when “Console Serial Redirect” is enabled. Sets the terminal type for Console Redirection
Baud rate	115200 / 57600 / 38400 / 19200 / 9600 / 4800 / 2400 / 1200	This item will be available only when “Console Serial Redirect” is enabled. Sets the baud rate for Console Redirection
Data Bits	7 bits / 8 bits	This item will be available only when “Console Serial Redirect” is enabled. Sets the number of data bits for Console Redirection
Parity	None / Even / Odd	This item will be available only when “Console Serial Redirect” is enabled. Sets the type of parity bit for Console Redirection
Stop Bits	1 bit / 2 bits	This item will be available only when “Console Serial Redirect” is enabled. Sets the stop bits for Console Redirection
Flow Control	None RTS/CTS XON/XOFF	This item will be available only when “Console Serial Redirect” is enabled. Sets the Flow Control type for Console Redirection
Information Wait Time	0 Second / 2 Seconds / 5 Seconds / 10 Seconds / 30 Seconds	This item will be available only when “Console Serial Redirect” is enabled. Sets the information Wait time
C.R. After Post	Yes / No	This item will be available only when “Console Serial Redirect” is enabled. When it is set to “Yes”, the Console Redirect will be active also after POST phase
AutoRefresh	Enabled / Disabled	This item will be available only when “Console Serial Redirect” is enabled. When this feature is set to Enabled, then the screen will be auto refreshed after detecting that a remote terminal has been connected.
FailSafeBaudRate	Enabled / Disabled	This item will be available only when “Console Serial Redirect” is enabled. When enabled, there will be auto detection of remote terminal baud rate. Such a baud rate will be used for the Console Redirection
ACPI SPCR Table	Enabled / Disabled	Serial Port Console Redirection (SPCR) table: when this feature is enabled, the SPCR tabel will be added into the ACPI tables.
Serial Port 0 - 03F8 IRQ4 Serial Port 1 - 02F8 IRQ3	Info in the submenu	These two items allow the settings of individual port COM A or COM B, which can share the global settings above described, or could have different settings each one

4.3.12 ACPI Table/features submenu

Menu Item	Options	Description
FACP - RTC S4 wakeup	Enabled / Disabled	Enable or disable FACP (Fixed ACPI Description Table) support for S4 wakeup from RTC
DSDT - ACPI S3	Enabled / Disabled	Enable or disable DSDT (Differentiated System Description Table) support for ACPI S3 State
DSDT - ACPI S4	Enabled / Disabled	Enable or disable DSDT (Differentiated System Description Table) support for ACPI S4 State
BGRT - ACPI BGRT	Enabled / Disabled	Enable or disable the support for ACPI Boot Graphics Resource Table

4.3.13 Super I/O configuration submenu

Menu Item	Options	Description
Winbond/Nuvoton W83627xxx (0x2E)		By selecting this voice, it will be possible to check and set all the following items. Please notice that is the carrier board has an additional SuperI/O, it will appear here, and it will offer a similar list of items to be configured
Keyboard Controller	Enabled / Disabled	Enable or Disable the Keyboard Controller It is strongly recommended to disable the Keyboard Controller in case that the PS/2 Keyboard interface is not used. This will result in a much faster boot of the O.S.
Serial Port 1	Enabled / Disabled	Enable or Disable the Serial Port 1
Address	0x3F8 / 02xF8 / 0x3E8 / 0x2E8 / 0x3E0 / 0x2E0 / 0x338 / 0x238 / 0x220 / 0x228	Sets the I/O Base Address for Serial Port #1
IRQ	3 / 4 / 5 / 6 / 7 /10 / 11 / 14 / 15	Sets the IRQ associated to Serial Port #1
Serial Port 2	Enabled / Disabled	Enable or Disable the Serial Port 2
Address	0x3F8 / 02xF8/ 0x3E8 / 0x2E8 / 0x3E0 / 0x2E0 / 0x338 / 0x238 / 0x220 / 0x228	Sets the I/O Base Address for Serial Port #2
IRQ	3 / 4 / 5 / 6 / 7 /10 / 11 / 14 / 15	Sets the IRQ associated to Serial Port #2
Floppy Disk Controller	Enabled / Disabled	Enable or Disable the Floppy Disk Controller

Parallel Port Mode	External FDC Parallel Port	Allows to select how the parallel port signals are used, i.e. for the connection of an external Floppy Disk Drive or as a Parallel Port
LPT Port	Enabled / Disabled	Only available when “Parallel Port Mode” is set to “Parallel Port”. Allows enabling or disabling the Parallel Port.
LPT Mode	SPP EPP 1.9 and SPP ECP ECP/EPP 1.9 Printer Mode EPP 1.7 and SPP ECP/EPP 1.7	Only available when “Parallel Port Mode” is set to “Parallel Port” and “LPT Port” is Enabled. Allows selecting the LPT Working mode
LPT IRQ	Disabled / 5 / 7	Only available when “Parallel Port Mode” is set to “Parallel Port” and “LPT Port” is Enabled. Allows selecting the IRQ associated to the LPT Port
Hardware Monitor	Enabled / Disabled	Enable or Disable the Hardware Monitor
Watchdog	Disabled / 1 Minute 2 Minutes / 3 Minutes	Disable the Watchdog functionality or sets the watchdog expiry time

4.3.14 Virtual SuperI/O configuration submenu

Menu Item	Options	Description
Address	Disabled / 0x3F8 / 0x2F8 / 0x3E8 / 0x2E8 / 0x3E0 / 0x2E0 / 0x338 / 0x238 / 0x220 / 0x228	Select the Base address for each virtual Serial Port, or disable it
IRQ	Disabled / 3 / 4 / 5 / 6 / 7 / 10 / 11 / 14 / 15	Select the IRQ line to assign to each Serial Port, if enabled.

4.3.15 INT/IRQ configuration submenu

Menu Item	Options	Description
INT A Irq / INT B Irq / INT C Irq / INT D Irq / INT E Irq / INT F Irq / INT G Irq / INT H Irq	3 / 4 / 5 / 6 / 7 /10 / 11 / 14 / 15	Selects individually the IRQ to assign to PCI INT line A / B / C / D / E / F / G / H

4.3.16 LPC to ISA Bridge Configuration submenu

Menu Item	Options	Description
LPC to ISA Clock Divider	3 / 4	Allows selecting the divider of LPC Clock that must be used to generate ISA clock. The Atom™ E38xx SOCS has a 33.3MHz LPC clock, and the Celeron® SOCS have a 25MHz LPC clock. Therefore, by dividing the LPC clock by 3, ISA clock will be 8.33MHz with Celeron® SOCs and 11.1MHz with Atom™ E38xx SOCs. By dividing the LPC clock by 4, ISA clock will be 6.25MHz with Celeron® SOCs and 8.33MHz with Atom™ E38xx SOCs.

4.4 Security menu

Menu Item	Options	Description
Set Supervisor Password		Install or Change the password for supervisor. Length of password must be greater than one character.
Power on Password	Enabled / Disabled	Available only when Supervisor Password has been set. Enabled: System will ask to input a password during P.O.S.T. phase. Disabled: system will ask to input a password only for entering Setup utility
User Access Level	Full View Only	View Only: Access to BIOS Setup allowed but the fields cannot be changed. Full: Any Field can be changed except the Supervisor Password
Set User Password		Install or Change the password for the users. Length of password must be greater than one character.
USB Disks Signature Option	See Submenu	Allow to enable or disable USB boot from signed USB disks only

4.4.1 USB Disk Signature Option submenu

Menu Item	Options	Description
USB Disks Signature Check	Enabled / Disabled	Enable the USB disk signature check. When enabled, if the USB disk used is not signed it will be removed from the boot devices list.
One Time Signature Check Disable	Enabled / Disabled	One time disable of USB disk signature check. When enabled, then for the subsequent boot only the USB disk signature will be automatically disabled.
Signature Byte 0	0 ÷ 255	Set the value for byte 0 of USB disks signature. The disk's signature check is always on 4 bytes.
Signature Byte 1	0 ÷ 255	Set the value for byte 1 of USB disks signature. The disk's signature check is always on 4 bytes.
Signature Byte 2	0 ÷ 255	Set the value for byte 2 of USB disks signature. The disk's signature check is always on 4 bytes.
Signature Byte 3	0 ÷ 255	Set the value for byte 3 of USB disks signature. The disk's signature check is always on 4 bytes.
USB Password	State Unknown / Installed / Not Installed	This item shows the state of USB Disk Password for Boot
Set USB Disks Password		When a USB Disk password is set, the system will first check if the USB disk is signed. If it is not signed, then the system will ask for a password, in order to continue booting from the USB disk.

4.5 Power menu

Menu Item	Options	Description
Advanced CPU Control	See submenu	These items control various CPU parameters
EC Watchdog configuration	See submenu	Embedded Controller Watchdog Configuration Settings
Thermal Zone configuration	See submenu	Thermal Zone Configuration: Active and Passive Cooling Settings.
Wake on PME	Enabled / Disabled	Determines whether the system must wake up or not when the system power is off and occurs a PCI Power Management Enable wake-up event (e.g. to enable Wake on LAN feature).
Auto Wake on S5	Disabled By Every Day By Day of Month	Auto Wake from Soft Off State. It can be set to wake every day at the same hour, or only a precise Day of Month
Wake from S5 time	hh:mm:ss	Only available when Auto Wake on S5 is not set to disabled. Allows selecting the exact hour, minute and seconds for the automatic wake of the board
Day of Month	0 ÷ 31	Only available when Auto Wake on S5 is set to By Day of Month. Allows selecting the day of month when the automatic wake must occur
LID_BTN# Configuration	Force Open Force Closed Normal Polarity Inverted Polarity	Configure LID_BTN# Signal as always open or closed (i.e., Force Open / Force Closed), no matter the pin level, or configures the signal polarity: “Normal Polarity” means the signal goes High when open, “Inverted Polarity” means the signal goes Low when open
LID_BTN# Wake Configuration	No Wake Only From S3 Wake From S3/S4/S5	This item can be changed only when “LID_BTN# Configuration” is not set to Force Open or Force Closed. Configure LID_BTN# Wake capability. According to the pin configuration, when the LID is open it can cause a system wake from a sleep state
Power Fail Resume Type	Always ON Always OFF Last State	Determine the System Behavior after a power failure event. In case the option is “Always ON”, the board will start every time the power supply is present. When the option is “Always OFF”, the board will not start automatically when the power supply returns. Finally, if this option is set to “Last State”, the board will remember the state it had when the power supply went down: so, if the board was on, it will start again when the power returns, and will remain off if the board was in this state when the power went down.
ACPI Power off management		When enabled, the board will automatically switch itself to S5 state after OS shutdown. When disabled, a manual Power off is required

4.5.1 Advanced CPU control submenu

Menu Item	Options	Description
Use XD Capability	Enabled / Disabled	Enable or disable processor XD (Execute Disable) capability, it allows to enable or disable the hardware feature needed for data execution prevention
Limit CPUID Max Value	Enabled / Disabled	Set this option to enabled for use with older O.S. that are not able to manage the CPUID value higher than 03h, which was typical for Intel® Pentium 4 with Hyper Threading Technology Leave disabled for newer O.S. able to manage actual CPUID value.
Bi-Directional PROCHOT#	Enabled / Disabled	PROCHOT# is the signal used to start thermal throttling. This signal can be driven by any processor cores' to signal that the processor will begin thermal throttling. If bi-directional signaling is enabled, then external components can also drive PROCHOT# signal in order to start throttling.
VTX-2	Enabled / Disabled	Enable or Disable Intel® Virtualization Technology, allowing hardware-assisted virtual machine management.
TM1 and TM2	Enabled / Disabled	Enable or Disable TM1 and TM2 Thermal management modes.
AESNI Feature	Enabled / Disabled	Enable or Disable AESNI (Advanced Encryption Standard New Instructions) set of instructions, which are used to improve the speed of applications performing encryption and decryption using the Advanced Encryption Standard (AES).
Active Processor Cores	1 / 2 / 3 / ALL	Number of cores to enable in each processor package. 1 means that multicore processing is disabled.
P-States (IST)	Enabled / Disabled	Enable or disable processor management of performance states (P-states)
Boot Performance Mode	Max Performance Low Power	Only available when P-states are enabled Allows to select which performance state must be set by BIOS before starting OS loading.
Turbo Mode	Auto / Enabled / Disabled	Only available when P-states are enabled Enable processor Turbo Mode
Force CPU Speed	Disabled *List of speeds supported by the SOC used*	Only available when P-states are enabled Force CPU speed After boot. When this feature is enabled, P-State APCI Table will be disabled. The list of the speeds shown depends on the SOC mounted on the module
C-States	Enabled / Disabled	Enable processor idle power saving states (C-States).
Max C-States	C1 / C6 / C7	Allows selection of the maximum C-State that must be supported by the OS.

4.5.2 EC Watchdog Configuration submenu

Menu Item	Options	Description
Watchdog	Enabled / Disabled	Enable or Disable the Watchdog
Watchdog Action	System reset Power Button 1s Power Button 4s (shutdown)	This submenu is available only when “Watchdog” is set to Enabled. Specifies the action that must be performed when Watchdog timeout occurs. With System Reset, the module will reset itself With “Power Button 1s”, the system will simulate the pressure for 1 sec. of Power button, which will lead the O.S. to close all his tasks then shutdown. With “Power Button 1s”, the system will simulate the pressure for 1 sec. of Power button, which will lead to the immediate shutdown of the module
Delay to start (sec.)	0 ÷ 600	This item can be changed only when “Watchdog” is enabled. Seconds of delay before the watchdog timer starts counting
Timeout (sec.)	20 ÷ 600	This item can be changed only when “Watchdog” is enabled. Watchdog Timeout.

4.5.3 Thermal Zone configuration submenu

Menu Item	Options	Description
Critical temperature (°C)	95 / 100 / 105 / 110 / 115	Use this item to set the maximum temperature that the CPU can reach. Above this temperature value, the system will perform a critical shutdown
Passive Cooling temperature (°C)	70 / 75 / 80 / 85 / 90	Use this item to set the temperature threshold for the CPU. Above this threshold, an ACPI aware OS will start to lower the CPU frequency.
AC0 Temperature (°C)	50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100 / 105 / 110 / 115	Select the highest temperature above which the onboard fan must work always at Full Speed
AC1 Temperature (°C)	25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100 / 105 / 110 / 115	Select the lowest temperature under which the onboard fan must be OFF.
FAN Duty Cycle (%) Above AC1	50 / 75 / 100	Use this item to set the Duty Cycle for the fan when the CPU temperature is between AC1 and AC0 threshold. Above AC0, the man will run at full speed.

4.6 Boot menu

Menu Item	Options	Description
Boot type	Dual boot Type Legacy Boot Type UEFI Boot Type	Allows to select if the OS must be booted using Legacy Boot Mode, UEFI Boot mode or indifferently using both modalities (depending on the OS)
Quick Boot	Enabled / Disabled	Skip certain tests while booting. This will decrease the time needed to boot the system.
Quiet Boot	Enabled / Disabled	Disables or enables booting in Text Mode.
Display ESC Key Strings	Enabled / Disabled	Display or Hide the "ESC key" strings during the BIOS boot. Disabling this configuration, no information on how to enter Setup Configuration Utility will be displayed.
Display Boot Logo	Enabled / Disabled	Enable or display the visualization of a logo during Boot phase
Logo persistence Time (s)	0 ÷ 10	This submenu is available only when "Display Boot Logo" is set to Enabled. Forced wait time in seconds during the boot logo visualization. 0 means boot as fast as possible. Even with 0 wait time. UEFI OSes supporting BGRT table will display the logo while booting.
Network Stack	Enabled / Disabled	This submenu is available only when "Boot Type" is set to "UEFI Boot type" or "Dual Boot type". When enabled, this option will make available the following Network Stack services: Windows 8 BitLocker Unlock UEFI IPv4/IPv6 PXE Legacy PXE OpROM
PXE Boot Capability	Disabled UEFI: IPv4 Legacy	This submenu is available only when "Network Stack" is Enabled Specifies the PXE (Preboot Execution Environment) Boot possibilities. When Disabled, Network Stack is supported For UEFI, it is possible to support IPv4, IPv6 or both of them In Legacy mode, only Legacy PXE OpROM is supported
PXE Boot to LAN	Enabled / Disabled	This submenu is available only when "Boot Type" is set to "Legacy Boot type". Disables or enables the possibility for the PXE to perform the boot from LAN.
Power Up in Standby Support	Enabled / Disabled	Disable or enable Power Up in Standby Support. The PUIS feature set allows devices to be powered-up in the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.
Add Boot options	First / Last / Auto	Specifies the position in Boot Order for Shell, Network and Removable Disks

ACPI selection	Acpi1.0B / Acpi3.0 / Acpi4.0 / Acpi5.0	Using this menu item it is possible to select to which specifications release the ACPI tables must be compliant.
CD/DVD Rom Boot	Enabled / Disabled	Disables or enables booting from CD/DVD Rom
Floppy Disk Boot	Enabled / Disabled	Disables or enables booting from FLppy Disk
USB Boot	Enabled / Disabled	Disables or enables booting from USB boot devices.
EFI/Legacy Device Order	EFI device first Legacy device first Smart Mode	Determine if boot must happen first through EFI devices or through legacy devices. When enabled, it will happen first from EFI devices. When disabled, it will happen first from Legacy devices.
Windows® 8 Fast Boot	Enabled / Disabled	This submenu is available only when “Boot Type” is set to UEFI Boot Type. If enabled, the system firmware does not initialize keyboard and check for firmware menu key.
USB Hot Key Support	Enabled / Disabled	Available only when “Boot Type” is set to UEFI Boot Type and “Windows® 8 Fast Boot” is Enabled. Enable or disable the support for USB HotKeys while booting. This will decrease the time needed to boot the system
Timeout	0 ÷ 60	The number of seconds that the firmware will wait before booting the original default boot selection.
Reset On No Boot Device Found	Enabled / Disabled	When this option is enabled, the system will reset itself each time that doesn’t find any valid boot device, instead of waiting indefinitely that a Boot device is plugged.
Touch Controller To Enter SCU	Enabled / Disabled	When this option is enabled, it will be possible to use a Touch screen to enter the Setup Configuration Utility, avoiding using additional external keyboard. The Touch detection will be used as hotkey
Legacy Device Fixed Order	Enabled / Disabled	Disable or enable fixed boot order for physical devices. Takes effect at the next boot of the board
Fixed Legacy Boot Order Settings	See Submenu	This submenu is available only when “Legacy Device Fixed Order” is enabled. Allows fixing the boot order by physical devices.
EFI	See Submenu	This submenu is available only when “Boot Type” is not set to “Legacy Boot type”. The submenu will show a list of EFI boot devices. Use F5 and F6 key to change order for boot priority.
Legacy	See Submenu	This submenu is available only when “Boot Type” is not set to “UEFI Boot type”. Allows setting of Legacy Boot Order

4.6.1 Fixed Legacy Boot Order Settings Submenu

Menu Item	Options	Description
First / Second / Third / Fourth / Fifth / Sixth / Seventh	LAN / EHCI / xHCI / SATA0 / SATA1 / eMMC / SD / NONE	Allows selecting the boot order of the possible boot devices. If it is necessary to force the boot from a specific device only, please set is as a first boot device, and set to NONE all other devices.

4.6.2 Legacy submenu

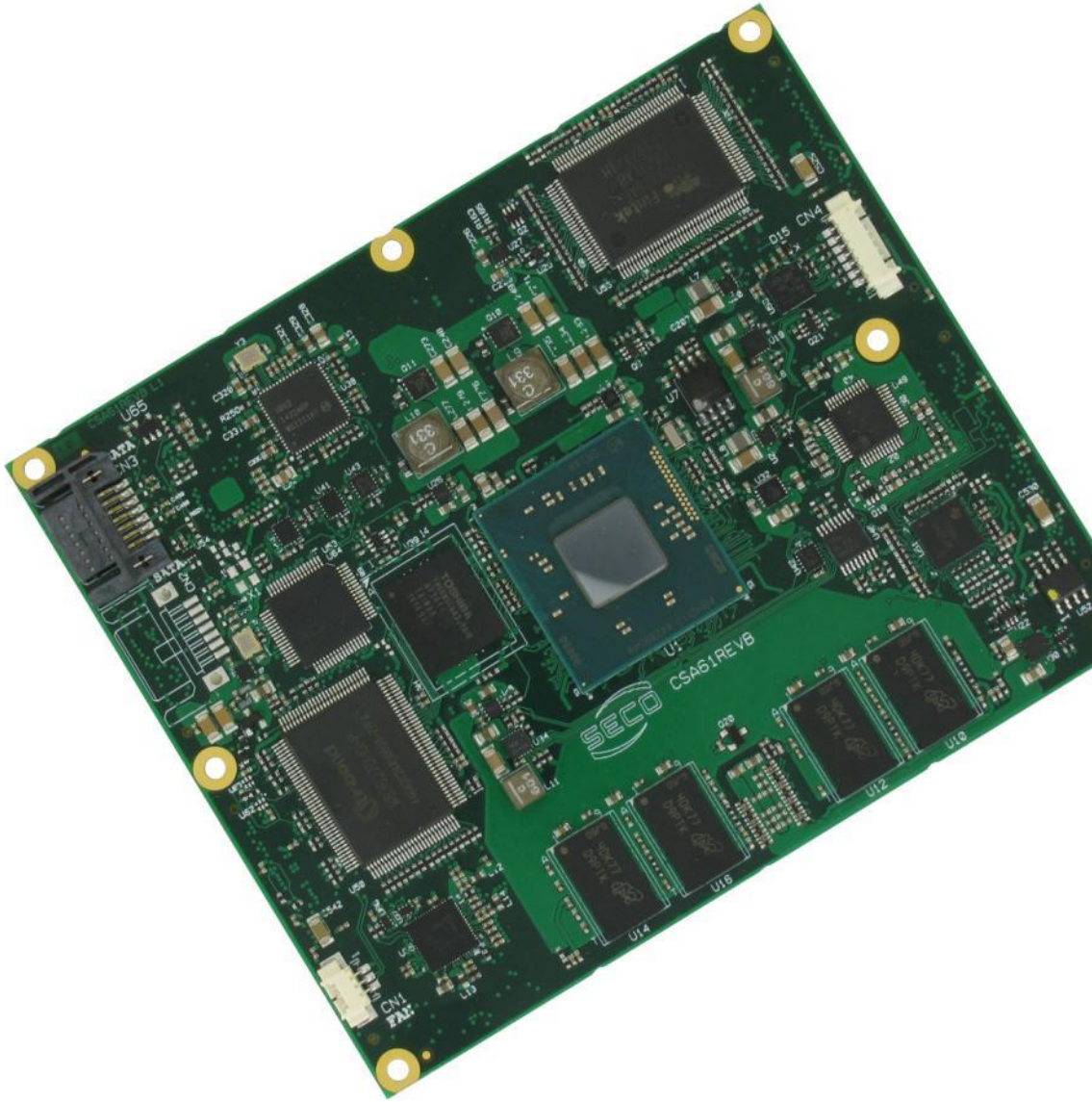
Menu Item	Options	Description
Boot Menu	Normal / Advance	When set to Normal, this submenu will allow configuring all possible options for Legacy boot. When set to Advance, it will be possible to configure Boot Order only for bootable devices found in the system
Boot Type Order	Floppy Drive / Hard Disk Drive CD/DVD-ROM Drive / USB / Other	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will allows selecting the boot from different devices. Use the + and - Keys to change the boot order priority
Hard Disk Drive	*List of HD Drives found connected*	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will show different Disk drives found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority
USB	*List of USB Disks found connected*	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will show different USB disks found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority

4.7 Exit menu

Menu Item	Options	Description
Exit Saving Changes		Exit system setup after saving the changes. F10 key can be used for this operation.
Save Change Without Exit		Save all changes made, but doesn't exit from setup utility.
Exit Discarding Changes		Exit system setup without saving any changes. ESC key can be used for this operation.
Load Optimal Defaults		Load Optimal Default values for all the setup items. F9 key can be used for this operation.
Load Custom Defaults		Load Custom Default values for all the setup items.
Save Custom Defaults		Save Custom Default values for all the setup items.

Chapter 5.
Appendices

- Thermal Design



5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like ETX-A61 module, offer to the user very good performances in minimal spaces, therefore allowing the system's minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

ETX® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the ETX® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsink with fan in some situation can represent the cooling solution. Indeed, when using ETX-A61 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with fan could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide ETX-A61 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

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