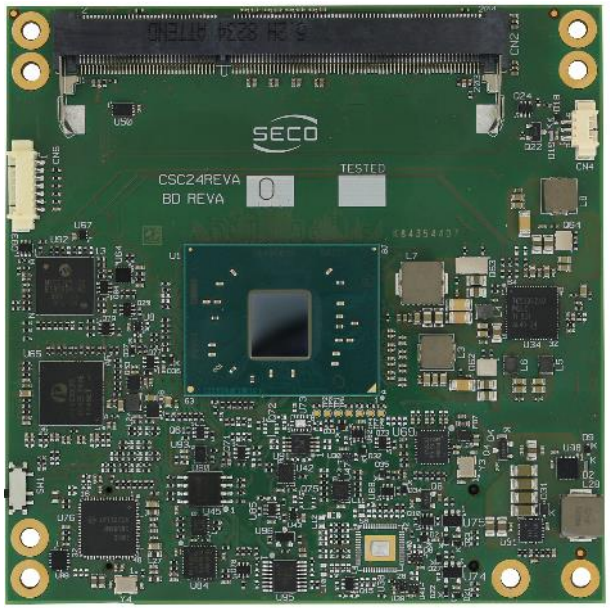
Com express

User Manual



COMe-C24 CT6

COM-Express™ Type 6 Module with the Intel®
Atom™, Pentium® and Celeron® CPUs

REVISION HISTORY

Revision	Date	Note	Rif
1.0	21 April 2021	First Official Release	AR
1.1	2 December 2021	Updated to PCB REV.C8 description and block design Changed fan connectors P/N and pictures (par. 3.2.1) BIOS documentation updated to Ver. 1.14	SO

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

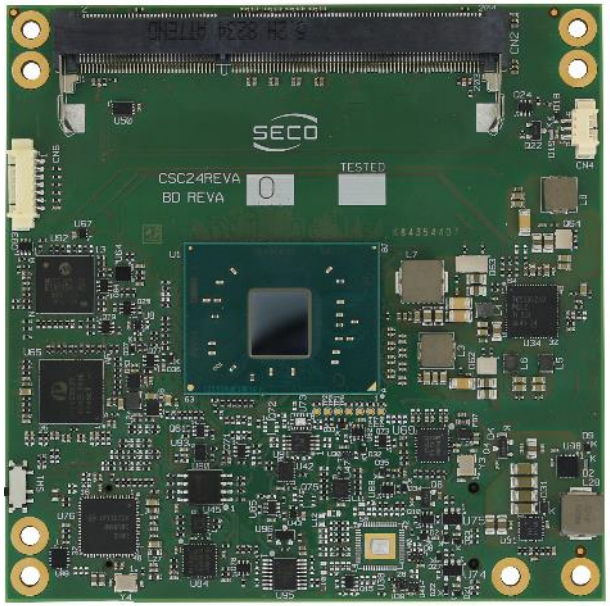
For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

INDEX

Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Safety Police
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipments and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The COMe-C24-CT6 module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!**
>
> Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.
>
> Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The COMe-C24-CT6 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!**
>
> Whenever handling a COMe-C24-CT6 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The COMe-C24-CT6 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Police

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, the COMe-C24 Module shall be:

- used inside a fire enclosure made of non-combustible material or V-1 material (the fire enclosure is not necessary if the maximum power supplied to the module never exceeds 100 W, even in worst-case fault);
- used inside an enclosure; the enclosure is not necessary if the temperature of the parts likely to be touched never exceeds 70 °C;
- installed inside an enclosure compliant with all applicable IEC 62368-1 requirements;

The manufacturer which include a COMe-C24 module in his end-user product shall:

- verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition
- Prescribe temperature and humidity range for operating, transport and storage conditions;
- Prescribe to perform maintenance on the module only when it is off and has already cooled down;
- Prescribe that the connections from or to the Module have to be compliant to ES1 requirements;
- The module in its enclosure must be evaluated for temperature and airflow considerations.

1.8 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CRT	Cathode Ray Tube. Initially used to indicate a type of monitor, this acronym has been used over time to indicate the analog video interface used to drive them.
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
DDR3	DDR, 3rd generation
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
ECC	Error Correcting Code, a peculiar type of memory module with 72-bit of data instead of 64, where the additional 8 bit are used to detect and correct possible errors on the remaining 64-bit data bus
eDP	embedded Display Port, a type of digital video display interface specifically developed for the internal connections between boards and digital displays
EMI	Electromagnetic Interference
GbE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signaling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
N.A.	Not Applicable

N.C.	Not Connected
OS	Operating System
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port
PCH	Platform Controller Hub
PCI-e	Peripheral Component Interface Express
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
PXE	Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signaling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
USB	Universal Serial Bus
V_REF	Voltage reference Pin
VGA	Video Graphics Array. An analog computer display standard, commonly referred to also as CRT.
xHCI	eXtensible Host Controller Interface, Host controller for USB 3.0 ports, which can also manage USB 2.0 and USB1.1 ports

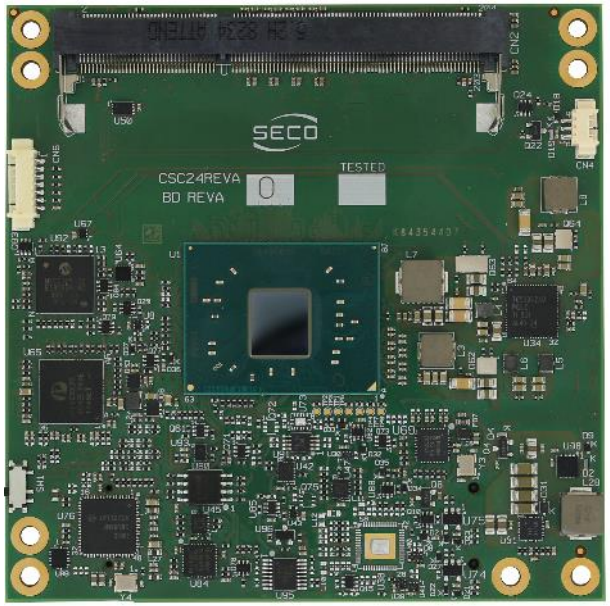
1.9 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
Com Express	https://www.picmg.org/openstandards/com-express/
Com Express Carrier Design Guide	http://picmg.org//wp-content/uploads/PICMG_COMDG_2.0-RELEASED-2013-12-061.pdf
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	https://cache.nxp.com/documents/user_manual/UM10204.pdf?fsrch=1&sr=2&pageNum=1
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SM Bus	http://www.smbus.org/specs
UEFI	http://www.uefi.org
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip
xHCI	http://www.intel.com/content/www/us/en/io/universal-serial-bus/extensible-host-controler-interface-usb-xhci.html?wapkw=xhci
Intel® Atom™, Pentium ® and Celeron® Apollo Lake family	http://ark.intel.com/products/codename/80644/Apollo-Lake#@Embedded

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram



2.1 Introduction

The COMe-C24-CT6 is a COM Express® Type 6, basic Form Factor, based on the Intel® Atom™ , Pentium® and Celeron® family of System-on-Chips (SOCs) formerly coded as Apollo Lake, a series of Single/ Dual / Quad SOCs with 64-bit instruction set.

These SOCs embed all the features usually obtained by combination of CPU + platform Controller hubs, all in one single IC, which allows, therefore, the system minimisation and performance optimisation. The CPUs have direct access to the memory, which is available on two SODIMM DDR3L memory modules, speed up to 1866MHz. Please notice that total amount of memory available is OS dependant.

All SOCs embed an Intel® HD Graphics 500 series controller, which offers an advanced 2D and 3D graphic engine and it is able to manage up to 3 independent displays (any combination possible between HDMI, DVI, DP++, eDP, LVDS and VGA). It makes available three Digital Display Interfaces that can be used to drive external Display Port, HDMI or DVI displays; moreover, the embedded Display Port interface can be carried out on COM Express connectors directly or used to realise a Dual Channel LVDS 18/24bit interface or a VGA interface (these are factory configurations).

The embedded PCH complete the functionalities of the board offering HD Audio Interface, up to 6 x PCI Express ports (one of them used to manage a Gigabit Ethernet controller), 2 x Serial ATA channels, up to 8 USB ports with up to 4 USB 3.0, Real Time Clock, SPI interface, 2xUARTs, LPC and SM Bus.

The module can be offered with an optional additional TPM module.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

The product is COM Express® Rel.3.0 standard compliant, an open industry standard defined specifically for COMs (computer on modules). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available. Specifically, COMe-C24-CT6 is a COM Express® module, Basic Form factor, Type 6 (95mm x 95mm).

COM Express® module integrates all the core components and has to be mounted onto an application-specific carrier board; carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimised package, which results in a more reliable product while simplifying system integration. Most important, COM Express® modules are scalable, which means that once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

2.2 Technical Specifications

CPU

Intel® Atom™ x5-E3930 Dual Core @1.3 GHz (Burst 1.8GHz), 2MB L2 Cache, 6.5W TDP
Intel® Atom™ x5-E3940 Quad Core @1.6 GHz (Burst 1.8GHz), 2MB L2 Cache, 9.5WTDP
Intel® Atom™ x7-E3950 Quad Core @1.6 GHz (Burst 2.0GHz), 2MB L2 Cache, 12W TDP
Intel® Pentium® N4200 Quad Core @1.1GHz (Burst 2.5GHz), 2MB L2 Cache, 6W TDP
Intel® Celeron® N3350 Dual Core @1.1GHz (Burst 2.4GHz), 2MB L2 Cache, 6W TDP
Intel® Celeron® J3455, Quad Core @1.5GHz (Burst 2.3GHz), 2MB L2Cache, 10W TDP
Intel® Celeron® J3355, Dual Core @2.0GHz (Burst 2.5GHz), 2MB L2Cache, 10W TDP

Memory

Two DDR3L SO-DIMM Slots supporting DDR3L-1866 non-ECC Memory, up to 8GB

Graphics

Intel® HD Graphics 500 series controller with up to 18 Execution Units
Up to 3 independent displays supported
HW decoding of HEVC(H.265), H.264, MVC, VP8, VP9, MPEG2, VC-1, WMV9, JPEG/MJPEG formats
HW encoding of HEVC(H.265), H.264, MVC, VP8, VP9 and JPEG/MPEG format

Video Interfaces

Up to 2 x Digital Display Interfaces (DDIs), supporting DP1.2, DVI and HDMI 1.4
eDP 1.3 or Single/Dual-Channel 18-/24- bit LVDS interface
optional VGA interface through a DP-to-VGA bridge

Video Resolutions

DP:	up to 4096x2160 @60Hz
eDP:	up to 3840x2160 @60Hz
HDMI:	up to 3840x2160 @30Hz
LVDS, VGA:	up to 1920x1200 @ 60Hz

Mass Storage

Optional eMMC 5.0 drive soldered on-board, up to 32GB
2 x external S-ATA Gen3 Channels

USB

8 x USB 2.0 Host Ports
Up to 4 x USB 3.0 Host ports

Networking

Optional Gigabit Ethernet interface
Intel® I210 or I211 GbE Controller (MAC + PHY)

Audio

HD Audio interface

PCI Express

Up to 5 x PCI-e x1 Gen2 lanes

Serial Ports

2 x UARTs

Other Interfaces

SPI, I2C, SM Bus, LPC bus, Thermal Management, FAN management
4 x GPI, 4 x GPO
LID# / SLEEP# / PWRBTN#, Watchdog
Optional TPM 2.0 on-board

Power supply voltage: +12V_{DC} ± 10% and + 5V_{SB} (optional)

Operating System:

Microsoft® Windows 10 Enterprise (64-bit)
Microsoft® Windows 10 IoT core
Wind River Linux (64 bit)
Yocto (64 bit)
Android (planning)

Operating temperature:

0°C ÷ +60°C (Commercial version) **

-40°C ÷ +85°C (Industrial version) **

Dimensions: 95 x 95 mm

! *** Temperatures indicated are the minimum and maximum temperature that the heatspreader / heatsink can reach in any of its parts. This means that it is customer's responsibility to use any passive cooling solution along with an application-dependent cooling system, capable to ensure that the heatspreader / heatsink temperature remains in the range above indicated. Please also check paragraph 5.1*

2.3 Electrical Specifications

According to COM Express® specifications, the COMe-C24-CT6 board needs to be supplied only with an external +12V_{DC} power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through COM Express Connectors CN1-AB and CN1-CD.

All remaining voltages needed for board's working are generated internally from +12V_{DC} power rail.

2.3.1 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

_SUS: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_SUS.

2.3.2 Power Consumption

COMe-C24-CT6 module, like all COM Express™ modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Therefore, power consumptions of the board are measured using a CCOMe-965 Carrier board on +12V_RUN power rail that supplies the board. For this reason, the values indicated in the table below are real power consumptions of the board, and are independent from those of the peripherals connected to the Carrier Board.

Power consumption in Suspend and Soft-Off States have been measured on +5V_ALW power rail. RTC power consumption has been measured on carrier board's backup battery when the system is not powered (VCC_RTC power rail). For the measurements, it has been used a DC Power Analyzer Keysight N6700B.

The current consumptions, written in the table of next page, have been measured using the following setup:

Board Configurations:

- O.S. Windows 10
- Intel™ Atom E3950 (config 1), Intel™ Atom E3940 (config 2), Intel™ Atom E3930 (config 3), Intel™ Pentium N4200 (config 4), Intel™ Celeron N3350 (config 5)
- eMMC 32GB
- TPM present, LVDS + DP (config 1,2,3) or eDP + VGA (config 4,5), Packed Switch + LAN (I210 on config 1,2,3, I211 on config 4,5), UART da EC, Industrial Temperature Range (config 1,2,3,5) or Commercial Temperature Range (config 4)
- 4GB DDR3L (2 x 2GB SO-DIMM DDR3L 1600MT/s modules on config 1,2,3) or 8GB DDR3L (2 x 4GB SO-DIMM DDR3L 1866MT/s modules on config 1,2,3)
- USB mouse and keyboard connected

Status	Config 1	Config 2	Config 3	Config 4	Config 5
Idle, power saving configuration	0,21A	0,24A	0,22A	0,2A	0,21A
OS Boot, power saving configuration	0,47A	0,43A	0,41	0,45A	0,47A
Video reproduction@720p, power saving configuration	0,37A	0,38A	0,21A	0,35A	0,42A
Video reproduction@1080p, power saving configuration	0,39A	0,22A	0,21A	0,34A	0,40A
Video reproduction@4K, power saving configuration	0,42A	0,43A	0,22A	0,40A	0,37A
Internal Test, maximum performance	1,82A	1,55A	0,46A	0,82A	0,85A
Suspend to RAM (typical)	75 mA	75 mA	75 mA	110 mA	85 mA
Soft Off (typical)	58 mA	58 mA	58 mA	68 mA	70 mA

2.4 Mechanical Specifications

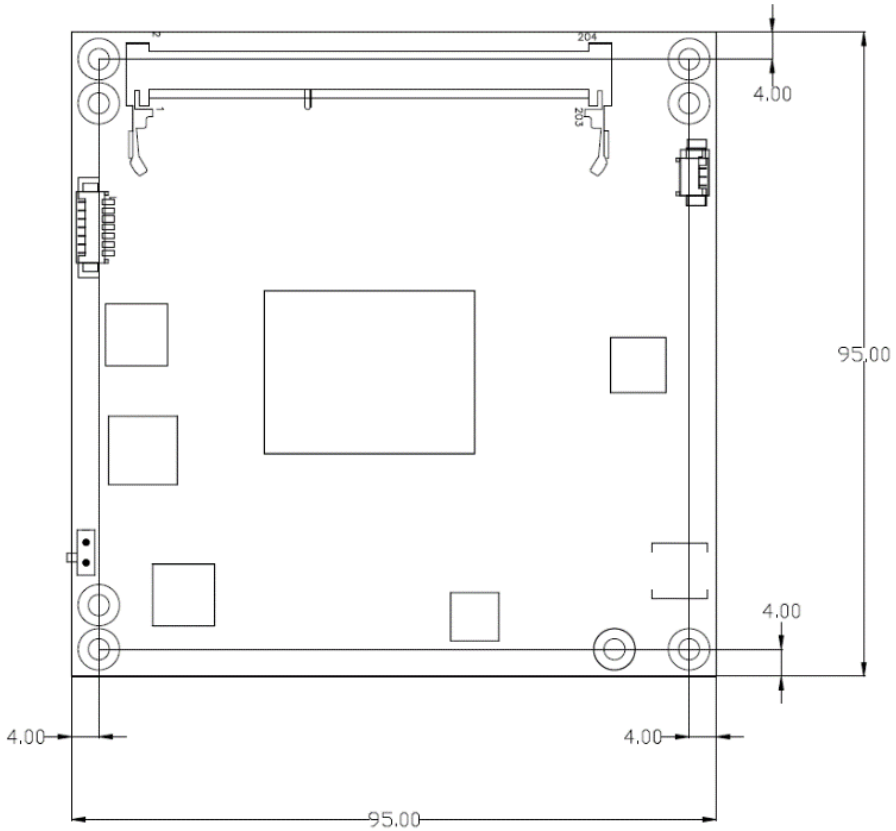
The COMe-C24-CT6 is a COM Express board, Compact form Factor type; therefore its dimensions are 95 mm x 95 mm (3.74" x 3.74").

Printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

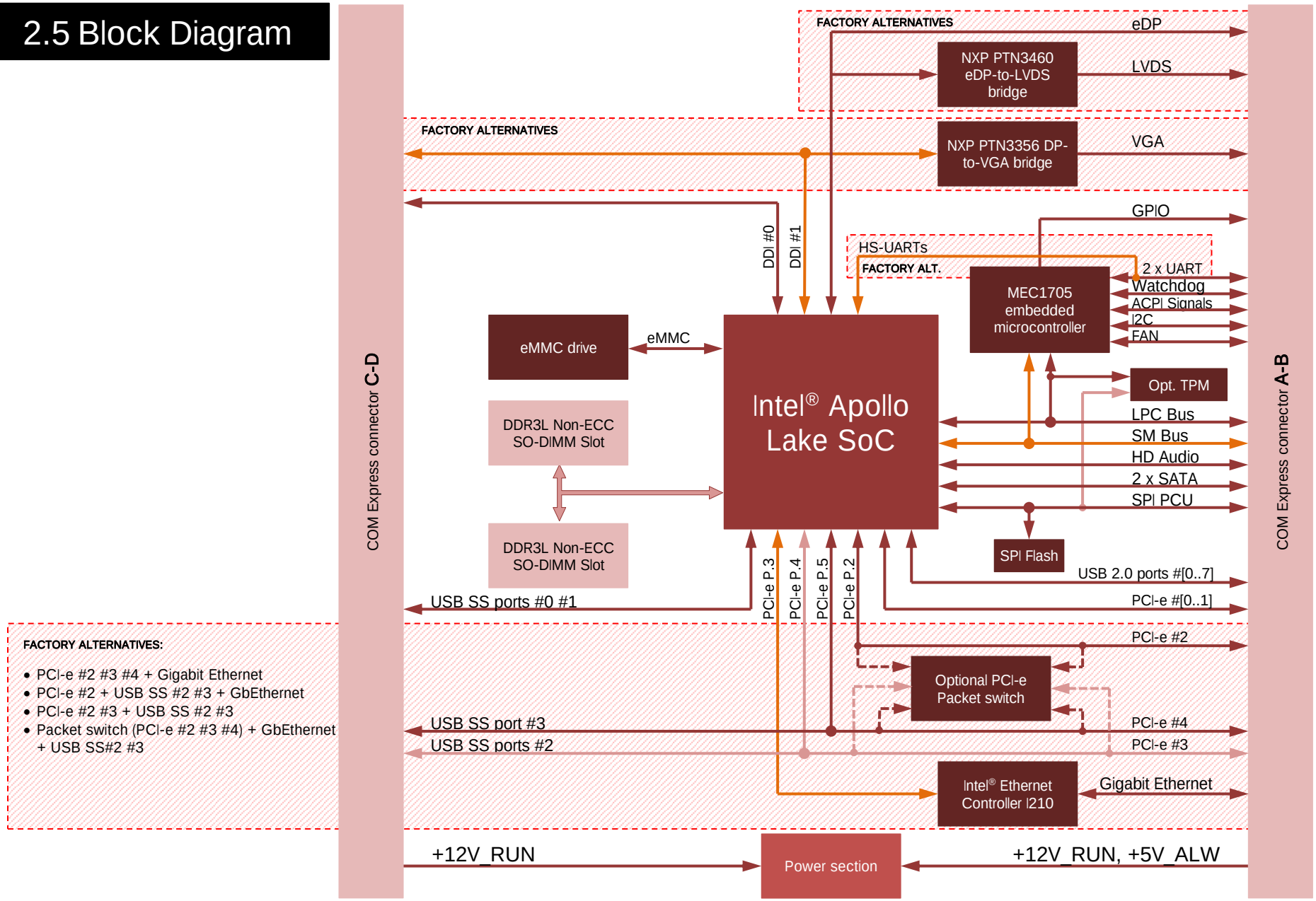
According to COM Express specifications, the carrier board plug can be of two different heights, 5mm and 8mm.

Whichever connector's height is chosen, in designing a custom carrier board please remember that the SO-DIMM connector on bottom side of COMe-C24-CT6 is 4mm high (it is the component with the maximum height).

This value must be kept in high consideration when choosing the carrier board plugs' height, if it is necessary to place components on the carrier board in the zone under the COM Express® module.

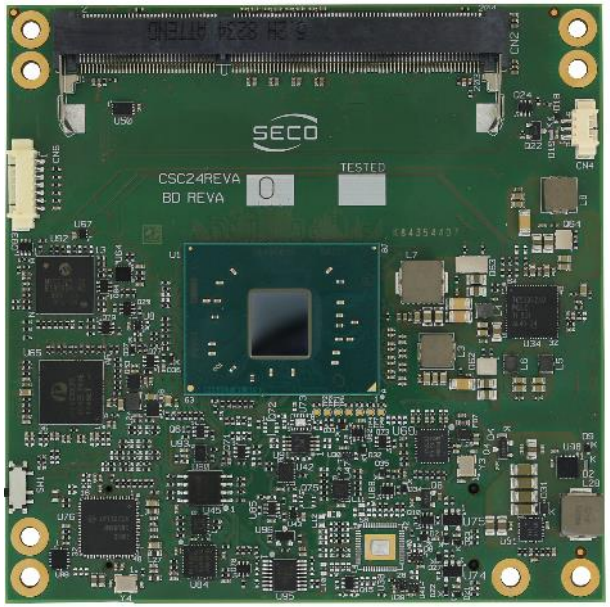


2.5 Block Diagram



Chapter 3.
CONNECTORS

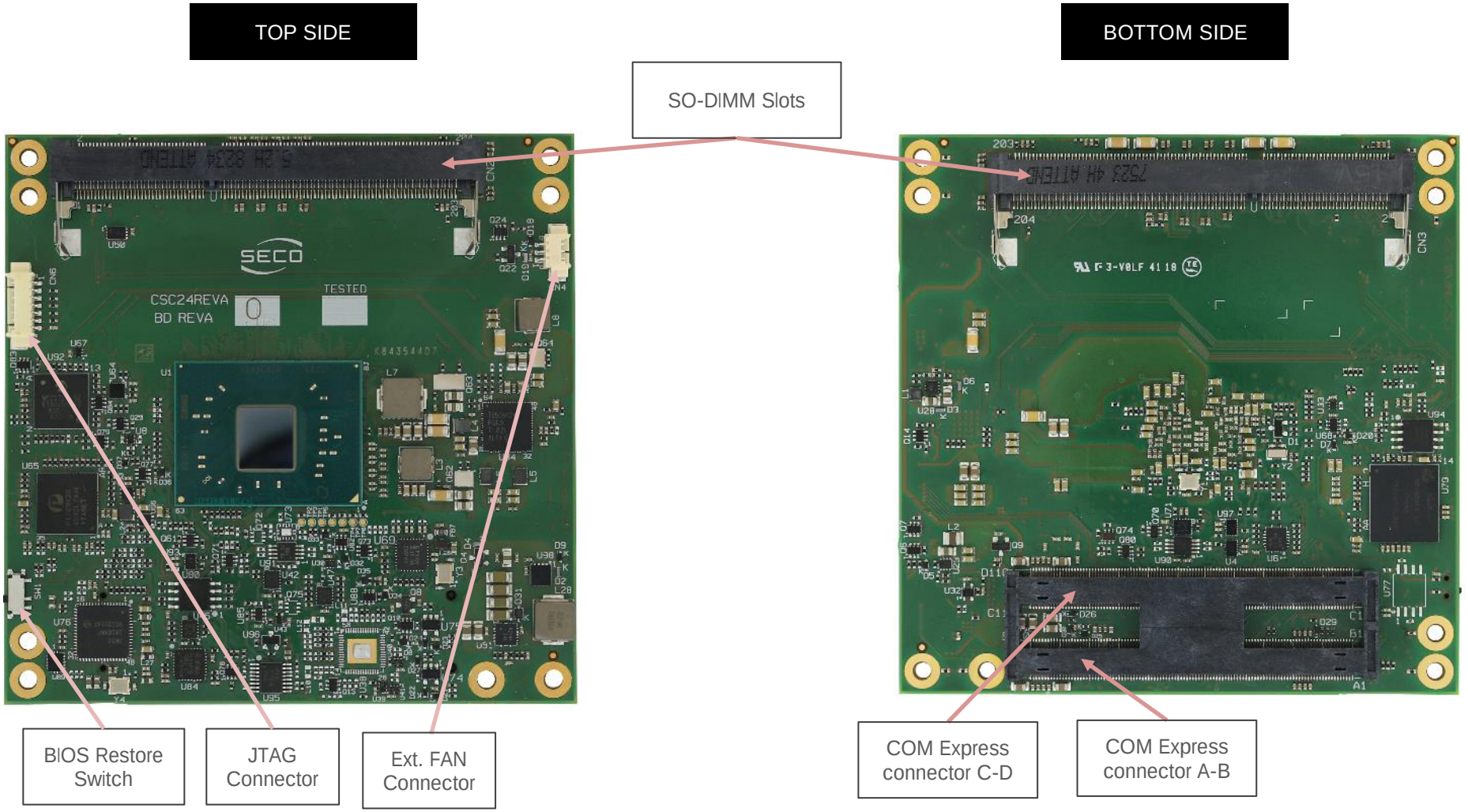
- Introduction
- Connectors description



3.1 Introduction

According to COM Express® specifications, all interfaces to the board are available through two 220 pin connectors, for a total of 440 pin. Simplifying the terminology in this documentation, the primary connector is called A-B and the secondary C-D, since each one consists of two rows.

In addition, a Fan connector has been placed on one side of the board, in order to allow an easier connection of active heatsinks to the module.

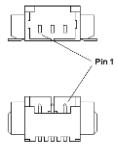


3.2 Connectors description

3.2.1 FAN Connector

FAN Connector - CN4	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN

Depending on the usage model of COMe-C24-CT6 module, for critical applications/environments on the module itself it is available a 3-pin dedicated connector for an external +12VDC FAN.



FAN Connector is a 3-pin single line SMT connector, type MOLEX 53261-0371 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

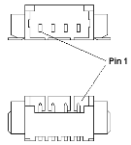
Please refer to chapter 5.1 for considerations about thermal dissipation.

FAN_POWER: +12V_RUN derived power rail for FAN, managed by the embedded microcontroller via PWM signal.

FAN_TACHO_IN: tachometric input from the fan to the embedded microcontroller, +3.3V_RUN electrical level signal with 10kΩ pull-up resistor and Schottky diode.

FAN Connector – CN7	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN
4	FAN_PWM

As a factory alternative, onboard it is available a 4-pin connector, type MOLEX 53261-0471 or equivalent, for the connection of tachometric FANs.



Mating connector: MOLEX 51021-0400 receptacle with MOLEX 50079-8000 female crimp terminals.

FAN_POWER: +12V_RUN derived power rail for FAN

FAN_TACHO_IN: tachometric input from the fan to the embedded microcontroller, +3.3V_RUN electrical level signal with 10kΩ pull-up resistor and Schottky diode.

FAN_PWM: +3.3V_RUN fan PWM input managed by the embedded microcontroller.

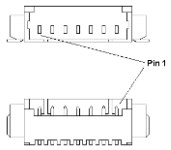
3.2.2 JTAG Connector

JTAG connector– CN6	
Pin	Signal
1	VDD
2	LM4_TMS
3	LM4_TCK
4	LM4_TDI
5	LM4_TD0
6	LM4_NRST
7	GND

The Apollo Lake family of processors does provide a JTAG interface, for test and debug purposes.

This interface is available through a on module connector CN6, type MOLEX p/n 53261-0719.

All these JTAG signals are at electrical level +3.3V_ALW with 10k pull-up resistor and are directly connected to SOC pins with same name. Please refer to Apollo Lake family of processors documentation for a description of the signals and their usage.



3.2.3 SO-DIMM DDR3 Slots

CPUs used on the COMe-C24-CT6 board provide support to DDR3L-1866 non-ECC memories, up to 8GB, which can be integrated by using the dedicated DDR3L SO-DIMM sockets.

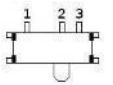
For use of this memories, on board there are two SO-DIMM DDR3 sockets.

The socket placed on top side (CN2) is type ATTEND 122A-52A10 or equivalent, a right angle, low profile, reverse type socket, used for high speed system memory applications.

The socket placed on bottom side (CN3) is type ATTEND 122A-40A00 or equivalent, and is a socket with performances similar to the other, only it is standard type, not reverse. The two sockets together allow the insertion of up to 2 SO-DIMM modules, for support of dual channel memories.

3.2.4 BIOS Restore switch

In some cases, a wrong configuration of BIOS parameters could lead the module in an unusable state (i.e. no video output, all USB HID devices disabled).



For these cases, on the module it has been placed a 3-way switch SW1 which can be used to restore the BIOS to factory default configuration. To do so, it is necessary to place the contact of the switch in 1-2 position, then turn on the module, wait until the board has started regularly then turn off the module. The contact MUST be now placed back to 2-3 position.

During normal use, the contact MUST be always placed in 2-3 position.

3.2.5 COM Express® Module connectors

For the connection of COM Express® CPU modules, on board there is one double connector, type TYCO 3-1827231-6 (440 pin, ultra thin, 0.5mm pitch, h=4mm), as requested by COM Express® specifications.

The pinout of the module is compliant to COM Express® Type 6 specifications. Not all the signals contemplated in COM Express® standard are implemented on the double connector, due to the functionalities really implemented on COMe-C24-CT6 board. Therefore, please refer to the following table for a list of effective signals reported on the connector. For accurate signals description, please consult the following paragraphs.

COM Express® Connector CN1 – Rows A & B

		ROW A			ROW B		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	A1	B1	GND	PWR	
GBE	I/O	GBE0_MDI3-	A2	B2	GBE0_ACT#	O	GBE
GBE	I/O	GBE0_MDI3+	A3	B3	LPC_FRAME#	O	LPC
GBE	O	GBE0_LINK100#	A4	B4	LPC_AD0	I/O	LPC
GBE	O	GBE0_LINK1000#	A5	B5	LPC_AD1	I/O	LPC
GBE	I/O	GBE0_MDI2-	A6	B6	LPC_AD2	I/O	LPC
GBE	I/O	GBE0_MDI2+	A7	B7	LPC_AD3	I/O	LPC
GBE	O	GBE0_LINK#	A8	B8	LPC_DRQ0#	I	LPC
GBE	I/O	GBE0_MDI1-	A9	B9	LPC_DRQ1#	I	LPC
GBE	I/O	GBE0_MDI1+	A10	B10	LPC_CLK	O	LPC
	PWR	GND	A11	B11	GND	PWR	
GBE	I/O	GBE0_MDI0-	A12	B12	PWRBTN#	I	PWR_MGMT
GBE	I/O	GBE0_MDI0+	A13	B13	SMB_CK	I/O	SMBUS
	N.A.	N.C.	A14	B14	SMB_DAT	O	SMBUS
PWR_MGMT	O	SUS_S3#	A15	B15	SMB_ALERT#	I	SMBUS
SATA	O	SATA0_TX+	A16	B16	SATA1_TX+	O	SATA
SATA	O	SATA0_TX-	A17	B17	SATA1_TX-	O	SATA
PWR_MGMT	O	SUS_S5#	A18	B18	SUS_STAT#	O	PWR_MGMT
SATA	I	SATA0_RX+	A19	B19	SATA1_RX+	I	SATA
SATA	I	SATA0_RX-	A20	B20	SATA1_RX-	I	SATA

	PWR	GND	A21	B21	GND	PWR	
	N.A.	N.C.	A22	B22	N.C.	N.A.	
	N.A.	N.C.	A23	B23	N.C.	N.A.	
PWR_MGMT	O	SUS_S5#	A24	B24	PWR_OK	I	PWR_MGMT
	N.A.	N.C.	A25	B25	N.C.	N.A.	
	N.A.	N.C.	A26	B26	N.C.	N.A.	
PWR_MGMT	I	BATLOW#	A27	B27	WDT	O	MISC
SATA	O	SATA_ACT#	A28	B28	N.C.	N.A.	
AUDIO	O	HDA_SYNC	A29	B29	N.C.	N.A.	
AUDIO	O	HDA_RST#	A30	B30	HDA_SDIN0	I/O	AUDIO
	PWR	GND	A31	B31	GND	PWR	
AUDIO	O	HDA_BITCLK	A32	B32	SPKR	O	MISC
AUDIO	O	HDA_SDOUT	A33	B33	I2C_CK	O	I2C
SPI	I	BIOS_DIS0#	A34	B34	I2C_DAT	I/O	I2C
MISC	O	THRMTRIP#	A35	B35	THRM#	I	MISC
USB	I/O	USB6-	A36	B36	USB7-	I/O	USB
USB	I/O	USB6+	A37	B37	USB7+	I/O	USB
USB	I	USB_6_7_OC#	A38	B38	USB_4_5_OC#	I	USB
USB	I/O	USB4-	A39	B39	USB5-	I/O	USB
USB	I/O	USB4+	A40	B40	USB5+	I/O	USB
	PWR	GND	A41	B41	GND	PWR	
USB	I/O	USB2-	A42	B42	USB3-	I/O	USB
USB	I/O	USB2+	A43	B43	USB3+	I/O	USB
USB	I	USB_2_3_OC#	A44	B44	USB_0_1_OC#	I	USB
USB	I/O	USB_0-	A45	B45	USB1-	I/O	USB
USB	I/O	USB_0+	A46	B46	USB1+	I/O	USB
	PWR	VCC_RTC	A47	B47	ESPI_EN#	I	SPI
	N.A.	N.C.	A48	B48	USB0_HOST_PRSNT	I	USB
	N.A.	N.C.	A49	B49	SYS_RESET#	I	PWR_MGMT
LPC	I/O	LPC_SERIRQ	A50	B50	CB_RESET#	O	PWR_MGMT

	PWR	GND	A51	B51	GND	PWR	
	N.A.	N.C.	A52	B52	N.C.	N.A.	
	N.A.	N.C.	A53	B53	N.C.	N.A.	
GPIO	I	GPI0	A54	B54	GPO1	O	GPIO
PCIE	O	PCIE_TX4+	A55	B55	PCIE_RX4+	I	PCIE
PCIE	O	PCIE_TX4-	A56	B56	PCIE_RX4-	I	PCIE
	PWR	GND	A57	B57	GPO2	O	GPIO
PCIE	O	PCIE_TX3+	A58	B58	PCIE_RX3+	I	PCIE
PCIE	O	PCIE_TX3-	A59	B59	PCIE_RX3-	I	PCIE
	PWR	GND	A60	B60	GND	PWR	
PCIE	O	PCIE_TX2+	A61	B61	PCIE_RX2+	I	PCIE
PCIE	O	PCIE_TX2-	A62	B62	PCIE_RX2-	I	PCIE
GPIO	I	GPI1	A63	B63	GPO3	O	GPIO
PCIE	O	PCIE_TX1+	A64	B64	PCIE_RX1+	I	PCIE
PCIE	O	PCIE_TX1-	A65	B65	PCIE_RX1-	I	PCIE
	PWR	GND	A66	B66	WAKE0#	I	PWR_MGMT
GPIO	I	GPI2	A67	B67	WAKE1#	I	PWR_MGMT
PCIE	O	PCIE_TX0+	A68	B68	PCIE_RX0+	I	PCIE
PCIE	O	PCIE_TX0-	A69	B69	PCIE_RX0-	I	PCIE
	PWR	GND	A70	B70	GND	PWR	
eDP/LVDS	O	eDP_TX2+/LVDS_A0+	A71	B71	LVDS_B0+	O	LVDS
eDP/LVDS	O	eDP_TX2-/LVDS_A0-	A72	B72	LVDS_B0-	O	LVDS
eDP/LVDS	O	eDP_TX1+/LVDS_A1+	A73	B73	LVDS_B1+	O	LVDS
eDP/LVDS	O	eDP_TX1-/LVDS_A1-	A74	B74	LVDS_B1-	O	LVDS
eDP/LVDS	O	eDP_TX0+/LVDS_A2+	A75	B75	LVDS_B2+	O	LVDS
eDP/LVDS	O	eDP_TX0-/LVDS_A2-	A76	B76	LVDS_B2-	O	LVDS
eDP/LVDS	O	eDP/LVDS_VDD_EN	A77	B77	LVDS_B3+	O	LVDS
LVDS	O	LVDS_A3+	A78	B78	LVDS_B3-	O	LVDS
LVDS	O	LVDS_A3-	A79	B79	eDP/LVDS_BKLT_EN	O	eDP/LVDS
	PWR	GND	A80	B80	GND	PWR	

eDP/LVDS	O	eDP_TX3+/LVDS_A_CK+	A81	B81	LVDS_B_CK+	O	LVDS
eDP/LVDS	O	eDP_TX3-/LVDS_A_CK-	A82	B82	LVDS_B_CK-	O	LVDS
eDP/LVDS	I/O	eDP_AUX+/LVDS_I2C_CK	A83	B83	eDP/LVDS_BKLT_CTRL	O	eDP/LVDS
eDP/LVDS	I/O	eDP_AUX-/LVDS_I2C_DAT	A84	B84	+5V_ALW	PWR	
GPIO	I	GPI3	A85	B85	+5V_ALW	PWR	
	N.A.	N.C.	A86	B86	+5V_ALW	PWR	
eDP	I	eDP_HPD	A87	B87	+5V_ALW	PWR	
PCIE	O	PCIE_CLK_REF+	A88	B88	BIOS_DIS1#	I	SPI
PCIE	O	PCIE_CLK_REF-	A89	B89	VGA_RED	O	VGA
	PWR	GND	A90	B90	GND	PWR	
SPI	O	SPI_POWER	A91	B91	VGA_GRN	O	VGA
SPI	I	SPI_MISO	A92	B92	VGA_BLU	O	VGA
GPIO	O	GPO0	A93	B93	VGA_HSYNC	O	VGA
SPI	O	SPI_CLK	A94	B94	VGA_VSYNC	O	VGA
SPI	O	SPI_MOSI	A95	B95	VGA_I2C_CK	I/O	VGA
MISC	I	TPM_PP	A96	B96	VGA_I2C_DAT	I/O	VGA
TYPE	N.A.	TYPE10#: N.C.	A97	B97	SPI_CS#	O	SPI
UART	O	SER0_TX	A98	B98	N.C.	N.A.	
UART	I	SER0_RX	A99	B99	N.C.	N.A.	
	PWR	GND	A100	B100	GND	PWR	
UART	O	SER1_TX	A101	B101	FAN_PWMOUT	O	MISC
UART	I	SER1_RX	A102	B102	FAN_TACHIN	I	MISC
PWR_MGMT	I	LID#	A103	B103	SLEEP#	I	PWR_MGMT
	PWR	+12V_RUN	A104	B104	+12V_RUN	PWR	
	PWR	+12V_RUN	A105	B105	+12V_RUN	PWR	
	PWR	+12V_RUN	A106	B106	+12V_RUN	PWR	
	PWR	+12V_RUN	A107	B107	+12V_RUN	PWR	
	PWR	+12V_RUN	A108	B108	+12V_RUN	PWR	
	PWR	+12V_RUN	A109	B109	+12V_RUN	PWR	
	PWR	GND	A110	B110	GND	PWR	

COM Express® Connector CN1 – Rows C & D							
		ROW C			ROW D		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	C1	D1	GND	PWR	
	PWR	GND	C2	D2	GND	PWR	
USB	I	USB_SSRX0-	C3	D3	USB_SSTX0-	O	USB
USB	I	USB_SSRX0+	C4	D4	USB_SSTX0+	O	USB
	PWR	GND	C5	D5	GND	PWR	
USB	I	USB_SSRX1-	C6	D6	USB_SSTX1-	O	USB
USB	I	USB_SSRX1+	C7	D7	USB_SSTX1+	O	USB
	PWR	GND	C8	D8	GND	PWR	
USB	I	USB_SSRX2-	C9	D9	USB_SSTX2-	O	USB
USB	I	USB_SSRX2+	C10	D10	USB_SSTX2+	O	USB
	PWR	GND	C11	D11	GND	PWR	
USB	I	USB_SSRX3-	C12	D12	USB_SSTX3-	O	USB
USB	I	USB_SSRX3+	C13	D13	USB_SSTX3+	O	USB
	PWR	GND	C14	D14	GND	PWR	
	N.A.	N.C.	C15	D15	DDI1_CTRLCLK_AUX+	I/O	DDI
	N.A.	N.C.	C16	D16	DDI1_CTRLDATA_AUX-	I/O	DDI
	N.A.	N.C.	C17	D17	N.C.	N.A.	
	N.A.	N.C.	C18	D18	N.C.	N.A.	
	N.A.	N.C.	C19	D19	N.C.	N.A.	
	N.A.	N.C.	C20	D20	N.C.	N.A.	
	PWR	GND	C21	D21	GND	PWR	
	N.A.	N.C.	C22	D22	N.C.	N.A.	
	N.A.	N.C.	C23	D23	N.C.	N.A.	
DDI	I	DDI1_HPD	C24	D24	N.C.	N.A.	
	N.A.	N.C.	C25	D25	N.C.	N.A.	
	N.A.	N.C.	C26	D26	DDI1_PAIR0+	O	DDI

	N.A.	N.C.	C27	D27	DDI1_PAIR0-	O	DDI
	N.A.	N.C.	C28	D28	N.C.	N.A.	
	N.A.	N.C.	C29	D29	DDI1_PAIR1+	O	DDI
	N.A.	N.C.	C30	D30	DDI1_PAIR1-	O	DDI
	PWR	GND	C31	D31	GND	PWR	
DDI	I/O	DDI2_CTRLCLK_AUX+	C32	D32	DDI1_PAIR2+	O	DDI
DDI	I/O	DDI2_CTRLDATA_AUX-	C33	D33	DDI1_PAIR2-	O	DDI
DDI	I	DDI2_DDC_AUX_SEL	C34	D34	DDI1_DDC_AUX_SEL	I	DDI
	N.A.	N.C.	C35	D35	N.C.	N.A.	
	N.A.	N.C.	C36	D36	DDI1_PAIR3+	O	DDI
	N.A.	N.C.	C37	D37	DDI1_PAIR3-	O	DDI
DDI	I	DDI3_DDC_AUX_SEL	C38	D38	N.C.	N.A.	
	N.A.	N.C.	C39	D39	DDI2_PAIR0+	O	DDI
	N.A.	N.C.	C40	D40	DDI2_PAIR0-	O	DDI
	PWR	GND	C41	D41	GND	PWR	
	N.A.	N.C.	C42	D42	DDI2_PAIR1+	O	DDI
	N.A.	N.C.	C43	D43	DDI2_PAIR1-	O	DDI
DDI	I	DDI3_HPD	C44	D44	DDI2_HPD	I	DDI
	N.A.	N.C.	C45	D45	N.C.	N.A.	
	N.A.	N.C.	C46	D46	DDI2_PAIR2+	O	DDI
	N.A.	N.C.	C47	D47	DDI2_PAIR2-	O	DDI
	N.A.	N.C.	C48	D48	N.C.	N.A.	
	N.A.	N.C.	C49	D49	DDI2_PAIR3+	O	DDI
	N.A.	N.C.	C50	D50	DDI2_PAIR3-	O	DDI
	PWR	GND	C51	D51	GND	PWR	
	N.A.	N.C.	C52	D52	N.C.	N.A.	
	N.A.	N.C.	C53	D53	N.C.	N.A.	
	N.A.	N.C.	C54	D54	N.C.	N.A.	
	N.A.	N.C.	C55	D55	N.C.	N.A.	
	N.A.	N.C.	C56	D56	N.C.	N.A.	

N.A.	N.C.	C57	D57	N.C.	N.A.
N.A.	N.C.	C58	D58	N.C.	N.A.
N.A.	N.C.	C59	D59	N.C.	N.A.
PWR	GND	C60	D60	GND	PWR
N.A.	N.C.	C61	D61	N.C.	N.A.
N.A.	N.C.	C62	D62	N.C.	N.A.
N.A.	N.C.	C63	D63	N.C.	N.A.
N.A.	N.C.	C64	D64	N.C.	N.A.
N.A.	N.C.	C65	D65	N.C.	N.A.
N.A.	N.C.	C66	D66	N.C.	N.A.
N.A.	N.C.	C67	D67	GND	PWR
N.A.	N.C.	C68	D68	N.C.	N.A.
N.A.	N.C.	C69	D69	N.C.	N.A.
PWR	GND	C70	D70	GND	PWR
N.A.	N.C.	C71	D71	N.C.	N.A.
N.A.	N.C.	C72	D72	N.C.	N.A.
PWR	GND	C73	D73	GND	PWR
N.A.	N.C.	C74	D74	N.C.	N.A.
N.A.	N.C.	C75	D75	N.C.	N.A.
PWR	GND	C76	D76	GND	PWR
N.A.	N.C.	C77	D77	N.C.	N.A.
N.A.	N.C.	C78	D78	N.C.	N.A.
N.A.	N.C.	C79	D79	N.C.	N.A.
PWR	GND	C80	D80	GND	PWR
N.A.	N.C.	C81	D81	N.C.	N.A.
N.A.	N.C.	C82	D82	N.C.	N.A.
N.A.	N.C.	C83	D83	N.C.	N.A.
PWR	GND	C84	D84	GND	PWR
N.A.	N.C.	C85	D85	N.C.	N.A.
N.A.	N.C.	C86	D86	N.C.	N.A.

PWR	GND	C87	D87	GND	PWR
N.A.	N.C.	C88	D88	N.C.	N.A.
N.A.	N.C.	C89	D89	N.C.	N.A.
PWR	GND	C90	D90	GND	PWR
N.A.	N.C.	C91	D91	N.C.	N.A.
N.A.	N.C.	C92	D92	N.C.	N.A.
PWR	GND	C93	D93	GND	PWR
N.A.	N.C.	C94	D94	N.C.	N.A.
N.A.	N.C.	C95	D95	N.C.	N.A.
PWR	GND	C96	D96	GND	PWR
N.A.	N.C.	C97	D97	N.C.	N.A.
N.A.	N.C.	C98	D98	N.C.	N.A.
N.A.	N.C.	C99	D99	N.C.	N.A.
PWR	GND	C100	D100	GND	PWR
N.A.	N.C.	C101	D101	N.C.	N.A.
N.A.	N.C.	C102	D102	N.C.	N.A.
PWR	GND	C103	D103	GND	PWR
PWR	+12V_RUN	C104	D104	+12V_RUN	PWR
PWR	+12V_RUN	C105	D105	+12V_RUN	PWR
PWR	+12V_RUN	C106	D106	+12V_RUN	PWR
PWR	+12V_RUN	C107	D107	+12V_RUN	PWR
PWR	+12V_RUN	C108	D108	+12V_RUN	PWR
PWR	+12V_RUN	C109	D109	+12V_RUN	PWR
PWR	GND	C110	D110	GND	PWR

3.2.5.1 Audio interface signals

The COMe-C24-CT6 module supports HD audio format, thanks to native support offered by the processor to this audio codec standard.

Here following the signals related to HD Audio interface:

HDA_SYNC: HD Audio Serial Bus Synchronization. 48kHz fixed rate output from the module to the Carrier board, electrical level +3.3V_RUN.

HDA_RST#: HD Audio Codec Reset. Active low signal, output from the module to the Carrier board, electrical level +3.3V_RUN.

HDA_BITCLK: HD Audio Serial Bit Clock signal. 24MHz serial data clock generated by the Intel HD audio controller, output from the module to the Carrier board, electrical level +3.3V_RUN.

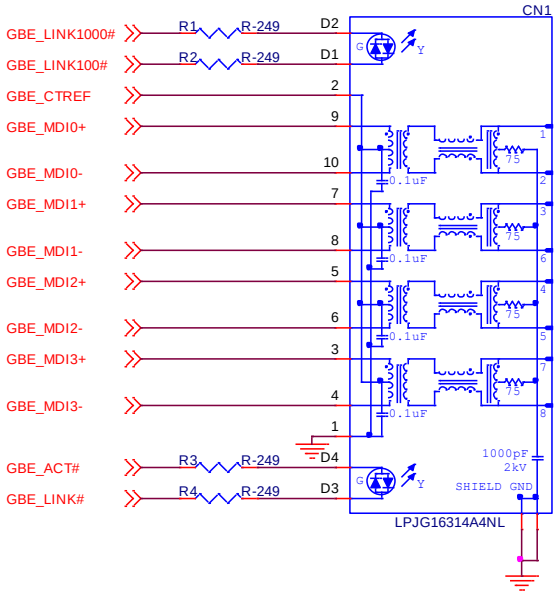
HDA_SDOUT: HD Audio Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_RUN.

HDA_SDIN0: HD Audio Serial Data In signal. Input to the module from the Codec placed on the Carrier board, electrical level +3.3V_RUN.

All these signals have to be connected, on the Carrier Board, to an HD Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.5.2 Gigabit Ethernet signals

The Gigabit Ethernet interface is realised, on COMe-C24-CT6 module, using an Intel® I210 Gigabit Ethernet controller, which is interfaced to the SOC through a dedicated PCI-express root port.



Here following the signals involved in PCI express management

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE0_ACT#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_ALW.

GBE0_LINK#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_ALW.

GBE0_LINK100#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_ALW.

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator, Active Low Output signal, electrical level +3.3V_ALW.

These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected. Please look to the schematic given as an example of implementation of Gigabit Ethernet connector. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. Intel® I210 Gigabit Ethernet controller, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on COM Express® connector AB.

All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.p.A. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

3.2.5.3 S-ATA signals

The Intel® family of SOCs formerly coded as Apollo Lake offers two S-ATA interfaces, which are carried out on the golden finger connector.

The interfaces are Gen3 compliant, with support of 1.5Gbps, 3.0 Gbps and 6.0 Gbps data rates.

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair.

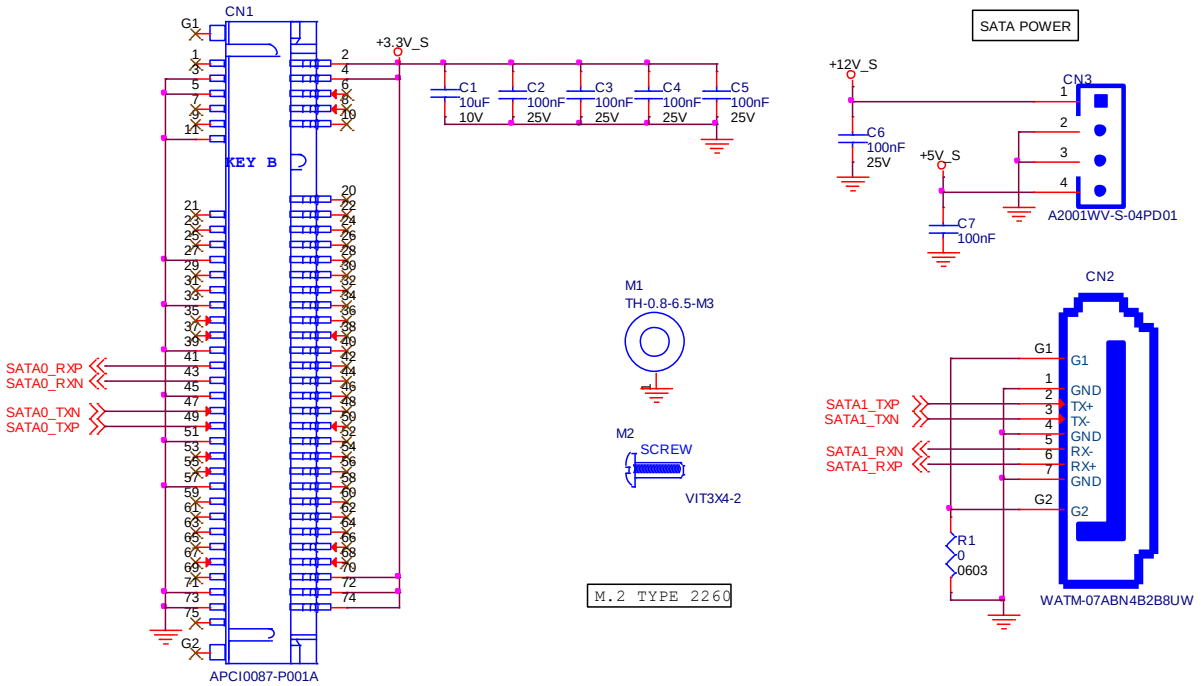
SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair.

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair.

SATA_ACT#: Serial ATA Activity Led. Active low output signal at +3.3V_RUN voltage.

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

On the carrier board, these signals can be carried out directly to the SATA connectors, like in the following example schematics.



3.2.5.4 PCI Express interface signals

COMe-C24-CT6 can offer externally up to five PCI Express lane, which are managed by the Intel® family of SOCs formerly coded as Apollo Lake.

PCI express Gen 2.0 (5Gbps) is supported.

The four PCI-e lanes from #0 to #3 can be managed as single PCI-e x4 port or 4 PCI-e x1 ports.

Please also be aware that these groupings cannot be changed dynamically, it is a fixed feature of the BIOS.

When ordering a COMe-C24-CT6 module, please take care of specifying which are the desired PCI-e groupings.

The single PCIe x4 port option is only available when USB Super Speed Port #2 , USB Super Speed Port #3 and Gigabit Ethernet Controller are not present.

Here following the signals involved in PCI express management:

PCIE_TX0+/PCIE_TX0-: PCI Express lane #0, Transmitting Output Differential pair

PCIE_RX0+/PCIE_RX0-: PCI Express lane #0, Receiving Input Differential pair

PCIE_TX1+/PCIE_TX1-: PCI Express lane #1, Transmitting Output Differential pair

PCIE_RX1+/PCIE_RX1-: PCI Express lane #1, Receiving Input Differential pair

PCIE_TX2+/PCIE_TX2-: PCI Express lane #2, Transmitting Output Differential pair

PCIE_RX2+/PCIE_RX2-: PCI Express lane #2, Receiving Input Differential pair

PCIE_TX3+/PCIE_TX3-: PCI Express lane #3, Transmitting Output Differential pair

PCIE_RX3+/PCIE_RX3-: PCI Express lane #3, Receiving Input Differential pair

PCIE_TX4+/PCIE_TX4-: PCI Express lane #4, Transmitting Output Differential pair

PCIE_RX4+/PCIE_RX4-: PCI Express lane #4, Receiving Input Differential pair

PCIE_CLK_REF+/ PCIE_CLK_REF-: PCI Express 100MHz Reference Clock, Differential Pair. Please consider that only one reference clock is supplied, while there are five different PCI express lanes. When more than one PCI Express lane is used on the carrier board, then a zero-delay buffer must be used to replicate the reference clock to all the devices.

3.2.5.5 USB interface signals

The Intel® family of SOCs formerly coded as Apollo Lake offers an xHCI controller, which is able to manage up to 4 Superspeed ports (i.e. USB 3.0 compliant), one of them also capable of OTG, plus up to 8 Ports able to work in USB 2.0 mode only. Via BIOS settings it is possible to enable or disable the xHCI controller, therefore enabling USB 3.0 functionalities or leaving only USB 1.1 and USB 2.0 support.

All USB 2.0 ports are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Here following the signals related to USB interfaces.

USB_0+/USB_0-: Universal Serial Bus Port #0 bidirectional differential pair

USB_1+/USB_1-: Universal Serial Bus Port #1 bidirectional differential pair

USB_2+/USB_2-: Universal Serial Bus Port #2 bidirectional differential pair

USB_3+/USB_3-: Universal Serial Bus Port #3 bidirectional differential pair

USB_4+/USB_4-: Universal Serial Bus Port #4 bidirectional differential pair

USB_5+/USB_5-: Universal Serial Bus Port #5 bidirectional differential pair

USB_6+/USB_6-: Universal Serial Bus Port #6 bidirectional differential pair

USB_7+/USB_7-: Universal Serial Bus Port #7 bidirectional differential pair

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair

USB_SSRX3+/USB_SSRX3-: USB Super Speed Port #3 receive differential pair

USB_SSTX3+/USB_SSTX3-: USB Super Speed Port #3 transmit differential pair

USB_0_1_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port#0 and #1 of COMe-C24-CT6 module

USB_2_3_OC#: USB Over Current Detect Input. Active Low Input signa.l, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Ports #2 and #3 of COMe-C24-CT6 module.

USB_4_5_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #4 and/or #5 of COMe-C24-CT6 module.

USB_6_7_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #6 and/or #7 of COMe-C24-CT6 module.

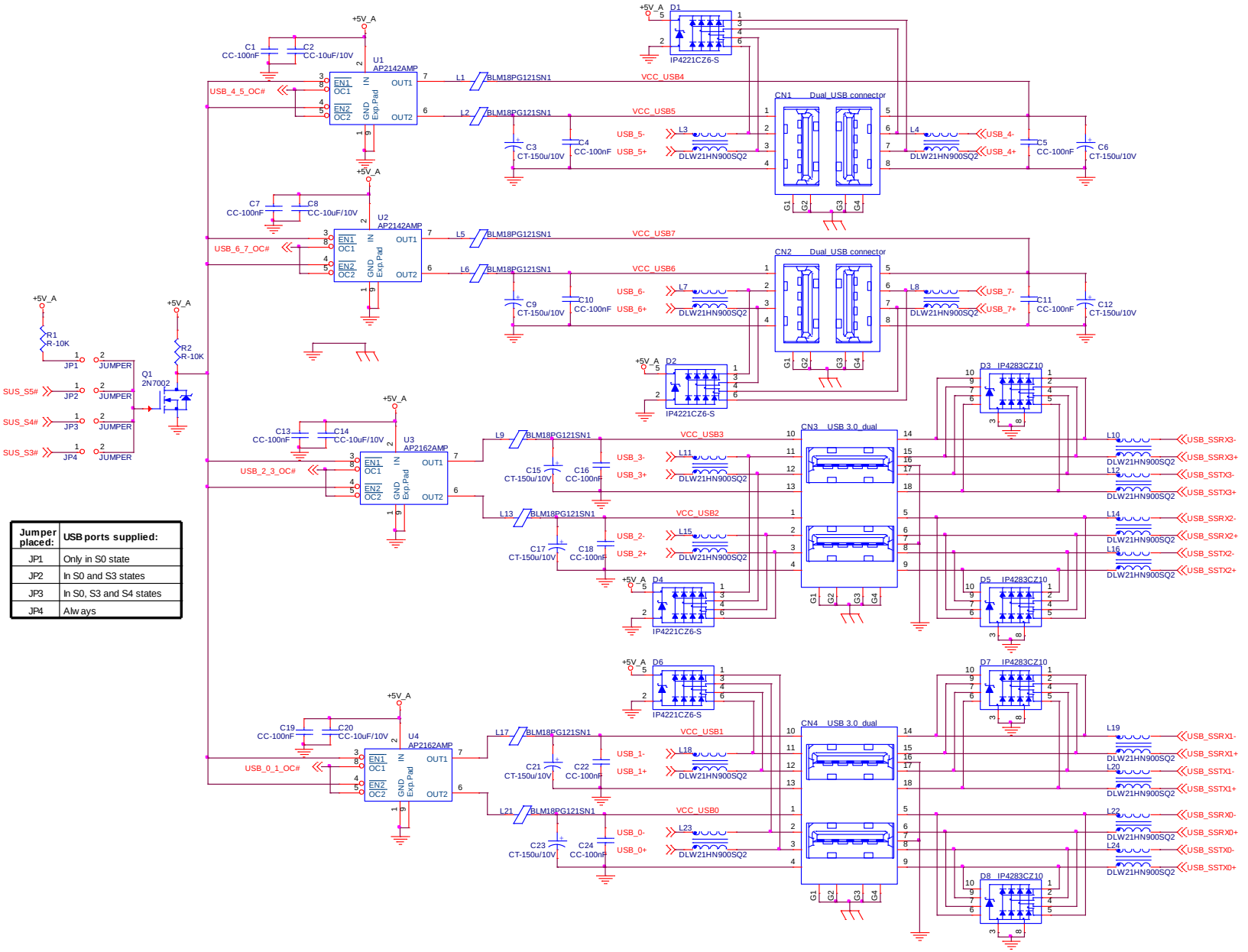
USB0_HOST_PRSNT: USB detection signal of USB host on USB0 when module is configured to be a client. Active High Input signal, electrical level +3.3V_ALW with 100kΩ pull-down resistor.

100nF AC series decoupling capacitors are placed on each transmitting line of USB Super speed differential pairs.

Please notice that for correct management of Overcurrent signals, power distribution switches are needed on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

The schematics in the following page show an example of implementation on the Carrier Board. In there, USB ports #4, #5, #6 and #7 are carried out to standard USB 2.0 Type A receptacles, while USB 2.0 port #0, #1, #2 and #3 along with the corresponding Superspeed USB ports, are carried to standard USB 3.0 Type A receptacles. Always remember that, for correct implementation of USB 3.0 connections, any Superspeed port must be paired with corresponding number of USB 2.0 port (i.e. USB 2.0 port#0 must be paired with USB 3.0 port #0 and so on).



Jumper placed:	USB ports supplied:
JP1	Only in S0 state
JP2	In S0 and S3 states
JP3	In S0, S3 and S4 states
JP4	Always

3.2.5.6 LVDS Flat Panel signals

The Intel® family of SOCs formerly coded as Apollo Lake offers offers three Digital Display Interfaces, of which the first is able to support natively embedded Display Port (eDP). Conversely, the LVDS interface, which is frequently used in many application fields, is not directly supported by these CPUs.

For this reason, considering that LVDS interface can be multiplexed on the same pin with the eDP interface, on COMe-C24-CT6 module can be implemented an eDP to LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hz (dual channel mode).

> **!** Please remember that LVDS interface is not native for the Intel® family of SOCs formerly coded as Apollo Lake, it is derived from an optional eDP-to-LVDS bridge. Depending on the factory option purchased, on the same pins it is possible to have available LVDS first channel or eDP interface.
>
> Please take care of specifying if LVDS interface or eDP is needed, before placing an order of COMe-C24-CT6 module.

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Channel #A differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Channel #A differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Channel #A differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Channel #A differential data pair #3.

LVDS_A_CK+/LVDS_A_CK-: LVDS Channel #A differential clock.

LVDS_B0+/LVDS_B0-: LVDS Channel #B differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Channel #B differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Channel #B differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Channel #B differential data pair #3.

LVDS_B_CK+/LVDS_B_CK-: LVDS Channel #B differential Clock

LVDS_VDD_EN: +3.3V_RUN electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display.

LVDS_BKLT_EN: +3.3V_RUN electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display.

LVDS_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

LVDS_I2C_DAT: DisplayID DDC Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN.

LVDS_I2C_CK: DisplayID DDC Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN.

Please be aware that External EDID through LVDS_I2C-xxx signals is actually not supported by COMe-C24-CT6 module

3.2.5.7 Embedded Display Port (eDP) signals

As described in the previous paragraph, the Intel® family of SOCs formerly coded as Apollo Lake offers a native 4-lanes embedded Display Port (eDP) interface.

As a factory option, the module can be configured with this eDP interface available on COM Express connector AB, which allows supporting displays with a resolution up 4096x2304 @ 60Hz.

Here following the signals related to eDP management:

eDP_TX0+/eDP_TX0-: eDP channel differential data pair #0.

eDP_TX1+/eDP_TX1-: eDP channel differential data pair #1.

eDP_TX2+/eDP_TX2-: eDP channel differential data pair #2.

eDP_TX3+/eDP_TX3-: eDP channel differential data pair #3.

eDP_AUX+/eDP_AUX-: eDP channel differential auxiliary channel.

eDP_HPD: eDP channel Hot Plug Detect. Active High Signal, +3.3V_RUN electrical level input with 100kΩ pull-down resistor.

eDP_VDD_EN: +3.3V_RUN electrical level output, Panel Power Enable signal. It can be used to turn On/Off the connected display.

eDP_BKLT_EN: +3.3V_RUN electrical level output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected display.

eDP_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

3.2.5.8 Analog VGA interface

The Intel® family of SOCs formerly coded as Apollo Lake doesn't offer any analog display interface, which could be used for the connection of older VGA/CRT displays.

As a factory option, however, it is possible to purchase COMe-C24-CT6 modules equipped with an eDP to VGA bridge (NXP PTN3356BS), which allow the implementation of a VGA interface with a maximum supported resolution of 2048x1536 @ 50Hz (reduced blanking). Modules equipped with the eDP-to-VGA bridge can also mount the eDP-to-LVDS bridge, since the two bridges use different eDP lanes.

> **!** Please remember that the VGA interface is not native for the Intel® Apollo Lake family of CPUs, it is derived from an optional eDP-to-VGA bridge. Furthermore, DDI Port #2 Aux channel is required to drive the VGA bridge. This means that, on modules equipped with the eDP-to-VGA bridge, the DDI interface #3 can be used exclusively in HDMI/DVI mode, not in DP++ mode
>
> Please take care of specifying if VGA interface is needed, before placing an order of COMe-C24-CT6 module.

Signals dedicated to VGA interface are the following:

VGA_RED: Red Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_GRN: Green Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_BLU: Blue Signal video output. A 150Ω pull-down resistor is placed on the line.

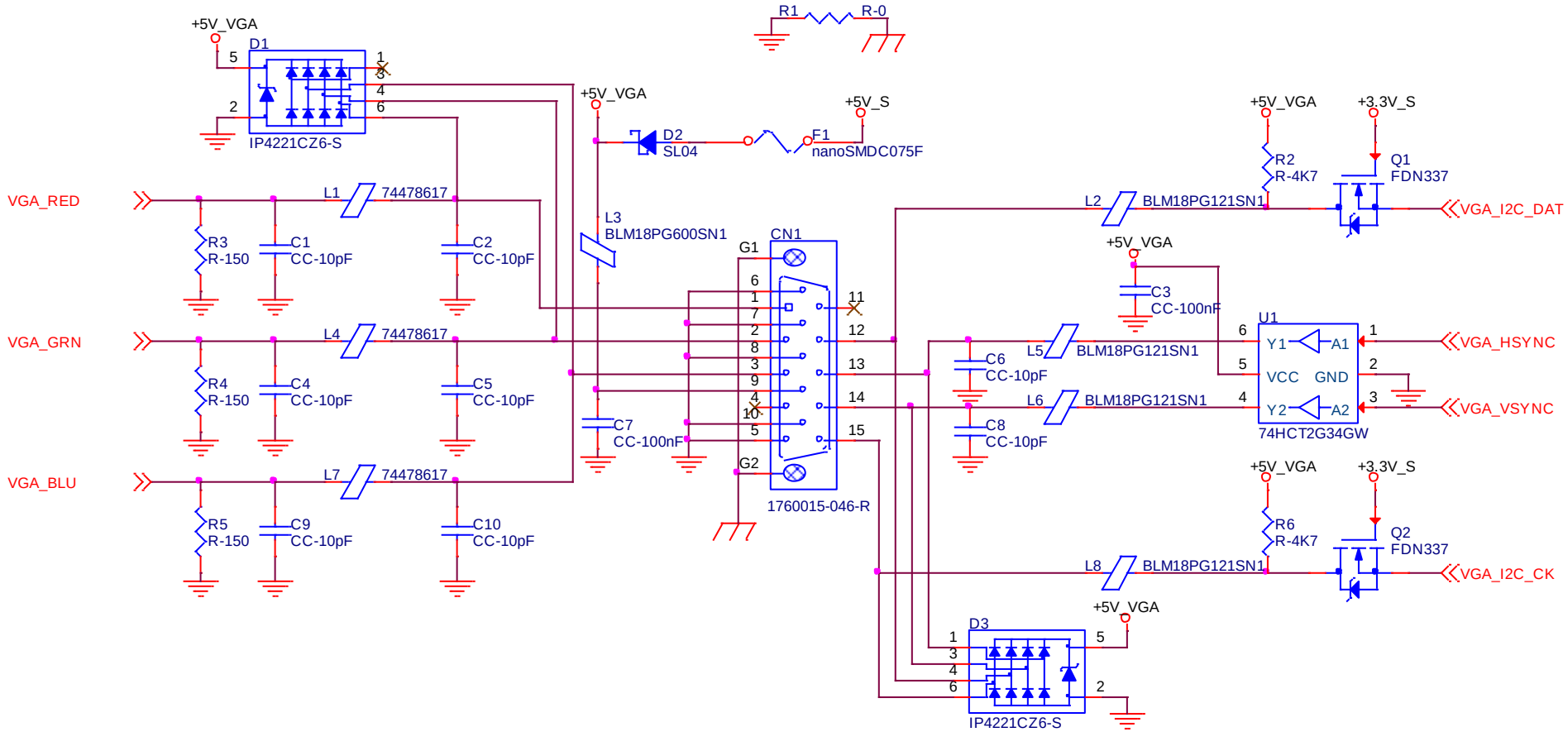
VGA_HSYNC: Horizontal Synchronization output signal.

VGA_VSYNC: Vertical Synchronization output signal.

VGA_I2C_CK: DDC Clock line for VGA displays detection. Output signal, electrical level +3.3V_RUN with 2K2Ω pull-up resistor.

VGA_I2C_DAT: DDC Clock line for VGA displays detection. Bidirectional signal, electrical level +3.3V_RUN with 2K2Ω pull-up resistor.

Please be aware that for the connection to external VGA displays, on the carrier board it is necessary to provide for filters and ESD protection like in the following example schematics.



3.2.5.9 Digital Display interfaces

The Intel® HD Graphics 500 controller, embedded inside the Intel® Apollo Lake family of CPUs, offers two Digital Display interfaces, which can be used for the implementation, on the carrier board, of HDMI/DVI or Multimode Display Port interfaces.

Switching between HDMI/DVI (or, more correctly, TMDS) and Display Port is dynamic, i.e. the interfaces coming out from COM Express® module can be used to implement a multimode Display Port interface (and in this way only AC coupling capacitors are needed on the carrier board) or a HDMI/DVI interface (an in this case TMDS level shifters are needed).

This is reached by multiplexing DP/HDMI interfaces on the same pins.

Depending by the interface chosen, therefore, on COM Express connector CD there will be available the following signals:

Digital Display Interfaces - Pin multiplexing					
		Multimode Display Port mode		TMDS (HDMI/DVI) mode	
Pin nr.	Pin name	Signal	Description	Signal	Description
D26	DDI1_PAIR0+	DP1_LANE0+	DP1 Differential pair #0 non-inverting line	TMDS1_DATA2+	TMDS1 Differential pair #2 non-inverting line
D27	DDI1_PAIR0-	DP1_LANE0-	DP1 Differential pair #0 inverting line	TMDS1_DATA2-	TMDS1 Differential pair #2 inverting line
D29	DDI1_PAIR1+	DP1_LANE1+	DP1 Differential pair #1 non-inverting line	TMDS1_DATA1+	TMDS1 Differential pair #1 non-inverting line
D30	DDI1_PAIR1-	DP1_LANE1-	DP1 Differential pair #1 inverting line	TMDS1_DATA1-	TMDS1 Differential pair #1 inverting line
D32	DDI1_PAIR2+	DP1_LANE2+	DP1 Differential pair #2 non-inverting line	TMDS1_DATA0+	TMDS1 Differential pair #0 non-inverting line
D33	DDI1_PAIR2-	DP1_LANE2-	DP1 Differential pair #2 inverting line	TMDS1_DATA0-	TMDS1 Differential pair #0 inverting line
D36	DDI1_PAIR3+	DP1_LANE3+	DP1 Differential pair #3 non-inverting line	TMDS1_CLK+	TMDS1 Differential clock non-inverting line
D37	DDI1_PAIR3-	DP1_LANE3-	DP1 Differential pair #3 inverting line	TMDS1_CLK-	TMDS1 Differential clock inverting line
C24	DDI1_HPD	DP1_HPD	DP1 Hot Plug Detect signal	HDMI1_HPD	HDMI #1 Hot Plug Detect signal
D15	DDI1_CTRLCLK_AUX+	DP1_AUX+	DP1 Auxiliary channel non-inverting line	HDMI1_CTRLCLK	DDC Clock line for HDMI panel #1.
D16	DDI1_CTRLDATA_AUX-	DP1_AUX-	DP1 Auxiliary channel inverting line	HDMI1_CTRLDATA	DDC Data line for HDMI panel #1.
D34	DDI1_DDC_AUX_SEL	DDI#1 DP or TMDS interface selector: pull this signal low or leave it floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface			
D39	DDI2_PAIR0+	DP2_LANE0+	DP2 Differential pair #0 non-inverting line	TMDS2_DATA2+	TMDS2 Differential pair #2 non-inverting line
D40	DDI2_PAIR0-	DP2_LANE0-	DP2 Differential pair #0 inverting line	TMDS2_DATA2-	TMDS2 Differential pair #2 inverting line
D42	DDI2_PAIR1+	DP2_LANE1+	DP2 Differential pair #1 non-inverting line	TMDS2_DATA1+	TMDS2 Differential pair #1 non-inverting line
D43	DDI2_PAIR1-	DP2_LANE1-	DP2 Differential pair #1 inverting line	TMDS2_DATA1-	TMDS2 Differential pair #1 inverting line
D46	DDI2_PAIR2+	DP2_LANE2+	DP2 Differential pair #2 non-inverting line	TMDS2_DATA0+	TMDS2 Differential pair #0 non-inverting line

D47	DDI2_PAIR2-	DP2_LANE2-	DP2 Differential pair #2 inverting line	TMDS2_DATA0-	TMDS2 Differential pair #0 inverting line
D49	DDI2_PAIR3+	DP2_LANE3+	DP2 Differential pair #3 non-inverting line	TMDS2_CLK+	TMDS2 Differential clock non-inverting line
D50	DDI2_PAIR3-	DP2_LANE3-	DP2 Differential pair #3 inverting line	TMDS2_CLK-	TMDS2 Differential clock inverting line
D44	DDI2_HPD	DP2_HPD	DP2 Hot Plug Detect signal	HDMI2_HPD	HDMI #2 Hot Plug Detect signal
C32	DDI2_CTRLCLK_AUX+	DP2_AUX+	DP2 Auxiliary channel non-inverting line	HDMI2_CTRLCLK	DDC Clock line for HDMI panel #2.
C33	DDI2_CTRLDATA_AUX-	DP2_AUX-	DP2 Auxiliary channel inverting line	HDMI2_CTRLDATA	DDC Data line for HDMI panel #2.
C34	DDI2_DDC_AUX_SEL	DDI#2 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface			
C44	DDI3_HPD	Tied to GND through a 1MΩ pull-down resistor			
C38	DDI3_DDC_AUX_SEL	Tied to GND through a 1MΩ pull-down resistor			

All Hot Plug Detect Input signals (valid both for DP++ and TMDS interface) are +3.3V_RUN electrical level signal, active high with 100KΩ pull-down resistors.

All HDMI Control /DP AUX signals (DDIx_CTRLCK_AUX+ and DDIx_CTRLDATA_AUX-) are bidirectional signal, electrical level +3.3V_RUN with a 100kΩ pull-up (on Data) / pull-down (on clock) resistor

Please be aware that for correct implementation of HDMI/DVI interfaces, it is necessary to implement, on the Carrier board, voltage level shifter for TMDS differential pairs, for Control data/Clock signals and for Hot Plug Detect signal.

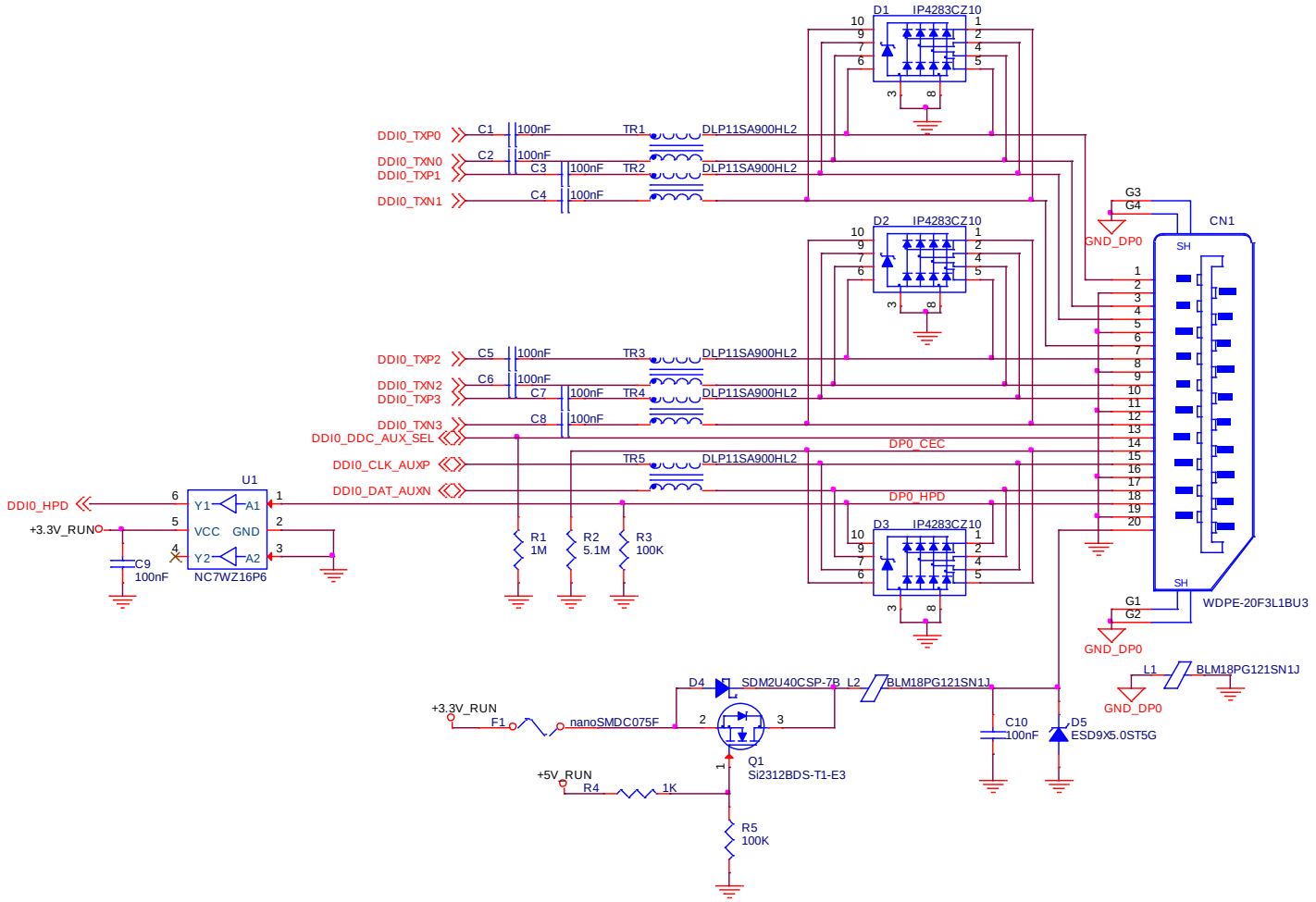
Voltage clamping diodes are also highly recommended on all signal lines for ESD suppression.

!

Please remember that modules configured with the VGA video output will use the DDI Port #2 to drive the DP-to-VGA bridge. This means that on these modules, the DDI interface #2 will not be externally available.

Please take care of specifying if VGA interface is needed, before placing an order of COMe-C24-CT6 module.

Here following an example of implementation of multimode Display Port on the carrier board. In this example, are used signals related to Digital Display interface #1, but any DDI interface can be used.



3.2.5.10 LPC interface signals

According to COM Express® specifications rel. 3.0, on the on COM Express connector AB there are 8 pins that can be used for implementation of Low Pin Count (LPC) Bus or enhanced SPI (eSPI) interfaces, which are two multiplexed interfaces made available by the PCH. However, since LPC bus is needed for the management of the Embedded microcontroller, then COMe-C24-CT6 module makes available only the LPC interface.

The following signals are available:

LPC_AD[0÷3]: LPC address, command and data bus, bidirectional signal, +3.3V_RUN electrical level 47kΩ pull-up resistors.

LPC_CLK: LPC Clock Output line, +3.3V_RUN electrical level. Since only a clock line is available, if more LPC devices are available on the carrier board, then it is necessary to provide for a zero-delay clock buffer to connect all clock lines to the single clock output of COM Express module.

LPC_FRAME#: LPC Frame indicator, active low output line, +3.3V_RUN electrical level. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

LPC_SERIRQ: LPC Serialised IRQ request, bidirectional line, +3.3V_RUN electrical level with 47kΩ pull-up resistor. This signal is used only by peripherals requiring Interrupt support.

LPC_DRQ[0÷1]#: LPC Serial DMA Request, +3.3V_RUN electrical level. These signals only have a 100kΩ pull-up resistor on module, internally they are not used by the chipset nor by the Embedded Controller.

ESPI_EN#: this input signal should be used by the carrier board to request eSPI interface configuration, which is, however, not supported by the module. Therefore, driving low this signal would have no effect. Electrical level +3.3V_RUN with 100kΩ pull-up resistor.

3.2.5.11 SPI interface signals

The Intel® Apollo Lake family of processors offer also one dedicated controller for Serial Peripheral Interface (SPI), which can be used for connection of Serial Flash devices. Please be aware that this interface can be used exclusively to support platform firmware (BIOS).

Signals involved with SPI management are the following:

SPI_CS#: SPI Chip select, active low output signal, +1.8V_ALW electrical level with 10kΩ pull-up resistor.

SPI_MISO: SPI Master In Slave Out, Input to COM Express® module from SPI devices embedded on the Carrier Board. Electrical level +1.8V_ALW.

SPI_MOSI: SPI Master Out Slave In, Output from COM Express® module to SPI devices embedded on the Carrier Board. Electrical level +1.8V_ALW

SPI_CLK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +1.8V_ALW. Supported clock frequencies are 20, 33 and 50 MHz.

SPI_POWER: +1.8V_ALW Power Supply Output for carrier board's SPI devices.

BIOS_DIS[0÷1]#: BIOS Disable strap signals. These two signals are inputs of the COM Express® Module, that on the carrier board can be left floating or pulled down in order to select which SPI Flash device has to be used for module's boot. Please refer to table 4.13 of COM Express® Module Base Specifications rel. 3.0 for the meaning of possible configurations of these two signals.

3.2.5.12 UART interface signals

According to COM Express® Rel. 3.0 specifications, since the COMe-C24-CT6 is a Type 6 module, it can offer two UART interfaces, which are managed by the embedded controller or directly from Intel® Apollo Lake family of CPUs.

Here following the signals related to UART interface:

SER0_TX: UART Interface #0, Serial data Transmit (output) line, 3.3V_RUN electrical level.

SER0_RX: UART Interface #0, Serial data Receive (input) line, 3.3V_RUN electrical level.

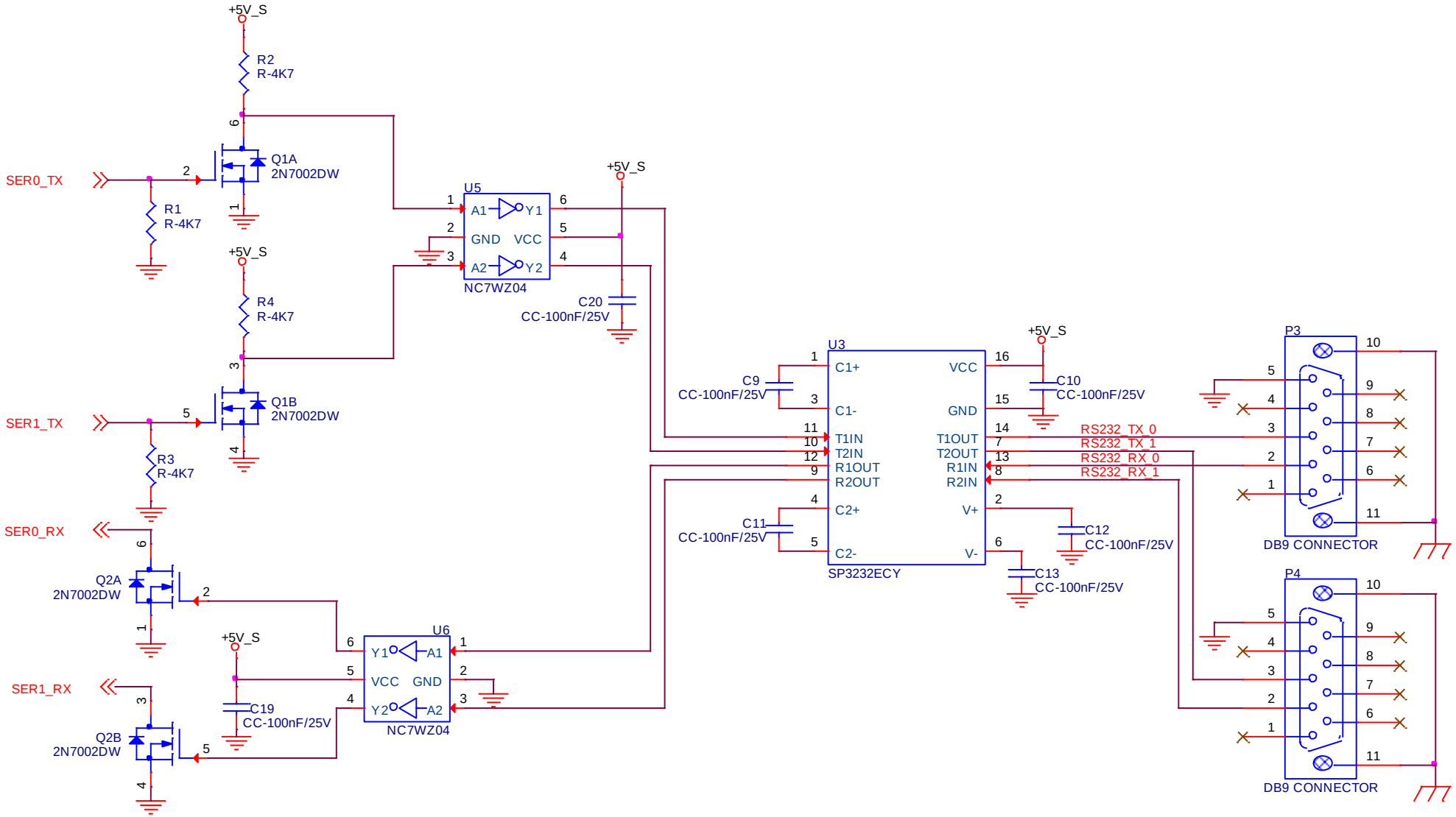
SER1_TX: UART Interface #1, Serial data Transmit (output) line, 3.3V_RUN electrical level.

SER1_RX: UART Interface #1, Serial data Receive (input) line, 3.3V_RUN electrical level.

In COM Express® specifications prior to Rel. 2.0, the pins dedicated to these two UART interfaces were dedicated to +12V_{IN} power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then Schottky-diodes have been added on UART interfaces' TX and RX lines so that they are +12V Tolerant.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it is not explicitly necessary to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The schematic on the next page shows an example of implementation of RS-232 transceiver for the Carrier board.


+5V_S
R2
R-4K7
Q1A
2N7002DW
SER0_TX
R1
R-4K7
U5
A1
Y1
GND
VCC
A2
Y2
NC7WZ04
C20
CC-100nF/25V
R4
R-4K7
Q1B
2N7002DW
SER1_TX
R3
R-4K7
SER0_RX
Q2A
2N7002DW
U6
C19
CC-100nF/25V
SER1_RX
Q2B
2N7002DW
U3
C1+
C1-
T1IN
T2IN
R1OUT
R2OUT
C2+
C2-
VCC
GND
T1OUT
T2OUT
R1IN
R2IN
V+
V-
SP3232ECY
C9
CC-100nF/25V
C10
CC-100nF/25V
C11
CC-100nF/25V
C12
CC-100nF/25V
C13
CC-100nF/25V
RS232_TX_0
RS232_TX_1
RS232_RX_0
RS232_RX_1
P3
P4
DB9 CONNECTOR
DB9 CONNECTOR

3.2.5.13 I2C interface signals

This interface is managed by the embedded microcontroller.

Signals involved are the following:

I2C_CK: general purpose I2C Bus clock line. Output signal, electrical level +3.3V_ALW with a 2K2Ω pull-up resistor.

I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3.3V_ALW with a 2K2Ω pull-up resistor.

3.2.5.14 Miscellaneous signals

Here following, a list of COM Express® compliant signals that complete the features of COMe-C24-CT6 module.

SPKR: Speaker output, +3.3V_RUN voltage signal.

WDT: Watchdog event indicator Output. It is an active high signal, +3.3V_ALW voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW. This signal is managed by the module's embedded microcontroller.

FAN_PWMOUT*: PWM output for FAN speed management, +3.3V_RUN voltage signal. It is managed by the module's embedded microcontroller.

FAN_TACHIN*: External FAN Tachometer Input. +3.3V_RUN voltage signal, directly managed by the module's embedded microcontroller.

TPM_PP: Trusted Platform Module (TPM) Physical Presence Input, +3.3V_ALW voltage signal with 100kΩ pull-down resistor, managed by the optional TPM device on-module.

THRM#: Thermal Alarm Input. Active Low +3.3V_RUN voltage signal with 10kΩ pull-up resistor, directly managed by the module's embedded microcontroller. This input gives the possibility, to carrier board's hardware, to indicate to the main module an overheating situation, so that the CPU can begin thermal throttling.

THRMTRIP#: Active Low +3.3V_ALW voltage output signal. This signal is used to communicate to the carrier board's devices that, due to excessive overheating, the CPU began the shutdown in order to prevent physical damages.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to FAN management were dedicated to $+12V_{IN}$ power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then protection circuitry has been added on FAN_PWM_OUT and FAN_TACHOIN lines so that they are +12V Tolerant.

3.2.5.15 Power Management signals

According to COM Express® specifications, on the connector AB there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWRBTN#: Power Button Input, active low, +3.3V_ALW buffered voltage signal with 47kΩ pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

SYS_RESET#: Reset Button Input, active low, +3.3V_ALW buffered voltage signal with 47kΩ pull-up resistor. This signal can be connected to a momentary push-

button: a pulse to GND of this signal will reset the COMe-C24-CT6 module.

CB_RESET#: System Reset Output, active low, +3.3V_ALW voltage buffered signal. It can be used directly to drive externally a single RESET Signal. In case it is necessary to supply Reset signal to multiple devices, a buffer on the carrier board is recommended.

PWR_OK: Power Good Input, +3.3V_RUN active high signal. It must be driven by the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

SUS_STAT#: Suspend status output, active low +3.3V_ALW electrical voltage signal with 10k pull-up resistor. This output can be used to report to the devices on the carrier board that the module is going to enter in one of possible ACPI low-power states.

SUS_S3#: S3 status output, active low +3.3V_ALW electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S5#: S5 status output, active low +3.3V_ALW electrical voltage signal. This signal is used, on the carrier board, to shut off the power supply to all the devices that must become inactive only during S5 (Soft Off) power state. SUS_S4# is connected internally to this signal.

WAKE0#: PCI Express Wake Input, active low +3.3V_ALW electrical voltage signal with 10kΩ pull-up resistor. This signal can be driven low, on the carrier board, to report that a Wake-up event related to PCI Express has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

WAKE1#: General Purpose Wake Input, active low +3.3V_ALW electrical voltage signal with 2k2Ω pull-up resistor. It can be driven low, on the carrier board, to report that a general Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used. While WAKE0# signal is managed directly by the Soc's embedded PCH, WAKE1#signal is managed by the Embedded microcontroller.

BATLOW#: Battery Low Input, active low, +3.3V_ALW voltage signal with 10kΩ pull-up resistor. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. It can be left unconnected if not used.

LID# *: LID button Input, active low +3.3V_ALW electrical level signal, with 47kΩ pull-up resistor. This signal can be driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

SLEEP# *: Sleep button Input, active low +3.3V_ALW electrical level signal, with 47kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to LID# and SLEEP# inputs were dedicated to +12V_{IN} power rail. Protection circuitry has been added on LID# and SLEEP# so that they are +12V Tolerant. This has been made in order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6.

3.2.5.16 SMBus signals

This interface is managed by the Soc's embedded PCH.

Signals involved are the following:

SMB_CK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_ALW with a 1kΩ pull-up resistor.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_ALW with a 1kΩ pull-up resistor.

SMB_ALERT#: SM Bus Alert line for System Management. Input signal, electrical level +3.3V_ALW with a 1kΩ pull-up resistor. Any device place on the SM Bus can drive this signal low to signal an event on the bus itself.

3.2.5.17 GPIO interface signals

According to COM Express® specifications rel. 3.0, there are 8 pins that could be used as General Purpose Inputs and Outputs, managed by embedded microcontroller

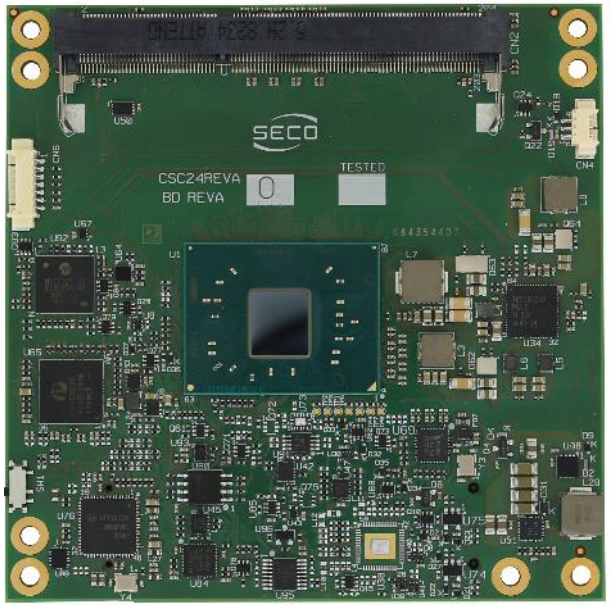
Signals involved are the following:

GPI[0÷3]: General Purpose Inputs, electrical level +3.3V_ALW with 10kΩ pull-up resistor each.

GPO[0÷3]: General Purpose Outputs, electrical level +3.3V_ALW with 10kΩ pull-down resistor each.

Chapter 4.
BIOS SETUP

- Aptio setup Utility
- Main setup menu
- Advanced menu
- Chipset menu
- Security menu
- Boot menu
- Save & Exit menu



4.1 Aptio setup Utility

Basic setup of the board can be done using American Megatrends, Inc. “Aptio Setup Utility”, that is stored inside an onboard SPI Serial Flash.

It is possible to access to Aptio Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select “SCU” icon.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
+ / -	+ and - keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows displaying the General Help screen.
<F2>	Previous Values
<F3>	<F3> key allows loading Optimised Defaults for the board. After pressing <F3> BIOS Setup utility will request for a confirmation, before loading such default values. By pressing <ESC> key, this function will be aborted
<F4>	<F4> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows discarding any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow displaying the setup sub-screens.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

4.2.1 System Date / System Time

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Trusted Computing	See submenu	Trusted Computing Settings
ACPI Settings	See submenu	System ACPI parameters
S5 RTC Wake Settings	See submenu	Enable System to wake from S5 using RTC alarm
CPU Configuration	See submenu	CPU Configuration Parameters
AMI Graphic Output Protocol Policy	See submenu	User Selected Monitor Output by Graphic Output protocol
PCI Subsystem Settings	See submenu	PCI Subsystem Settings
Network Stack Configuration	See submenu	Network Stack Settings
CSM Configuration	See submenu	Compatibility Support Module (CSM) Configuration: Enable/Disable, Option ROM execution Settings, etc...
NVMe Configuration	See submenu	NVMe Device Options Settings
SDIO Configuration	See submenu	SDIO
USB Configuration	See submenu	USB Configuration Parameters
Platform Trust Technology	See submenu	Platform Trust Technology
Main Thermal Configuration	See submenu	Main thermal Configuration Parameters
LVDS Configuration	See submenu	LVDS Configuration Parameters
SMBIOS Information	See submenu	SMBIOS Information
Embedded Controller	See submenu	Embedded Controller Parameters

4.3.1 Trusted computing submenu

Menu Item	Options	Description
Security Device Support	Enabled / Disabled	Enables or Disables BIOS support for security device. OS will not show the Security Device. TCG EFI protocol and INT1A interface will not be available. When enabled all the following items will be available.
SHA-1 PCR Bank	Enabled / Disabled	Enables or Disables SHA-1 PCR Bank
SHA256 PCR Bank	Enabled / Disabled	Enables or Disables SHA256 PCR Bank
Pending Operation	None / TPM Clear	Schedule an Operation for the Security Device. NTE: your Computer will reboot during restart in order to change State of Security Device.
Platform Hierarchy	Enabled / Disabled	Enables or Disabled the Platform Hierarchy
Storage Hierarchy	Enabled / Disabled	Enables or Disabled the Storage Hierarchy
Endorsement Hierarchy	Enabled / Disabled	Enables or Disabled the Endorsement Hierarchy
TPM2.0 UEFI Spec Version	TCG_1_2 TCG_2	Select the TCG Spec Version support. TCG_1_2 is the compatible mode for Windows 8 / Windows 10. TCG 2 supports the new TCG2 protocol and event format for Windows 10 or later.
Physical Presence Spec Version	1.2 / 1.3	Select to tell OS to support PPI Spec Version 1.2 or 1.3. Please note that some HCK tests might not support 1.3
Device Select	Auto TPM 1.2 TPM 2.0	TPM 1.2 will restrict the support to TPM 1.2 devices only, TPM 2.0 will restrict the support to TPM 2.0 devices only, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

4.3.2 ACPI Settings submenu

Menu Item	Options	Description
Enable ACPI Auto Configuration	Disabled / Enabled	Enables or Disables BIOS ACPI Auto Configuration. The following menu items will appear only when this menu item is Disabled
Enable Hibernation	Disabled / Enabled	Enables or disables system ability to Hybernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled S3 (Suspend to RAM)	Select the highest ACPI Sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy resources	Disabled / Enabled	Enables or Disables Lock of Legacy resources

4.3.3 S5 RTC Wake Settings submenu

Menu Item	Options	Description
Wake system from S5	Disabled By Every Day By Day of Month	Enables or disables System Wake on Alarm event. The following menu items will appear only when this voice is not set to Disabled
Wake up hour	0..23	Sets the wake up hour in 0..23 format (i.e.,3 means 3am, 15 means 3pm)
Wake up minute	0..59	Sets the wake up minute
Wake up second	0..59	Sets the wake up second
Day of Month	1..31	This item is available only when “Wake system from S5” is set to “By Day of Month”. Sets the day of month for Wake on Alarm event. Valid range s from 1 to 31, error checking will be done against month/day/year combinations that are not valid.

4.3.4 CPU Configuration submenu

Menu Item	Options	Description
Detailed CPU Information		Shows board's specific SoC information
CPU Power Management	See Submenu (par. 4.3.4.1)	CPU Power Management options
Active Processor Cores	Disabled / Enabled	Number of Cores to enable in each processor package
Core 0 Core 1 Core 2 Core 3	Disabled / Enabled	Core #x Enable / Disable. Only available when “Active Processor Cores” is enabled
Intel Virtualization Technology	Disabled / Enabled	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology
VT-d	Disabled / Enabled	Enables or disables CPU VT-d
Bi-directional PROCHOT	Disabled / Enabled	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor
Thermal Monitor	Disabled / Enabled	Enables or disables the Thermal Monitor
Monitor Mwait	Disabled / Enabled / Auto	Enables or disables Monitor Mwait
P-STATE Coordination	HW_ALL / SW_ALL / SW_ANY	Change P-STATE Coordination type
DTS	Disabled / Enabled	Enables or disables the Digital Thermal Sensor

4.3.4.1 CPU Power Management submenu

Menu Item	Options	Description
EIST	Disabled / Enabled	Enables or disables Intel® SpeedStep
Turbo mode	Disabled / Enabled	Only Available when "EIST" is enabled. Enables or disables the Turbo Mode
Boot Performance mode	Max performance Max battery	Select the performance state that the BIOS will set before OS handoff
Power Limit 1 Enable	Disabled / Enabled	Enables or disables Power Limit 1. When Enabled, the following menu items will appear
Power Limit 1 Clamp Mode	Disabled / Enabled	Only Available when Power Limit 1 is Enabled. Enables or disables the Clamp Mode
Power Limit 1 Power	Auto / 3 / 4 / 5 / 6 / 7 / 8 / 9 / 10	Power Limit 1 in Watts. Auto will program Power Limit 1 based on silicon default support value.
Power Limit 1 Time Windows	Auto / 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8 / 10 / 12 / 14 / 16 / 20 / 24 / 28 / 32 / 40 / 48 / 56 / 64 / 80 / 96 / 112 / 128	Power Limit 1 Time Window Value in Seconds. Auto will program the Power Limit 1 Time Window based on silicon default support value

4.3.5 AMI graphic Output Protocol Policy submenu

Menu Item	Options	Description
Output Select	*List of available / connected module's video interfaces*	User select monitor for graphic console output in the pre-OS phase

4.3.6 PCI Subsystem Settings submenu

Menu Item	Options	Description
Above 4G Decoding	Disabled / Enabled	Globally Enabled or Disabled 64-bitcapable Devices to be decoded in Address Space above 4GB (only if system supports 64-bit PCI Decoding).
BME DMA Mitigation	Disabled / Enabled	Re-enable Bus Master Attribute disabled during PCI enumeration for PCI Bridges after SMM has been locked
Hot-Plug Support	Disabled / Enabled	Globally Enables or Disables Hot-Plug support for the entire System. If System has Hot-Plug capable Slots and this option set to Enabled, it provides a Setup screen for selecting PCI resource padding for Hot-Plug.

4.3.7 Network Stack configuration submenu

Menu Item	Options	Description
Network Stack	Enabled / Disabled	Enables or disables UEFI Network Stack. When enabled, following menu items will appear
Ipv4 PXE Support	Enabled / Disabled	Enables or disables IPV4 PXE Boot Support. If disabled, IPV4 PXE boot option will not be created
Ipv4 HTTP Support	Enabled / Disabled	Enables or disables IPV4 HTTP Boot Support. If disabled, IPV4 HTTP boot option will not be created
Ipv6 PXE Support	Enabled / Disabled	Enables or disables IPV6 PXE Boot Support. If disabled, Ipv6 PXE boot option will not be created
Ipv6 HTTP Support	Enabled / Disabled	Enables or disables IPV6 HTTP Boot Support. If disabled, Ipv6 HTTP boot option will not be created
PXE boot wait time	[0..5]	Wait time to press ESC key to abort the PXE boot
Media detect count	[1..50]	Number of times that the presence of media will be checked

4.3.8 CSM configuration submenu

Menu Item	Options	Description
CSM Support	Enabled / Disabled	Enables or disables the Compatibility Support Module. When enabled, the following menu items will appear
GateA20 Active	Upon Request Always	Upon Request: GateA20 can be disabled using BIOS services, Always: do not allow disabling GateA20; this option is useful when any RT code is executed above 1MB.
INT19 Trap Response	Immediate Postponed	BIOS Reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot
Boot option filter	UEFI and Legacy Legacy only UEFI only	This option controls Legacy / UEFI ROMs priority
Network	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy PXE OpROM
Storage	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Video OpROM

Other PCI devices	Do not launch UEFI Legacy	Determines the OpROM execution policy for devices other than Network, Storage or Video

4.3.9 NVMe configuration submenu

NVMe Device Options Settings, depend on NVMe Devices found in the system.

4.3.10 SDIO configuration submenu

Menu Item	Options	Description
SDIO Access Mode	Auto ADMA SDMA PIO	Auto Option: Access the SD Device in DMA mode if the controller supports it, otherwise in PIO Mode. DMA Option: Access the SD Device in DMA mode ADMA Option: Access the SD Device in Advanced DMA mode PIO Option: Access the SD Device in PIO mode
List of SDIO devices found, if available	Auto Floppy Forced FDD Hard Disk	Mass storage device emulation type. 'Auto' enumerates devices less than 530Mb as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD.

4.3.11 USB configuration submenu

Menu Item	Options	Description
Legacy USB Support	Enabled / Disabled / Auto	Enables Legacy USB Support. AUTO Option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
XHCI hand-off	Enabled/ Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enabled/ Disabled	Enables or disables USB Mass Storage Driver Support
USB Transfer time-out	1 sec / 5 sec / 10 sec / 20 sec	Sets the time-out value for Control, Bulk and Interrupt transfers
Device reset time-out	10 sec / 20 sec / 30 sec / 40 sec	USB mass storage device Start Unit command time-out
Device power-up delay	Auto / Manual	Sets the maximum time that the device will take before it properly reports itself to the Host controller. 'Auto' uses the default vale (for a Root port it is 100ms, for a Hub port the delay is taken from the Hub descriptor).
Device power-up delay in seconds	[1..40]	When "Device power-up delay" is set to manual. Delay range in seconds, in increments of one second.

4.3.12 Platform Trust technology submenu

Menu Item	Options	Description
fTPM	Enabled / Disabled	Enable/Disable fTPM

4.3.13 Main Thermal Configuration submenu

Menu Item	Options	Description
Critical Temperature (°C)	80 .. 110	Above this threshold, an ACPI aware OS will perform a critical shut-down. Allowed range is from 80 to 110, where 110 means disabled.
Passive Cooling Temperature (°C)	60 .. 105	This value controls the temperature of the ACPI Passive Trip Point - the point at which the OS will begin lowering the CPU speed. Allowed range is from 60 to 105, where values above Critical Temperature mean Disabled.
TC1	1 .. 16	Thermal Constant 1: part of the ACPI Passive Cooling Formula
TC2	1 .. 16	Thermal Constant 1: part of the ACPI Passive Cooling Formula
TSP (seconds)	2 .. 32	Period of temperature sampling when Passive Cooling

4.3.14 LVDS Configuration submenu

Menu Item	Options	Description
LVDS interface	Enabled / Disabled	Enables or Disables the LVDS interface. When enabled all the following parameters will appear
Edid Mode	External / Default / Custom	Select the source (EDID, Extended Display Identification Data) to be used for the internal flat panel. Depending on the setting chosen, only some of the following option or none will appear.
EDID	640x480 / 800x480 / 800x600 / 1024x600 / 1024x768 / 1280x720 / 1280x800 / 1280x1024 / 1366x768 / 1400x900 / 1600x900 / 1680x1050 / 1920x1080	Only available when Edid Mode is set to “default”. Select a software resolution (EDID settings) to be used for the internal flat panel.
Color Mode	VESA 24bpp / JEIDA 24bpp / 18 bpp	Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.
Interface	Single Channel / Dual Channel	Allows configuration of LVDS interface in Single or Dual channel mode
DE Polarity	Active High Active Low	Data Enable Polarity

V-Sync Polarity	Negative / Positive	Vertical Sync Signal Polarity: Default is Negative (Active Low)
H-Sync Polarity	Negative / Positive	Horizontal Sync Signal Polarity: Default is Negative (Active Low)
LVDS Advanced Options	See Submenu (par. 4.3.14.1)	LVDS Advanced Options Configurations
Save to EEPROM	Enabled / Disabled	Save current LVDS configuration to module EEPROM

4.3.14.1 LVDS Advanced options submenu

Menu Item	Options	Description
Spreading Depth	No Spreading / 0.5% / 1.0% / 1.5% / 2.0% / 2.5%	Sets spread-spectrum bandwidth of LVDS clock frequency for EMI reduction
Output Swing	150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV / 450 mV	Sets the LVDS differential output swing level
T3 Timing	0 ÷ 255	Minimum T3 timing of panel power sequence to enforce (expressed in units of 50ms)
T4 Timing	0 ÷ 255	Minimum T4 timing of panel power sequence to enforce (expressed in units of 50ms)
T12 Timing	0 ÷ 255	Minimum T12 timing of panel power sequence to enforce (expressed in units of 50ms)
T2 Delay	Enabled / Disabled	When Enabled, T2 is delayed by 20ms ± 50%
T5 Delay	Enabled / Disabled	When Enabled, T5 is delayed by 20ms ± 50%
P/N Pairs Swapping	Enabled / Disabled	Enable or disable LVDS Differential pairs swapping (Positive ⇔ Negative)
Pairs Order Swapping	Enabled / Disabled	Enable or disable channel differential pairs order swapping (A ⇔ D, B ⇔ CLK, C ⇔ C)
Bus Swapping	Enabled / Disabled	Enable or disable Bus swapping (Odd ⇔ Even)
Firmware PLL	0: +/- 1.56% 1: +/- 3.12% 2: +/- 6.25% 3: +/- 12.5% 4: +/- 25% 5: +/- 50% 6: +/- 100%	Firmware PLL range

4.3.15 SMBIOS Information

Display only screen, shows information about the module and the Carrier board.

4.3.16 Embedded Controller submenu

Menu Item	Options	Description
Power Fail resume Type	Always ON Always OFF Last State	Specifies what must happen when power is re-applied after a power failure (G3 state). Always ON: the System will boot directly as soon as the power is applied. Always OFF: the system remains in power off State until power button is pressed
No C-MOS battery handling	Disabled / Enabled	This option is enabled when "Power Fail resume Type" is set to Always OFF or Last State. In system with no C-MOS battery, the chipset always powers on after a power failure: Always OFF Resume Type or Last State when Last State was OFF will therefore require an immediate shutdown
LID_BTN# Configuration	Force Open Force Closed Normal Polarity Inverted Polarity	Configures the LID_BTN# signal as always open or closed, no matter the pin level, or configures the pin polarity: High = Open (Normal), Low = Open (Inverted)
LID_BTN# Wake Configuration	No Wake Only From S3 Wake From S3/S4/S5	Configures LID_BTN# wake capability (when not forced to Open or Closed). According to the pin configuration, when the LID is open it can cause a system wake from a sleep state.
SMB_ALERT# wake	Disabled / Enabled	Enables or disables SMBUS Alert Wake from Suspend State.
OUT 80 serial redirection port	None 1 2 1+2	Select on which Embedded Controller UART(s) to redirect OUT 80 (Post Codes)
Hardware Monitor		By selecting this item, an information screen with System parameters will appear
Reset Causes Handling		By selecting this item, an information screen with the handling of latest resets causes will appear
Super IO Configuration	See Submenu (par. 4.3.16.1)	Sets the parameters for Serial Ports
Internal FAN Settings	See Submenu (par. 4.3.16.2)	Sets the parameters for internal (i.e. on-module) FAN
External FAN/PWM Settings	See Submenu (par. 4.3.16.3)	Sets the parameters for external (i.e. on-carrier FAN
Watchdog configuration	See Submenu (par. 4.3.16.4)	Configures the Embedded Controller's Watchdog Timer
GPIO Configurations	See Submenu (par. 4.3.16.5)	Sets the parameters for GPIOs

4.3.16.1 Super IO Configuration submenu

Menu Item	Options	Description
Serial Port 1	Enabled / Disabled	Enables or Disables Serial Port 1
Address	0x3F8 0x3E8 0x2F0 0x2E8 0x2E0 0x2A8 0x2A0 0x288 0x280	Serial Port IO Base Address
IRQ	3 / 4 / 5 / 6 / 7 / 10 / 11 / 14 / 15	Serial Port IRQ
Serial Port 2	Enabled / Disabled	Enables or Disables Serial Port 2
Address	0x3F8 0x3E8 0x2F0 0x2E8 0x2E0 0x2A8 0x2A0 0x288 0x280	Serial Port IO Base Address
IRQ	3 / 4 / 5 / 6 / 7 / 10 / 11 / 14 / 15	Serial Port IRQ

4.3.16.2 Internal FAN Settings submenu

Menu Item	Options	Description
Enhanced 3 wire RPM measurement	Enabled / Disabled	Enabled: on each measurement phase Duty Cycle will be raised to 100% for 100mS then restored to original value to allow a more precise measure avoiding unwanted ripple on tachometer. Disabled: periodic fan speed up will not occur, but RPM measurement will not be accurate
Automatic Temperature FAN Control	Enabled / Disabled	Disable / Enable Thermal Feed-back FAN Control
AC0 Temperature (°C)	70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "Automatic Temperature FAN Control"is Enabled AC0: above this temperature the FAN runs at full speed

AC1 Temperature (°C)	5 / 10 / 15 / 20 /25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "Automatic Temperature FAN Control" is Enabled. AC1: below this temperature the FAN is OFF; between AC1 and AC0 the FAN runs at low speed: this never happens if AC1 is not below AC0.
Temperature Hysteresis	0 .. 10	Only available when "Automatic Temperature FAN Control" is Enabled. Value added (when temperature is growing) to the ACx thresholds or subtracted from them (when temperature is decreasing) to avoid oscillations.
Linear Speed change	Enabled / Disabled	Only available when "Automatic Temperature FAN Control" is Enabled. Linear FAN Duty Cycle growth between AC1 and AC0
FAN Duty Cycle (%) Above AC1	0 .. 100	Only available when "Automatic Temperature FAN Control" is Enabled and "Linear Speed change" is Disabled Fan Duty Cycle (%) between AC1 and AC0 (low speed)
Speed Change Duration	0 .. 50	Only available when "Automatic Temperature FAN Control" is Enabled and "Linear Speed change" is Disabled Duration in seconds of linear FAN Speed Change. Allowed range: from 0 to 50.
FAN PWM Frequency	1 .. 60000	Only available when "Automatic Temperature FAN Control" is Disabled. Sets the frequency of the FAN_PWMOUT signal. Typical values are 100 for a 3-wire device and 20000 for a 4-wire one. Allowed range is 1-60000.
FAN Duty Cycle	0 .. 100	Only available when "Automatic Temperature FAN Control" is Disabled. Default FAN Duty Cycle (%).

4.3.16.3 External FAN/PWM Settings submenu

Menu Item	Options	Description
FAN_PWMOUT Device Type	3-Wire FAN 4-Wire FAN Generic PWM	Specifies if FAN_PWMOUT is connected to a 3-wire or 4-wire FAN or to a generic PWM.
Enhanced 3 wire RPM measurement	Enabled / Disabled	Only available when "FAN_PWMOUT Device Type" is set to 3-Wire FAN Enabled: on each measurement phase Duty Cycle will be raised to 100% for 100mS then restored to original value to allow a more precise measure avoiding unwanted ripple on tachometer. Disabled: periodic fan speed up will not occur, but RPM measurement will not be accurate
Automatic Temperature FAN Control	Enabled / Disabled	Only available when "FAN_PWMOUT Device Type" is set to 3-Wire FAN or 4-Wire FAN Disable / Enable Thermal Feed-back FAN Control
AC0 Temperature (°C)	70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "Automatic Temperature FAN Control" is Enabled AC0: above this temperature the FAN runs at full speed

AC1 Temperature (°C)	5 / 10 / 15 / 20 /25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "Automatic Temperature FAN Control" is Enabled. AC1: below this temperature the FAN is OFF; between AC1 and AC0 the FAN runs at low speed: this never happens if AC1 is not below AC0.
Temperature Hysteresis	0 .. 10	Only available when "Automatic Temperature FAN Control" is Enabled. Value added (when temperature is growing) to the ACx thresholds or subtracted from them (when temperature is decreasing) to avoid oscillations.
Linear Speed change	Enabled / Disabled	Only available when "Automatic Temperature FAN Control" is Enabled. Linear FAN Duty Cycle growth between AC1 and AC0
FAN Duty Cycle (%) Above AC1	0 .. 100	Only available when "Automatic Temperature FAN Control" is Enabled and "Linear Speed change" is Disabled Fan Duty Cycle (%) between AC1 and AC0 (low speed)
Speed Change Duration	0 .. 50	Only available when "Automatic Temperature FAN Control" is Enabled and "Linear Speed change" is Disabled Duration in seconds of linear FAN Speed Change. Allowed range: from 0 to 50.
FAN PWM Frequency	1 .. 60000	Only available when "Automatic Temperature FAN Control" is Disabled. Sets the frequency of the FAN_PWMOUT signal. Typical values are 100 for a 3-wire device and 20000 for a 4-wire one. Allowed range is 1-60000.
FAN Duty Cycle	0 .. 100	Only available when "Automatic Temperature FAN Control" is Disabled. Default FAN Duty Cycle (%).

4.3.16.4 Watchdog Configuration submenu

Menu Item	Options	Description
Watchdog Status	Disabled / Enabled	Enables or disables the Watchdog Timer. When enabled, the following parameters will appear
Event action	Raise WDT Signal Power Button Pulse	Action executed at the expiring of the Event time-out.
Reset action	System Reset Power Button Override Raise WDT Signal	Action executed at the expiring of the reset time-out.
Watchdog Delay	0 .. 60	Minutes before watchdog normal operations starts. During delay time-out, a refresh operation will immediately trigger the normal operation.
Event time-out	0 .. 60	Time-out minutes that can pass without refresh before triggering the Event Action. A refresh will restart the time-out.

Reset time-out	1 .. 60	Time-out minutes that can pass without refresh before triggering the Reset Action, this timer will start counting when event time-out is expired.

4.3.16.5 GPIO Configurations submenu

Menu Item	Options	Description
GPO0 GPO1 GPO2 GPO3	Output Low Output High Output Last	Configure pin output starting value. Last means no changes with respect to the last boot.

4.4 Chipset menu

Menu Item	Options	Description
South Bridge	See submenu	South Bridge Parameters
Uncore Configuration	See submenu	Uncore Configuration Parameters
South Cluster Configuration	See submenu	South Cluster Configuration Parameters

4.4.1 South Bridge submenu

Menu Item	Options	Description
Serial IRQ Mode	Quiet Mode Continuous Mode	Select Serial IRQ Mode. In continuous mode, the host will continually check for device interrupts. In Quiet Mode, Host will wait for a SERIRQ slave to generate a request by driving the SERIRQ line low.
OS Selection	Windows / Android / Win7 / Intel Linux	Select the Target OS

4.4.2 Uncore Configuration submenu

Menu Item	Options	Description
GOP Brightness Level	20/40/60/80/100/120/140/160/180/200/220/240/255	Set Graphics Output Protocol (GOP) Brightness Level
DDI0 DDC Pull Type	Pull Up 1K Pull Up 2K Pull Up 5K	Sets DDI #0 Pull-up values
DDI1 DDC Pull Type	Pull Up 1K Pull Up 2K Pull Up 5K	Sets DDI #1 Pull-up values
Integrated Graphics Device	Enabled / Disabled	Enable the Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor, or always disable it.
Primary Display	IGD / PCIe / HG	Select which of IGD / PCIe /HG graphics device should be the Primary Display
HG Delay After Power Enable	[0..1000]	Only available when "Primary Display" is set to HG. Delay in milliseconds after power enable
HG Delay After Hold Reset	[0..1000]	Only available when "Primary Display" is set to HG. Delay in milliseconds after hold reset

RC6 (Render Standby)	Enabled / Disabled	Permits to enable the render standby features, which allows the on-board graphics entering in standby mode to decrease power consumption
GTT Size	2 MB / 4 MB / 8 MB	Select the GTT (Graphics Translation Table) Size
Aperture Size	256 MB	Use this item to set the total size of Memory that must be left to the GFX Engine
DVMT Pre-Allocated	64M / 96M / 128M / 160M / 192M / 224M / 256M / 288M / 320M / 352M / 384M / 416M / 448M / 480M / 512M	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphic Device
DVMT Total Gfx Mem	128M / 256M / MAX	Select the size of DVMT (Dynamic Video Memory) 5.0 that the Internal Graphics Device will use
Cd Clock Frequency	144 MHz / 288 MHz / 384 MHz / 576 MHz / 624 MHz	Select the highest CD Clock frequency supported by the platform
GT PM Support	Enabled / Disabled	Enable / Disable GT Power Management Support
PAVP Enable	Enabled / Disabled	Enable / Disable Protected Audio Video Playback (PAVP)
Memory Scrambler	Enabled / Disabled	Enable / Disable the Memory Scrambler Support

4.4.3 South Cluster Configuration submenu

Menu Item	Options	Description
HD Audio Configuration	See submenu	HD Audio Configuration Settings
LPSS Configuration	See submenu	Low Power Sub System Configuration Settings
PCI Express Configuration	See submenu	PCI Express Configuration Settings
SATA Drives	See submenu	SATA Devices Configuration Setup options
SCC Configuration	See submenu	Storage Control Cluster Configuration Settings
USB Configuration	See submenu	USB configuration Settings
Miscellaneous Configuration	See submenu	Miscellaneous Settings

4.4.3.1 HD Audio Configuration submenu

Menu Item	Options	Description
HD Audio Support	Enabled / Disabled	Enable / Disable HD Audio Support

HD Audio DSP	Enabled / Disabled	Enable / Disable HD Audio DSP

4.4.3.2 LPSS Configuration

Low Power Sub System configuration settings may not be available.

4.4.3.3 PCI Express Configuration submenu

Menu Item	Options	Description
Compliance Mode	Enabled / Disabled	Enable / Disable Compliance Mode
PCIE Root Port 3 - COMe PCIE0 PCIE Root Port 4 - COMe PCIE1 PCIE Root Port 5 - COMe PCIE2 PCIE Root Port 6 – Internal LAN	See submenus	Sets the parameters for each single PCI-e Root Port

4.4.3.3.1 PCIE Root Port #x submenus

Menu Item	Options	Description
PCIE Root Port 3 - COMe PCIE0 PCIE Root Port 4 - COMe PCIE1 PCIE Root Port 5 - COMe PCIE2 PCIE Root Port 6 – Internal LAN	Auto Enabled Disabled	Controls the PCI Express Root Port. Auto: disable unused root port automatically for the most optimised power saving. Enable: Always enable the PCIe root port. Disable: Always disable the PCIe root port *(all the following items will disappear)*
ASPM	Disable / L0s	PCI Express Active State Power Management Settings
PCIe Speed	Auto Gen1 Gen2	Configure PCIe Speed
PCIe Selectable De-Emphasis	Enabled / Disabled	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5dB 0b -6dB

4.4.3.4 SATA Drives Configuration submenu

Menu Item	Options	Description
SATA Controller	Enabled / Disabled	Enable / Disable Chipset SATA controller, which supports the 2 black internal SATA ports (up to 3GB/s supported per port).
SATA Test Mode	Enabled / Disabled	Enable / Disable SATA Test Modes

SATA Speed	Gen1 Gen2 Gen3	Select SATA Speed
Port 0 Port 1	Enabled / Disabled	Enable / Disable SATA Port #x

4.4.3.5 SCC Configuration submenu

Menu Item	Options	Description
SCC SD Card Support	Enabled / Disabled	Enable / Disable SCC SD Card Support
SCC eMMC Support	Enabled / Disabled	Enable / Disable SCC eMMC Card Support

4.4.3.6 USB Configuration submenu

Menu Item	Options	Description
xHCI Pre-Boot Driver	Enable / Disable	Enable / Disable support for XHCI Pre-boot driver
xHCI Mode	Enable / Disable	Once Disabled, the xHCI Controller function will be disabled, none of the USB devices will be detectable and usable during boot and from the OS. Do not disable xHCI unless is for debug purposes
USB Port Disable Override	Enable / Disable	Allows enabling or disabling selectively each single USB port from reporting a device connection to the controller.
USB Port #0 USB Port #1 USB Port #2 USB Port #3 USB Port #4 USB Port #5 USB Port #6 USB Port #7 USB 3 Port #0 USB 3 Port #1 USB 3 Port #2 USB 3 Port #3	Enable / Disable	Only available when "USB Port Disable Override" is Enabled. Allows enabling or disabling the single USB Port #x. Once disabled, any USB device connected to the corresponding port will not be detected by the BIOS neither by the OS
XDCI Support	Disable / PCI Mode	Enable / Disable XDCI (USB dual role functionality)
XDCI Disable Compliance Mode	FALSE / TRUE	Options to disable XHCI Link Compliance Mode. Default is FALSE to not disable Compliance Mode. Set TRUE to disable Compliance Mode

4.4.3.7 Miscellaneous Configuration submenu

Menu Item	Options	Description
Wake On Lan	Enabled / Disabled	Enable / disable the Wake On LAN Feature
BIOS Lock	Enabled / Disabled	Enables or disables the SC BIOS Lock enable feature. It is required that it is enabled to ensure SMM protection of flash
Flash Protection Range Registers	Enabled / Disabled	Enable Flash Protection Range registers
Reset Power Cycle Duration	1-2 seconds 2-3 seconds 3-4 seconds 4-5 seconds	The value in this register determines the minimum time a platform will stay in reset during a host partition reset with power cycle or a global reset

4.5 Security menu

Menu Item	Options	Description
Setup Administrator Password		Set Setup Administrator Password
User Password		Set User Password
Secure Boot	See Submenu	Customizable Secure Boot Settings

4.5.1 Secure Boot submenu

Menu Item	Options	Description
Secure Boot	Enabled / Disabled	Secure Boot is activated when the Platform Key (PK) is enrolled, System Mode is User/Deployed and CSM function is disabled.
Secure Boot Customization	Standard / Custom	Set UEFI Secure Boot Mode to STANDARD Mode or CUSTOM mode. Effective after save, reverts to Standard after reset.
Restore Factory Keys		Active only when "Secure Boot Customization" is set to Custom. Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys
Key management	See submenu	Active only when "Secure Boot Customization" is set to Custom. Enable expert users to modify Secure Boot Policy variables without full authentication

4.5.1.1 Key Management submenu

Menu Item	Options	Description
Factory Key Provision	Enabled / Disabled	Provision factory default keys on next re-boot only when System in Setup Mode
Restore Factory Keys		Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys
Enroll Efi Image	*File System Image*	Run selected image in Secure Boot mode. Enrol SHA256 Hash Certificates of image into Authorized Signature Database
Restore DB defaults		Restore DB variable to factory defaults
Platform key (PK) Key Exchange Keys Authorized Signatures Forbidden Signatures Authorized Timestamps OS Recovery Signatures	Set New Var Append Key	Enrol factory Defaults or load certificates from a file: 1. Public Key Certificate in: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER encoded) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHA256,384,512 2. Authenticated UEFI variables 3. EFI PE/COFF Image (SHA256), Key Source: Factory, External, Mixed

4.6 Boot menu

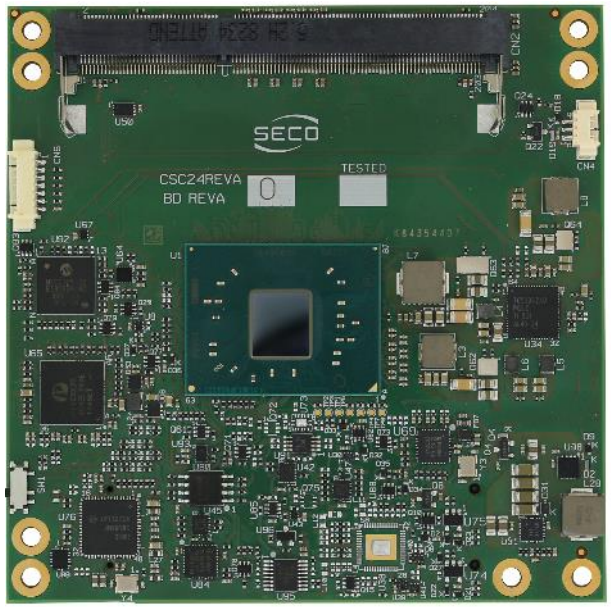
Menu Item	Options	Description
Setup Prompt Timeout	0 .. 65535	Number of seconds to wait for setup activation key. 655535 means indefinite waiting.
Bootup NumLock State	On / Off	Select the Keyboard NumLock State at boot
Quiet Boot	Enabled / Disabled	Enables or Disables Quiet Boot options
New Boot Option Policy	Default Place First Place Last	Controls the placement of newly detected UEFI boot options
Boot Mode Select	LEGACY UEFI	Select the boot mode between Legacy and UEFI
Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4 Boot Option #5 Boot Option #6 Boot Option #7 Boot Option #8	Hard Disk0 Hard Disk1 eMMC CD/DVD SD USB Device Network Other Device Disabled	Select the system boot order

4.7 Save & Exit menu

Menu Item	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Changes and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset the system without saving any changes.
Save Changes		Save the changes done so far to any of the setup options.
Discard Changes		Discard the changes done so far to any of the setup options.
Restore Defaults		Restore/Load Default values for all the setup options
Save as User Defaults		Save the changes done so far as User Defaults
Restore User Defaults		Restore the User Defaults to all the setup options
Launch EFI Shell from filesystem device		Attempt to Launch the EFI Shell application (Shell.efi) from one of the available filesystem devices

Chapter 5.
Appendices

- Thermal Design



5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like COMe-C24-CT6 module, offer to the user very good performances in minimal spaces, therefore allowing the system's minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

COM Express® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the COM Express® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsink with fan in some situation can represent the cooling solution. Indeed, when using COMe-C24-CT6 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with FAN could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide COMe-C24-CT6 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions. Please ask SECO for specific ordering codes.

Warning!

The thermal solutions available with SECO boards are tested in the commercial temperature range (0-60°C), without housing and inside climatic chamber. Therefore, the customer is suggested to study, develop and validate the cooling solution for his system, considering ambient temperature, processor's workload, utilisation scenarios, enclosures, air flow and so on.

In particular, the heatspreader is not intended to be a cooling system by itself, but only as the standard means for transferring heat to cooler, like heatsinks, cold plate, heat pipes and so on.

SECO S.p.A. - Via A. Grandi, 20
52100 Arezzo - ITALY
Ph: +39 0575 26979 - Fax: +39 0575 350210
www.seco.com