Com express

User Manual

COMe-953 BT6

COM-Express™ Type 6 Module with the
Intel® Haswell family CPUs and the QM87 Chipset

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	16th February 2015	First Official Release	SB
2.0	26th January 2016	Product name change	SB
2.1	5th August 2016	ECC version added. Block diagram updated. UART interface signals added	SB

Every effort has been made to ensure the accuracy of this manual. However, SECO S.r.l. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.r.l. reserves the right to change precise specifications without prior notice to supply the best product possible.

Some of the information found in the BIOS SETUP Chapter has been extracted from the following copyrighted Insyde Software Corp. documents:

- InsydeH2O™ Setup Utility - User Reference Guide

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist you.

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Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications

1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.r.l. could impair the equipments and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.r.l. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The COMe-953-BT6 module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The COMe-953-BT6 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling a COMe-953-BT6 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The COMe-953-BT6 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CRT	Cathode Ray Tube. Initially used to indicate a type of monitor, this acronym has been used over time to indicate the analog video interface used to drive them.
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
DDR3	DDR, 3rd generation
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
ECC	Error Correcting Code, a peculiar type of memory module with 72-bit of data instead of 64, where the additional 8 bit are used to detect and correct possible errors on the remaining 64-bit data bus
eDP	embedded Display Port, a type of digital video display interface specifically developed for the internal connections between boards and digital displays
EHCI	Enhanced Host Controller interface, a high-speed controller for USB ports, able to support USB2.0 standard
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
JTAG	Joint Test Action Group, common name of IEEE1149.1 standard for testing printed circuit boards and integrated circuits through the Debug port
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signaling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second

MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC: They are devices that include both the memory controller and the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OHCI	Open Host Controller Interface, full-speed and low-speed controller for support of USB 1.1 ports
OS	Operating System
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port
PCI-e	Peripheral Component Interface Express
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
PXE	Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDHC	Secure Digital Host Controller
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signaling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
USB	Universal Serial Bus
V_REF	Voltage reference Pin
VGA	Video Graphics Array. An analog computer display standard, commonly referred to also as CRT.
xHCI	eXtensible Host Controller Interface, Host controller for USB 3.0 ports, which can also manage USB 2.0 and USB1.1 ports

1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
Com Express	http://www.picmg.org/v2internal/specifications2.cfm?thetype=One&thebusid=3
Com Express Carrier Design Guide	http://picmg.org//wp-content/uploads/PICMG_COMDG_2.0-RELEASED-2013-12-061.pdf
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
UEFI	http://www.uefi.org
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip
Intel® Haswell family	http://www.intel.com/content/www/us/en/processors/core/4th-gen-core-processor-family.html

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram

2.1 Introduction

The COMe-953-BT6 is a COM Express® Type 6, basic Form Factor, based on the 4th generation of Intel® Core™ or Celeron® CPUs, interfaced to Intel® QM87 chipset, which completes the standard functionalities. A complete list of CPUs available is detailed in the next chapter.

All the supported CPUs offer a 64-bit Instruction set and Hyper Threading capabilities, and provide direct access to the memory, which is available on two SODIMM DDR3L memory modules. Depending on the CPU, memory frequencies up to 1866MHz are supported, with a maximum capacity up to 16GB. Please notice that total amount of memory available is OS dependant.

The COMe-953-BT6 module is available in two versions, able to support ECC or non-ECC modules. Please be aware that boards configured to work with non-ECC modules will not work using ECC modules, and vice versa.

All CPUs integrate an Intel® HD Graphics Controller, which offers an advanced 2D and 3D graphic engine and it is able to manage up to 3 independent displays (any combination possible between HDMI, DVI, DP++, eDP, LVDS and VGA, with the only exception of 3 HDMI/DVI displays, which are not supported). It makes available three Digital Display Interfaces that can be used to drive external Display Port, HDMI or DVI displays; moreover, the embedded Display Port interface can be carried out on COM Express connectors directly or used to realise a Dual Channel 18/24bit interface (this is a factory configuration). An additional CRT interface represents another video output offered by the CPU. Further graphical possibilities are given by CPU's PCI Express graphics x 16 interface.

The QM87 chipset completes the functionalities of the board offering HD Audio Interface, 8 x PCI Express ports (one of them used to manage a Gigabit Ethernet controller), 4 x Serial ATA channels, 8 USB 2.0 ports, 4 USB 3.0 ports, Real Time Clock, LPC and SM Bus.

The module can be offered with an optional additional TPM module OR with two serial ports at TTL level.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

The product is COM Express® Rel.2.1 standard compliant, an open industry standard defined specifically for COMs (computer on modules). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available. Specifically, COMe-953-BT6 is a COM Express® module, Basic Form factor, Type 6 (125mm x 95mm).

COM Express® module integrates all the core components and has to be mounted onto an application-specific carrier board; carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimised package, which results in a more reliable product while simplifying system integration. Most important, COM Express® modules are scalable, which means that once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

2.2 Technical Specifications

CPU

Intel® Core™ i3-4100E, Dual Core with HT @ 2.4GHz, 3MB Cache, 37W TDP
Intel® Core™ i3-4102E, Dual Core with HT @ 1.6GHz, 3MB Cache, 25W TDP
Intel® Core™ i5-4400E Dual Core with HT @ 2.7GHz, 3MB Cache, 37W TDP
Intel® Core™ i5-4402E Dual Core with HT @ 1.6GHz, 3MB Cache, 25W TDP
Intel® Core™ i7-4700EQ Quad Core with HT @ 2.4GHz, 6MB Cache, 47W TDP
Intel® Celeron® 2002E Dual Core @1.5GHz, 2MB Cache, 25W TDP
Intel® Celeron® 2000E Dual Core @2.2GHz, 2MB Cache, 37W TDP

Chipset

Intel® QM87 Chipset

Memory

Up to 16GB 1.35V DDR3L-1600 on two SO-DIMM slots, supporting Dual-Channel
M953 modules support non-ECC SO-DIMMs only, MB28 modules support ECC modules only

Graphics

Integrated Intel® HD Graphics
Up to 3 independent display supported
DirectX® 11, OpenGL4.0 supported

Video Interfaces

3 x HDMI/DVI/Multimode Display Port interfaces
embedded Display Port **or** 18/24 bit single/dual channel LVDS interface
CRT interface
PCI Express Graphics (PEG) x 16 interface

Video Resolutions

CRT Interface:	up to 1920 x 1200 @ 60Hz
HDMI	up to 4096x2304 @ 24Hz / 2560x1600 @ 60Hz
DVI	up to 1920x1200 @ 60Hz
Display Port	up to 3840 x 2160 @ 60Hz
LVDS, eDP	up to 1920 x 1200 @ 60Hz

Mass Storage

4 x external S-ATA channels

USB

8 x USB 2.0 Host Ports
4 x USB 3.0 Host ports

Networking

Gigabit Ethernet interface
Supports remote management (Intel® AMT Technology)

Audio

HD Audio interface

PCI Express

7 x PCI-e x1 lanes (configurable as 1 PCI-e x 4 + 3 PCI-e x1)

Serial Ports

2 x serial ports (Tx/Rx only, TTL interface; MB28 modules only)

Other Interfaces

2 x Express Card interfaces
I2C bus
LPC Bus
SM Bus
4 x GPI, 4 x GPO
Thermal / FAN management
Watch Dog timer
Optional TPM on-board (M953 modules only)
Power Management Signals

Power supply voltage: +12V_{DC} ± 10% and + 5V_{SB} (optional)

Operating temperature: 0°C ÷ +60°C (commercial version) **

Dimensions: 125 x 95 mm (4.92" x 3.74")

! *** Temperatures indicated are the minimum and maximum temperature that the heatspreader / heatsink can reach in any of its parts. This means that it is customer's responsibility to use any passive cooling solution along with an application-dependent cooling system, capable to ensure that the heatspreader / heatsink temperature remains in the range above indicated. Please also check paragraph 5.1*

2.3 Electrical Specifications

According to COM Express® specifications, the COMe-953-BT6 board needs to be supplied only with an external +12V_{DC} power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through COM Express Connectors CN5 and CN6.

All remaining voltages needed for board's working are generated internally from +12V_{DC} power rail.

2.3.1 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_S: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_S, +5V_S.

_A: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_A, +3.3V_A.

_U: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_U.

2.3.2 Power Consumption

COMe-953-BT6 module, like all COM Express™ modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Therefore, power consumptions of the board are measured using a CCOMe-965 Carrier board on +12V_S power rail that supplies the board. For this reason, the values indicated in the table below are real power consumptions of the board, and are independent from those of the peripherals connected to the Carrier Board.

Power consumption in Suspend and Soft-Off States have been measured on +5V_A power rail. RTC power consumption has been measured on carrier board's backup battery when the system is <not powered (VCC_RTC power rail).

The current consumptions, written in the table of this page, have been measured using the following setup:

- O.S. Windows 8 Enterprise 64-Bit
- 8GB DDR3L (2 x 4GB SO-DIMM DDR3L 1600MHz modules, p/n Transcend TS512MSK64W6H)
- 120GB SATA mechanical Hard Disk (p/n HM121HI) connected
- USB mouse and keyboard connected
- VGA display connected.
- Network connected, Wake-On-LAN enabled
- PSU Enermax FMAll 535W, p/n E6G565AX-VE (G)

Status	CPU				
	i7-4700EQ	i5-4400E	i5-4402E	i3-4100E	i3-4102E
Idle, power saving configuration	1018 mA	946 mA	920 mA	933 mA	925 mA
OS Boot, power saving configuration	2565 mA	2520 mA	1750 mA	1865 mA	1350 mA
Video reproduction@720p, power saving configuration	1330 mA	1390 mA	1738 mA	1799 mA	1314 mA
Video reproduction@1080p, power saving configuration	1380 mA	1413 mA	1745 mA	1856 mA	1320 mA
3DMark Vantage benchmark, power saving configuration	3212 mA	2825 mA	2046 mA	2396 mA	1880 mA
3DMark Vantage benchmark, maximum performance	3223 mA	2899 mA	2147 mA	2721 mA	2596 mA
Suspend to RAM (typical)	75 mA	75 mA	75 mA	75 mA	75 mA
Soft Off (typical)	48 mA	48 mA	48 mA	48 mA	48 mA
RTC Power consumption (typical)	2,8 µA	2,8 µA	2,8 µA	2,8 µA	2,8 µA

2.3.3 Inrush Current

In the following table are shown the inrush current relative to the total current drawn by COMe-953-BT6 module on +12V_S and +5V_A power rails.

Inrush current measurements are made using a Current Probe Chauvin Arnoux E3N 10-100A/V and an Oscilloscope Agilent DSO 3202A.

These inrush currents have been measured using the same setup described in the previous paragraph.

Status	CPU				
	i7-4700EQ	i5-4400E	i5-4402E	i3-4100E	i3-4102E
12V_S Peak Current at Power On	2.1 A	2.2 A	2.22 A	2.22 A	2 A
5V_A Peak Current at Power On	2.25 A	2.4 A	2.4 A	2.3 A	2.4 A
12V_S Peak Current during O.S. Boot	4.45 A	3 A	2.5 A	2.4 A	2.2 A

2.4 Mechanical Specifications

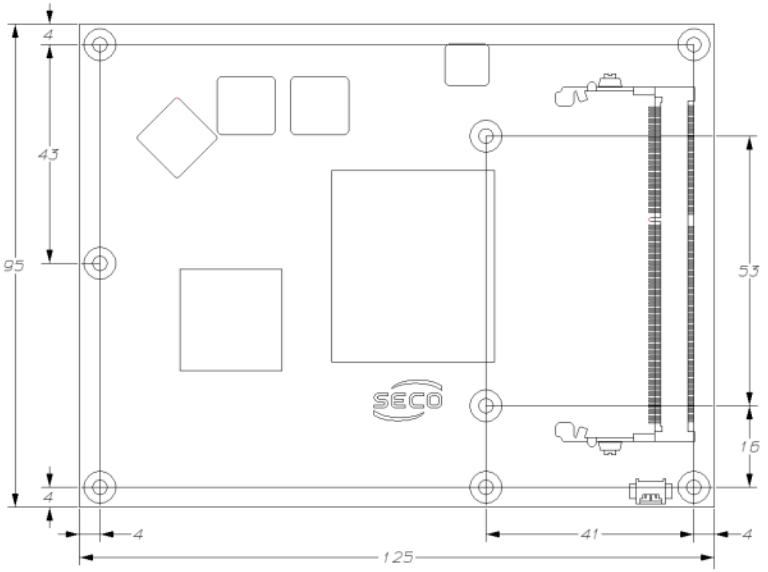
The COMe-953-BT6 is a COM Express board, Basic form Factor type; therefore its dimensions are 125 mm x 95 mm (4.92” x 3.74”).

Printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

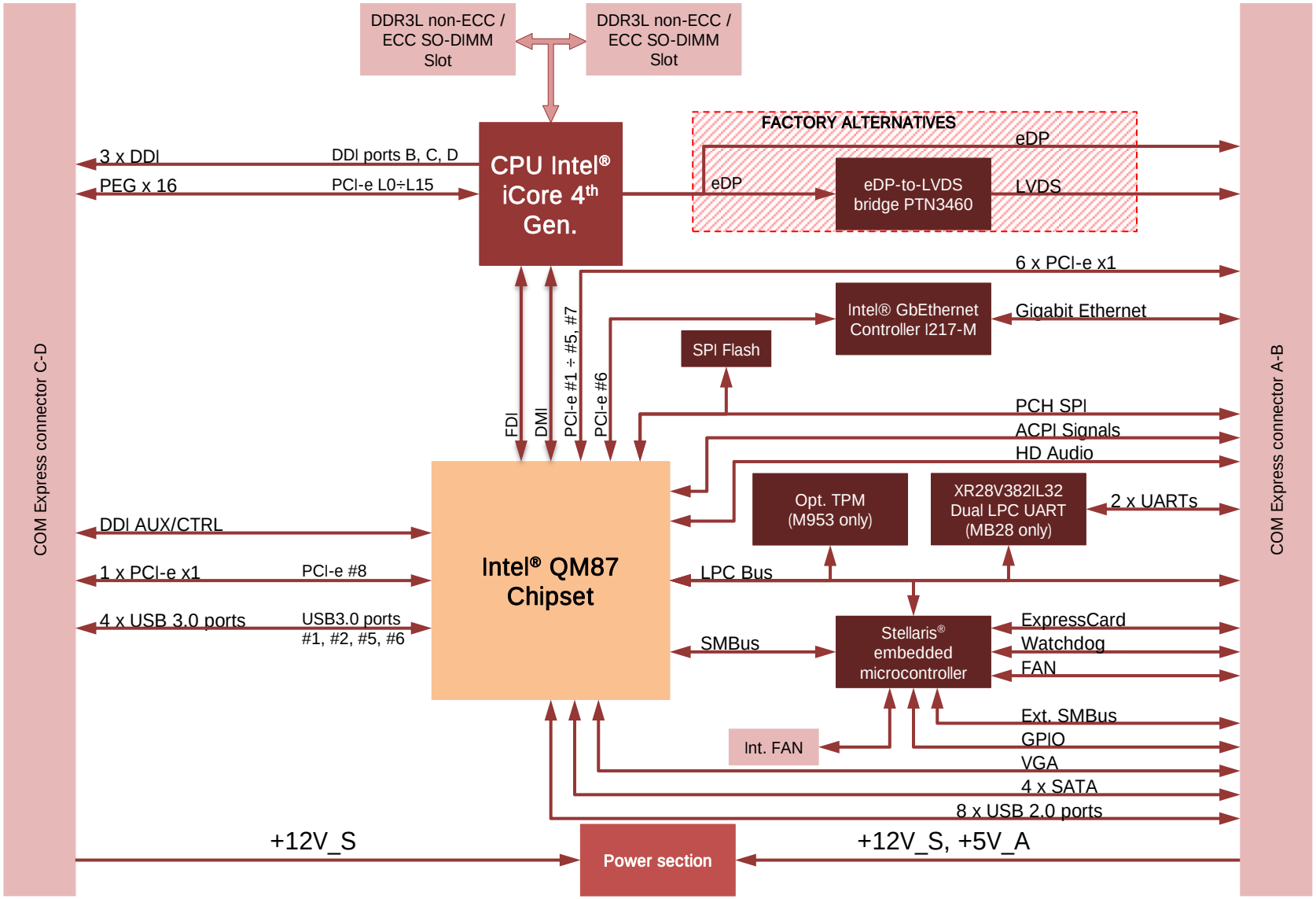
According to COM Express specifications, the carrier board plug can be of two different heights, 5mm and 8mm.

Whichever connector’s height is chosen, in designing a custom carrier board please remember that, according to COM Express® specifications, components placed on bottom side of COMe-953-BT6 will have a maximum height of 3.8mm.

This value must be kept in high consideration when choosing the carrier board plugs’ height, if it is necessary to place components on the carrier board in the zone under the COM Express® module.



2.5 Block Diagram



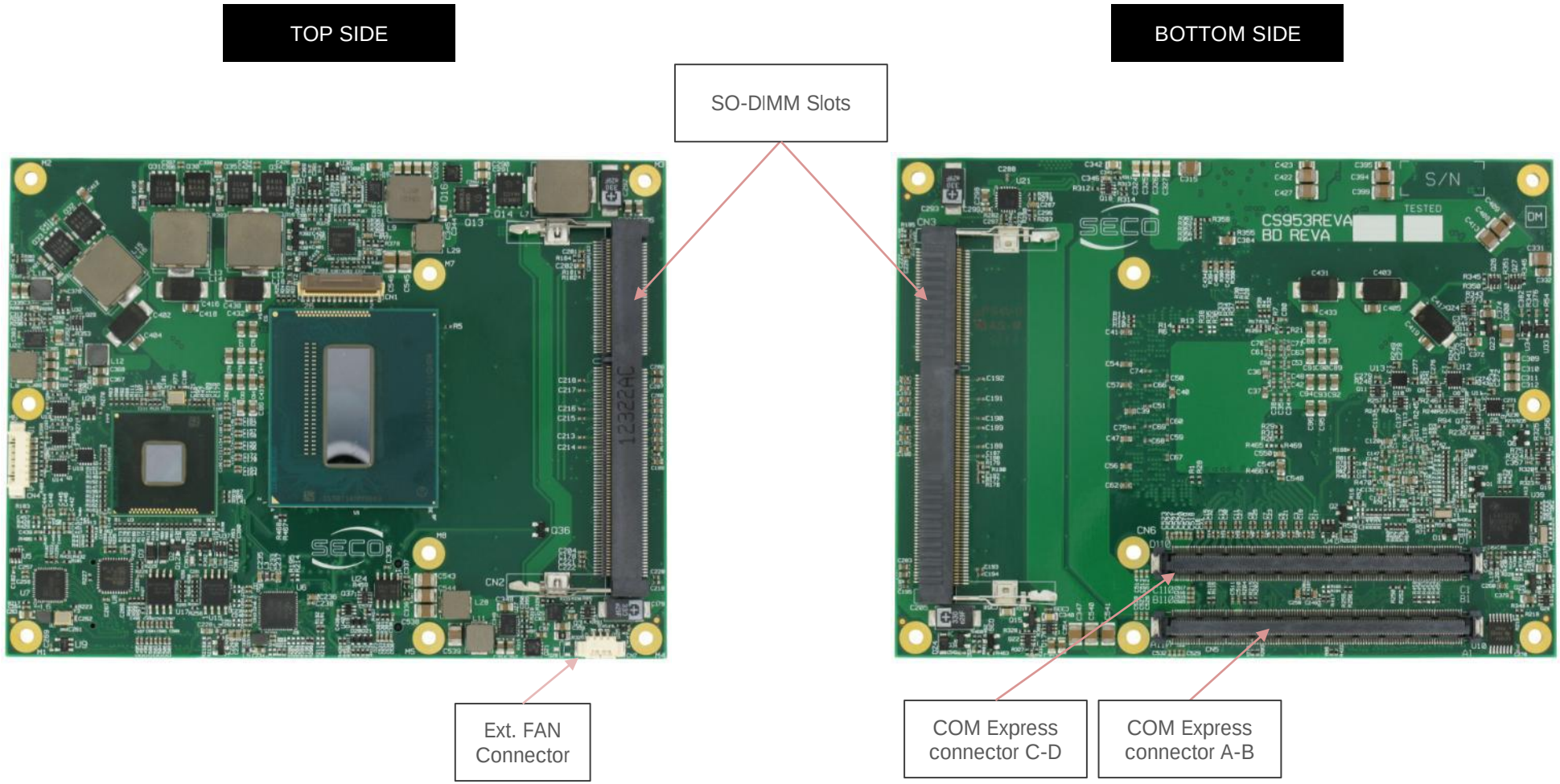
Chapter 3.
CONNECTORS

- Introduction
- Connectors description

3.1 Introduction

According to COM Express® specifications, all interfaces to the board are available through two 220 pin connectors, for a total of 440 pin. Simplifying the terminology in this documentation, the primary connector is called A-B and the secondary C-D, since each one consists of two rows.

In addition, a Fan connector has been placed on one side of the board, in order to allow an easier connection of active heatsinks to the module.

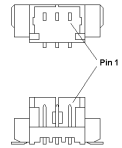


3.2 Connectors description

3.2.1 FAN Connector

FAN Connector - CN2	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN

Depending on the usage model of COMe-953-BT6 module, for critical applications/environments on the module itself it is available a 3-pin dedicated connector for an external +12VDC FAN.



FAN Connector is a 3-pin single line SMT connector, type MOLEX 53261-0319 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

Please refer to chapter 5.1 for considerations about thermal dissipation.

FAN_POWER: +12V_S derived power rail for FAN, managed by the embedded microcontroller via PWM signal.

FAN_TACHO_IN: tachometric input from the fan to the embedded microcontroller, +3.3V_S electrical level signal with 10kΩ pull-up resistor.

3.2.2 SO-DIMM DDR3 Slots

CPUs used on the COMe-953-BT6 board provide support to DDR3L-1600 (i.e., working with +1.35V voltage) memories.

For use of this memories, on board there are two SO-DIMM DDR3L sockets.

The socket placed on top side (CN2) is type Tyco 2013290-1 or equivalent, a right angle, low profile, reverse type socket, used for high speed system memory applications.

The socket placed on bottom (CN3) side is type Tyco 2013022-1 or equivalent, and is a socket with performances similar to the other, only it is standard type, not reverse. The two sockets together allow the insertion of up to 2 SO-DIMM modules, for support to dual channel memories.

Please be aware that M953 modules support non-ECC modules only, while MB28 modules support ECC modules only.

Using the wrong type of modules will prevent the board from starting, and could result also in damages to the module itself.

3.2.3 COM Express® Module connectors

For the connection of COM Express® CPU modules, on board there is one double connector, type TYCO 3-1827231-6 (440 pin, ultra thin, 0.5mm pitch, h=4mm), as requested by COM Express® specifications.

The pinout of the module is compliant to COM Express® Type 6 specifications. Not all the signals contemplated in COM Express® standard are implemented on the double connector, due to the functionalities really implemented on COMe-953-BT6 board. Therefore, please refer to the following table for a list of effective signals reported on the connector. For accurate signals description, please consult the following paragraphs.

COM Express® Connector AB - CN5							
		ROW A			ROW B		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	A1	B1	GND	PWR	
GBE	I/O	GBE0_MDI3-	A2	B2	GBE0_ACT#	O	GBE
GBE	I/O	GBE0_MDI3+	A3	B3	LPC_FRAME#	O	LPC
GBE	O	GBE0_LINK100#	A4	B4	LPC_AD0	I/O	LPC
GBE	O	GBE0_LINK1000#	A5	B5	LPC_AD1	I/O	LPC
GBE	I/O	GBE0_MDI2-	A6	B6	LPC_AD2	I/O	LPC
GBE	I/O	GBE0_MDI2+	A7	B7	LPC_AD3	I/O	LPC
GBE	O	GBE0_LINK#	A8	B8	LPC_DRQ0#	I	LPC
GBE	I/O	GBE0_MDI1-	A9	B9	LPC_DRQ1#	I	LPC
GBE	I/O	GBE0_MDI1+	A10	B10	LPC_CLK	O	LPC
	PWR	GND	A11	B11	GND	PWR	
GBE	I/O	GBE0_MDI0-	A12	B12	PWRBTN#	I	PWR_MGMT
GBE	I/O	GBE0_MDI0+	A13	B13	SMB_CK	I/O	SMBUS
	N.A.	N.C.	A14	B14	SMB_DAT	O	SMBUS
PWR_MGMT	O	SUS_S3#	A15	B15	SMB_ALERT#	I	SMBUS
SATA	O	SATA0_TX+	A16	B16	SATA1_TX+	O	SATA
SATA	O	SATA0_TX-	A17	B17	SATA1_TX-	O	SATA
PWR_MGMT	O	SUS_S4#	A18	B18	SUS_STAT#	O	PWR_MGMT
SATA	I	SATA0_RX+	A19	B19	SATA1_RX+	I	SATA
SATA	I	SATA0_RX-	A20	B20	SATA1_RX-	I	SATA

	PWR	GND	A21	B21	GND	PWR	
SATA	O	SATA2_TX+	A22	B22	SATA3_TX+	O	SATA
SATA	O	SATA2_TX-	A23	B23	SATA3_TX-	O	SATA
PWR_MGMT	O	SUS_S5#	A24	B24	PWR_OK	I	PWR_MGMT
SATA	I	SATA2_RX+	A25	B25	SATA3_RX+	I	SATA
SATA	I	SATA2_RX-	A26	B26	SATA3_RX-	I	SATA
PWR_MGMT	I	BATLOW#	A27	B27	WDT	O	MISC
SATA	O	SATA_ACT#	A28	B28	HDA_SDIN2	I/O	AUDIO
AUDIO	O	HDA_SYNC	A29	B29	HDA_SDIN1	I/O	AUDIO
AUDIO	O	HDA_RST#	A30	B30	HDA_SDIN0	I/O	AUDIO
	PWR	GND	A31	B31	GND	PWR	
AUDIO	O	HDA_BITCLK	A32	B32	SPKR	O	MISC
AUDIO	O	HDA_SDOUT	A33	B33	I2C_CK	O	I2C
SPI	I	BIOS_DIS0#	A34	B34	I2C_DAT	I/O	I2C
MISC	O	THRMTRIP#	A35	B35	THRM#	I	MISC
USB	I/O	USB6-	A36	B36	USB7-	I/O	USB
USB	I/O	USB6+	A37	B37	USB7+	I/O	USB
USB	I	USB_6_7_OC#	A38	B38	USB_4_5_OC#	I	USB
USB	I/O	USB4-	A39	B39	USB5-	I/O	USB
USB	I/O	USB4+	A40	B40	USB5+	I/O	USB
	PWR	GND	A41	B41	GND	PWR	
USB	I/O	USB2-	A42	B42	USB3-	I/O	USB
USB	I/O	USB2+	A43	B43	USB3+	I/O	USB
USB	I	USB_2_3_OC#	A44	B44	USB_0_1_OC#	I	USB
USB	I/O	USB_0-	A45	B45	USB1-	I/O	USB
USB	I/O	USB_0+	A46	B46	USB1+	I/O	USB
	PWR	VCC_RTC	A47	B47	EXCD1_PERST#	O	EXCD
EXCD	O	EXCD0_PERST#	A48	B48	EXCD1_CPPE#	I	EXCD
EXCD	I	EXCD0_CPPE#	A49	B49	SYS_RESET#	I	PWR_MGMT
LPC	I/O	LPC_SERIRQ	A50	B50	CB_RESET#	O	PWR_MGMT

	PWR	GND	A51	B51	GND	PWR	
PCIE	O	PCIE_TX5+	A52	B52	PCIE_RX5+	I	PCIE
PCIE	O	PCIE_TX5-	A53	B53	PCIE_RX5-	I	PCIE
GPIO	I	GPI0	A54	B54	GPO1	O	GPIO
PCIE	O	PCIE_TX4+	A55	B55	PCIE_RX4+	I	PCIE
PCIE	O	PCIE_TX4-	A56	B56	PCIE_RX4-	I	PCIE
	PWR	GND	A57	B57	GPO2	O	GPIO
PCIE	O	PCIE_TX3+	A58	B58	PCIE_RX3+	I	PCIE
PCIE	O	PCIE_TX3-	A59	B59	PCIE_RX3-	I	PCIE
	PWR	GND	A60	B60	GND	PWR	
PCIE	O	PCIE_TX2+	A61	B61	PCIE_RX2+	I	PCIE
PCIE	O	PCIE_TX2-	A62	B62	PCIE_RX2-	I	PCIE
GPIO	I	GPI1	A63	B63	GPO3	O	GPIO
PCIE	O	PCIE_TX1+	A64	B64	PCIE_RX1+	I	PCIE
PCIE	O	PCIE_TX1-	A65	B65	PCIE_RX1-	I	PCIE
	PWR	GND	A66	B66	WAKE0#	I	PWR_MGMT
GPIO	I	GPI2	A67	B67	WAKE1#	I	PWR_MGMT
PCIE	O	PCIE_TX0+	A68	B68	PCIE_RX0+	I	PCIE
PCIE	O	PCIE_TX0-	A69	B69	PCIE_RX0-	I	PCIE
	PWR	GND	A70	B70	GND	PWR	
LVDS	O	LVDS_A0+	A71	B71	LVDS_B0+	O	LVDS
LVDS	O	LVDS_A0-	A72	B72	LVDS_B0-	O	LVDS
eDP/LVDS	O	eDP_TX1+/LVDS_A1+	A73	B73	LVDS_B1+	O	LVDS
eDP/LVDS	O	eDP_TX1-/LVDS_A1-	A74	B74	LVDS_B1-	O	LVDS
eDP/LVDS	O	eDP_TX0+/LVDS_A2+	A75	B75	LVDS_B2+	O	LVDS
eDP/LVDS	O	eDP_TX0-/LVDS_A2-	A76	B76	LVDS_B2-	O	LVDS
eDP/LVDS	O	eDP/LVDS_VDD_EN	A77	B77	LVDS_B3+	O	LVDS
LVDS	O	LVDS_A3+	A78	B78	LVDS_B3-	O	LVDS
LVDS	O	LVDS_A3-	A79	B79	eDP/LVDS_BKLT_EN	O	eDP/LVDS
	PWR	GND	A80	B80	GND	PWR	

LVDS	O	LVDS_A_CK+	A81	B81	LVDS_B_CK+	O	LVDS
LVDS	O	LVDS_A_CK-	A82	B82	LVDS_B_CK-	O	LVDS
eDP/LVDS	I/O	eDP_AUX+/LVDS_I2C_CK	A83	B83	eDP/LVDS_BKLT_CTRL	O	LVDS
eDP/LVDS	I/O	eDP_AUX-/LVDS_I2C_DAT	A84	B84	+5V_A	PWR	
GPIO	I	GPI3	A85	B85	+5V_A	PWR	
	N.A.	N.C.	A86	B86	+5V_A	PWR	
eDP	I	eDP_HPD	A87	B87	+5V_A	PWR	
PCIE	O	PCIE_CLK_REF+	A88	B88	BIOS_DIS1#	I	SPI
PCIE	O	PCIE_CLK_REF-	A89	B89	VGA_RED	O	VGA
	PWR	GND	A90	B90	GND	PWR	
SPI	O	SPI_POWER	A91	B91	VGA_GRN	O	VGA
SPI	I	SPI_MISO	A92	B92	VGA_BLU	O	VGA
GPIO	O	GPO0	A93	B93	VGA_HSYNC	O	VGA
SPI	O	SPI_CLK	A94	B94	VGA_VSYNC	O	VGA
SPI	O	SPI_MOSI	A95	B95	VGA_I2C_CK	I/O	VGA
MISC	I	TPM_PP	A96	B96	VGA_I2C_DAT	I/O	VGA
TYPE	N.A.	TYPE10#: N.C.	A97	B97	SPI_CS#	O	SPI
	N.A.	SER0_TX	A98	B98	N.C.	N.A.	
	N.A.	SER0_RX	A99	B99	N.C.	N.A.	
	PWR	GND	A100	B100	GND	PWR	
	N.A.	SER1_TX	A101	B101	FAN_PWNOUT	O	MISC
	N.A.	SER1_RX	A102	B102	FAN_TACHIN	I	MISC
PWR_MGMT	I	LID#	A103	B103	SLEEP#	I	PWR_MGMT
	PWR	+12V_S	A104	B104	+12V_S	PWR	
	PWR	+12V_S	A105	B105	+12V_S	PWR	
	PWR	+12V_S	A106	B106	+12V_S	PWR	
	PWR	+12V_S	A107	B107	+12V_S	PWR	
	PWR	+12V_S	A108	B108	+12V_S	PWR	
	PWR	+12V_S	A109	B109	+12V_S	PWR	
	PWR	GND	A110	B110	GND	PWR	

COM Express® Connector CD - CN6							
		ROW C			ROW D		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	C1	D1	GND	PWR	
	PWR	GND	C2	D2	GND	PWR	
USB	I	USB_SSRX0-	C3	D3	USB_SSTX0-	O	USB
USB	I	USB_SSRX0+	C4	D4	USB_SSTX0+	O	USB
	PWR	GND	C5	D5	GND	PWR	
USB	I	USB_SSRX1-	C6	D6	USB_SSTX1-	O	USB
USB	I	USB_SSRX1+	C7	D7	USB_SSTX1+	O	USB
	PWR	GND	C8	D8	GND	PWR	
USB	I	USB_SSRX2-	C9	D9	USB_SSTX2-	O	USB
USB	I	USB_SSRX2+	C10	D10	USB_SSTX2+	O	USB
	PWR	GND	C11	D11	GND	PWR	
USB	I	USB_SSRX3-	C12	D12	USB_SSTX3-	O	USB
USB	I	USB_SSRX3+	C13	D13	USB_SSTX3+	O	USB
	PWR	GND	C14	D14	GND	PWR	
	N.A.	N.C.	C15	D15	DDI1_CTRLCLK_AUX+	I/O	DDI
	N.A.	N.C.	C16	D16	DDI1_CTRLDATA_AUX-	I/O	DDI
	N.A.	N.C.	C17	D17	N.C.	N.A.	
	N.A.	N.C.	C18	D18	N.C.	N.A.	
PCIE	I	PCIE_RX6+	C19	D19	PCIE_TX6+	O	PCIE
PCIE	I	PCIE_RX6-	C20	D20	PCIE_TX6-	O	PCIE
	PWR	GND	C21	D21	GND	PWR	
	N.A.	N.C.	C22	D22	N.C.	N.A.	
	N.A.	N.C.	C23	D23	N.C.	N.A.	
DDI	I	DDI1_HPD	C24	D24	N.C.	N.A.	
	N.A.	N.C.	C25	D25	N.C.	N.A.	
	N.A.	N.C.	C26	D26	DDI1_PAIR0+	O	DDI

	N.A.	N.C.	C27	D27	DDI1_PAIR0-	O	DDI
	N.A.	N.C.	C28	D28	N.C.	N.A.	
	N.A.	N.C.	C29	D29	DDI1_PAIR1+	O	DDI
	N.A.	N.C.	C30	D30	DDI1_PAIR1-	O	DDI
	PWR	GND	C31	D31	GND	PWR	
DDI	I/O	DDI2_CTRLCLK_AUX+	C32	D32	DDI1_PAIR2+	O	DDI
DDI	I/O	DDI2_CTRLDATA_AUX-	C33	D33	DDI1_PAIR2-	O	DDI
DDI	I	DDI2_DDC_AUX_SEL	C34	D34	DDI1_DDC_AUX_SEL	I	DDI
	N.A.	N.C.	C35	D35	N.C.	N.A.	
DDI	I/O	DDI3_CTRLCLK_AUX+	C36	D36	DDI1_PAIR3+	O	DDI
DDI	I/O	DDI3_CTRLDATA_AUX-	C37	D37	DDI1_PAIR3-	O	DDI
DDI	I	DDI3_DDC_AUX_SEL	C38	D38	N.C.	N.A.	
DDI	O	DDI3_PAIR0+	C39	D39	DDI2_PAIR0+	O	DDI
DDI	O	DDI3_PAIR0-	C40	D40	DDI2_PAIR0-	O	DDI
	PWR	GND	C41	D41	GND	PWR	
DDI	O	DDI3_PAIR1+	C42	D42	DDI2_PAIR1+	O	DDI
DDI	O	DDI3_PAIR1-	C43	D43	DDI2_PAIR1-	O	DDI
DDI	I	DDI3_HPD	C44	D44	DDI2_HPD	I	DDI
	N.A.	N.C.	C45	D45	N.C.	N.A.	
DDI	O	DDI3_PAIR2+	C46	D46	DDI2_PAIR2+	O	DDI
DDI	O	DDI3_PAIR2-	C47	D47	DDI2_PAIR2-	O	DDI
	N.A.	N.C.	C48	D48	N.C.	N.A.	
DDI	O	DDI3_PAIR3+	C49	D49	DDI2_PAIR3+	O	DDI
DDI	O	DDI3_PAIR3-	C50	D50	DDI2_PAIR3-	O	DDI
	PWR	GND	C51	D51	GND	PWR	
PEG	I	PEG_RX0+	C52	D52	PEG_TX0+	O	PEG
PEG	I	PEG_RX0-	C53	D53	PEG_TX0-	O	PEG
TYPE	N.A.	TYPE0#: N.C.	C54	D54	PEG_LANE_RV#	I	PEG
PEG	I	PEG_RX1+	C55	D55	PEG_TX1+	O	PEG
PEG	I	PEG_RX1-	C56	D56	PEG_TX1-	O	PEG

TYPE	N.A.	TYPE1#: N.C.	C57	D57	TYPE2#: GND	N.A.	TYPE
PEG	I	PEG_RX2+	C58	D58	PEG_TX2+	O	PEG
PEG	I	PEG_RX2-	C59	D59	PEG_TX2-	O	PEG
	PWR	GND	C60	D60	GND	PWR	
PEG	I	PEG_RX3+	C61	D61	PEG_TX3+	O	PEG
PEG	I	PEG_RX3-	C62	D62	PEG_TX3-	O	PEG
	N.A.	N.C.	C63	D63	N.C.	N.A.	
	N.A.	N.C.	C64	D64	N.C.	N.A.	
PEG	I	PEG_RX4+	C65	D65	PEG_TX4+	O	PEG
PEG	I	PEG_RX4-	C66	D66	PEG_TX4-	O	PEG
	N.A.	N.C.	C67	D67	GND	PWR	
PEG	I	PEG_RX5+	C68	D68	PEG_TX5+	O	PEG
PEG	I	PEG_RX5-	C69	D69	PEG_TX5-	O	PEG
	PWR	GND	C70	D70	GND	PWR	
PEG	I	PEG_RX6+	C71	D71	PEG_TX6+	O	PEG
PEG	I	PEG_RX6-	C72	D72	PEG_TX6-	O	PEG
	PWR	GND	C73	D73	GND	PWR	
PEG	I	PEG_RX7+	C74	D74	PEG_TX7+	O	PEG
PEG	I	PEG_RX7-	C75	D75	PEG_TX7-	O	PEG
	PWR	GND	C76	D76	GND	PWR	
	N.A.	N.C.	C77	D77	N.C.	N.A.	
PEG	I	PEG_RX8+	C78	D78	PEG_TX8+	O	PEG
PEG	I	PEG_RX8-	C79	D79	PEG_TX8-	O	PEG
	PWR	GND	C80	D80	GND	PWR	
PEG	I	PEG_RX9+	C81	D81	PEG_TX9+	O	PEG
PEG	I	PEG_RX9-	C82	D82	PEG_TX9-	O	PEG
	N.A.	N.C.	C83	D83	N.C.	N.A.	
	PWR	GND	C84	D84	GND	PWR	
PEG	I	PEG_RX10+	C85	D85	PEG_TX10+	O	PEG
PEG	I	PEG_RX10-	C86	D86	PEG_TX10-	O	PEG

	PWR	GND	C87	D87	GND	PWR	
PEG	I	PEG_RX11+	C88	D88	PEG_TX11+	O	PEG
PEG	I	PEG_RX11-	C89	D89	PEG_TX11-	O	PEG
	PWR	GND	C90	D90	GND	PWR	
PEG	I	PEG_RX12+	C91	D91	PEG_TX12+	O	PEG
PEG	I	PEG_RX12-	C92	D92	PEG_TX12-	O	PEG
	PWR	GND	C93	D93	GND	PWR	
PEG	I	PEG_RX13+	C94	D94	PEG_TX13+	O	PEG
PEG	I	PEG_RX13-	C95	D95	PEG_TX13-	O	PEG
	PWR	GND	C96	D96	GND	PWR	
	N.A.	N.C.	C97	D97	N.C.	N.A.	
PEG	I	PEG_RX14+	C98	D98	PEG_TX14+	O	PEG
PEG	I	PEG_RX14-	C99	D99	PEG_TX14-	O	PEG
	PWR	GND	C100	D100	GND	PWR	
PEG	I	PEG_RX15+	C101	D101	PEG_TX15+	O	PEG
PEG	I	PEG_RX15-	C102	D102	PEG_TX15-	O	PEG
	PWR	GND	C103	D103	GND	PWR	
	PWR	+12V_S	C104	D104	+12V_S	PWR	
	PWR	+12V_S	C105	D105	+12V_S	PWR	
	PWR	+12V_S	C106	D106	+12V_S	PWR	
	PWR	+12V_S	C107	D107	+12V_S	PWR	
	PWR	+12V_S	C108	D108	+12V_S	PWR	
	PWR	+12V_S	C109	D109	+12V_S	PWR	
	PWR	GND	C110	D110	GND	PWR	

3.2.3.1 Audio interface signals

The COMe-953-BT6 module supports HD audio format, thanks to native support offered by the processor to this audio codec standard. Up to 3 HD audio codecs on the carrier board can be supported.

Here following the signals related to HD Audio interface:

HDA_SYNC: HD Audio Serial Bus Synchronization. 48kHz fixed rate output from the module to the Carrier board, electrical level +3.3V_S.

HDA_RST#: HD Audio Codec Reset. Active low signal, output from the module to the Carrier board, electrical level +3.3V_S.

HDA_BITCLK: HD Audio Serial Bit Clock signal. 24MHz serial data clock generated by the Intel HD audio controller, output from the module to the Carrier board, electrical level +3.3V_S.

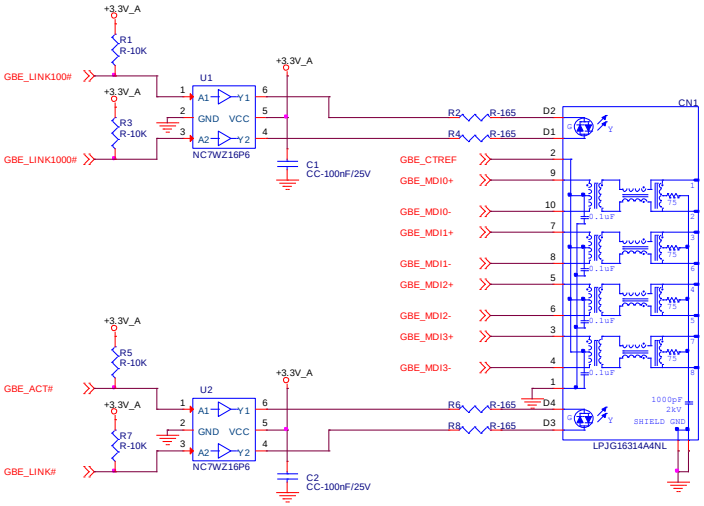
HDA_SDOUT: HD Audio Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_SDIN[0..2]: HD Audio Serial Data In signal. Inputs to the module from the Codec(s) placed on the Carrier board, electrical level +3.3V_S.

The first four signals have to be connected to all the HD Audio codecs present on the carrier board. For each Codec, only one HDA_SDIN signal must be used. Please refer to the chosen Codecs' Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.3.2 Gigabit Ethernet signals

The Gigabit Ethernet interface is realised, on COMe-953-BT6 module, using an Intel® I217 Gigabit Ethernet controller, which is interfaced to the PCH through PCI-express lane #6.



Here following the signals involved in Gigabit Ethernet management

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE_ACT#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_A.

GBE0_LINK#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_A.

GBE0_LINK100#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_A.

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator, Active Low Output signal, electrical level +3.3V_A.

These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected. Please look to the schematic on the left as an example of implementation of Gigabit Ethernet connector. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. Intel® I217 Gigabit Ethernet controller, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on COM Express® connector AB.

All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.r.l. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

3.2.3.3 S-ATA signals

The Intel® QM87 Chipset offers four S-ATA interfaces. All of them are carried out on COM Express® connector AB.

SATA ports #0 and #1 support 1.5 Gbps, 3.0 Gbps and 6.0 Gbps data rates. SATA ports #2 and #3 support 1.5 Gbps and 3.0 Gbps data rates.

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair.

SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair.

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair.

SATA2_TX+/SATA2_TX-: Serial ATA Channel #2 Transmit differential pair.

SATA2_RX+/SATA2_RX-: Serial ATA Channel #2 Receive differential pair.

SATA3_TX+/SATA3_TX-: Serial ATA Channel #3 Transmit differential pair.

SATA3_RX+/SATA3_RX-: Serial ATA Channel #3 Receive differential pair.

SATA_ACT#: Serial ATA Activity Led. Active low output signal at +3.3V_S voltage.

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

On the carrier board, these signals can be carried out directly to the SATA connectors.

3.2.3.4 PCI Express interface signals

COMe-953-BT6 can offer externally seven PCI Express lane, which are directly managed by the Intel® QM87 Chipset.

PCI express Gen 2.0 (5Gbps) is supported.

PCI Express Lanes #0 ÷ #3 can be managed as one port PCI-e x4, two ports PCI-e x2, one port PCI-e x2 plus two ports PCI-e x1 or four ports PCI-e x1.

The other PCI Express Lanes can be managed only as single PCI-e x1 lanes.

Here following the signals involved in PCI express management (Lane #6 is available on connector CD, the other lanes are available on connector AB).

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair.

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE1_TX+/PCIE1_TX-: PCI Express lane #1, Transmitting Output Differential pair

PCIE1_RX+/PCIE1_RX-: PCI Express lane #1, Receiving Input Differential pair

PCIE2_TX+/PCIE2_TX-: PCI Express lane #2, Transmitting Output Differential pair

PCIE2_RX+/PCIE2_RX-: PCI Express lane #2, Receiving Input Differential pair

PCIE3_TX+/PCIE3_TX-: PCI Express lane #3, Transmitting Output Differential pair

PCIE3_RX+/PCIE3_RX-: PCI Express lane #3, Receiving Input Differential pair

PCIE4_TX+/PCIE4_TX-: PCI Express lane #4, Transmitting Output Differential pair

PCIE4_RX+/PCIE4_RX-: PCI Express lane #4, Receiving Input Differential pair

PCIE5_TX+/PCIE5_TX-: PCI Express lane #5, Transmitting Output Differential pair

PCIE5_RX+/PCIE5_RX-: PCI Express lane #5, Receiving Input Differential pair

PCIE6_TX+/PCIE6_TX-: PCI Express lane #6, Transmitting Output Differential pair

PCIE6_RX+/PCIE6_RX-: PCI Express lane #6, Receiving Input Differential pair

PCIE_CLK_REF+/ PCIE_CLK_REF-: PCI Express 100MHz Reference Clock, Differential Pair. Please consider that only one reference clock is supplied, while there are seven different PCI express lanes and one PEG. When more than one PCI Express lane is used on the carrier board, then a zero-delay buffer must be used to replicate the reference clock to all the devices.

3.2.3.5 PEG interface signals

In addition to the seven PCI express lanes, described in the previous paragraph, the COMe-953-BT6 module offer a PCI-Express x16 graphics interface (PEG), which can be used for connection of external graphics cards. Such an interface is directly managed by the Intel® iCore processor's embedded GPUs.

PCI express Gen 3.0 is supported.

Here following the signals involved in PEG management.

PEG_TX[0..15]+/PEG_TX[0..15]-: PCI Express Graphics lane #0 ÷ #15, Transmitting Output Differential pairs.

PEG_RX[0..15]+/PEG_RX[0..15]-: PCI Express Graphics lane #0 ÷ #15, Receiving Output Differential pairs.

PEG_LANE_RV#: PCI Express Graphics lane reversal input strap. This signal must be driven low, on the carrier board, only in case it is necessary to reverse the lane order of PEG interface. It must be left unconnected if lane reversal is not necessary.

3.2.3.6 Express Card interface signals

According to Com Express® specifications, the COMe-953-BT6 module offers the signals necessary for management of up to two Express Cards, managed by the module's embedded microcontroller.

The signals involved in Express Card management are the following.

EXCD0_CPPE#: PCI Express Capable Card slot #0 Request, +3.3V_S Active Low input signal.

EXCD0_PERST#: Express Card slot#0 reset, +3.3V_S Active Low output signal.

EXCD1_CPPE#: PCI Express Capable Card slot #1 Request, +3.3V_S Active Low input signal.

EXCD1_PERST#: Express Card slot #1 reset, +3.3V_S Active Low output signal.

3.2.3.7 USB interface signals

Intel® QM87 Chipset embeds an xHCI controller, which is able to manage up to four Superspeed ports (i.e. USB 3.0 compliant) and up to fourteen USB 1.x / 2.0 Host ports, or, alternatively, two EHCI Controllers, which are able to manage only the USB 1.x / USB 2.0 host ports functionalities. Via BIOS settings it is possible to enable or disable the xHCI controller, therefore enabling USB 3.0 functionalities or leaving only USB 1.1 and USB 2.0 support.

All USB 2.0 ports are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Here following the signals related to USB interfaces.

USB_0+/USB_0-: Universal Serial Bus Port #0 bidirectional differential pair.

USB_1+/USB_1-: Universal Serial Bus Port #1 bidirectional differential pair.

USB_2+/USB_2-: Universal Serial Bus Port #2 bidirectional differential pair.

USB_3+/USB_3-: Universal Serial Bus Port #3 bidirectional differential pair.

USB_4+/USB_4-: Universal Serial Bus Port #4 bidirectional differential pair.

USB_5+/USB_5-: Universal Serial Bus Port #5 bidirectional differential pair.

USB_6+/USB_6-: Universal Serial Bus Port #6 bidirectional differential pair.

USB_7+/USB_7-: Universal Serial Bus Port #7 bidirectional differential pair.

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair; it is managed by the xHCI controller only.

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair; it is managed by the xHCI controller only.

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair; it is managed by the xHCI controller only.

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair; it is managed by the xHCI controller only.

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair; it is managed by the xHCI controller only.

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair; it is managed by the xHCI controller only.

USB_SSRX3+/USB_SSRX3-: USB Super Speed Port #3 receive differential pair; it is managed by the xHCI controller only.

USB_SSTX3+/USB_SSTX3-: USB Super Speed Port #3 transmit differential pair; it is managed by the xHCI controller only.

USB_0_1_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port#0 and #1 of COMe-953-BT6 module

USB_2_3_OC#: USB Over Current Detect Input. Active Low Input signa.l, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Ports #2 and #3 of COMe-953-BT6 module.

USB_4_5_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #4 and/or #5 of COMe-953-BT6 module.

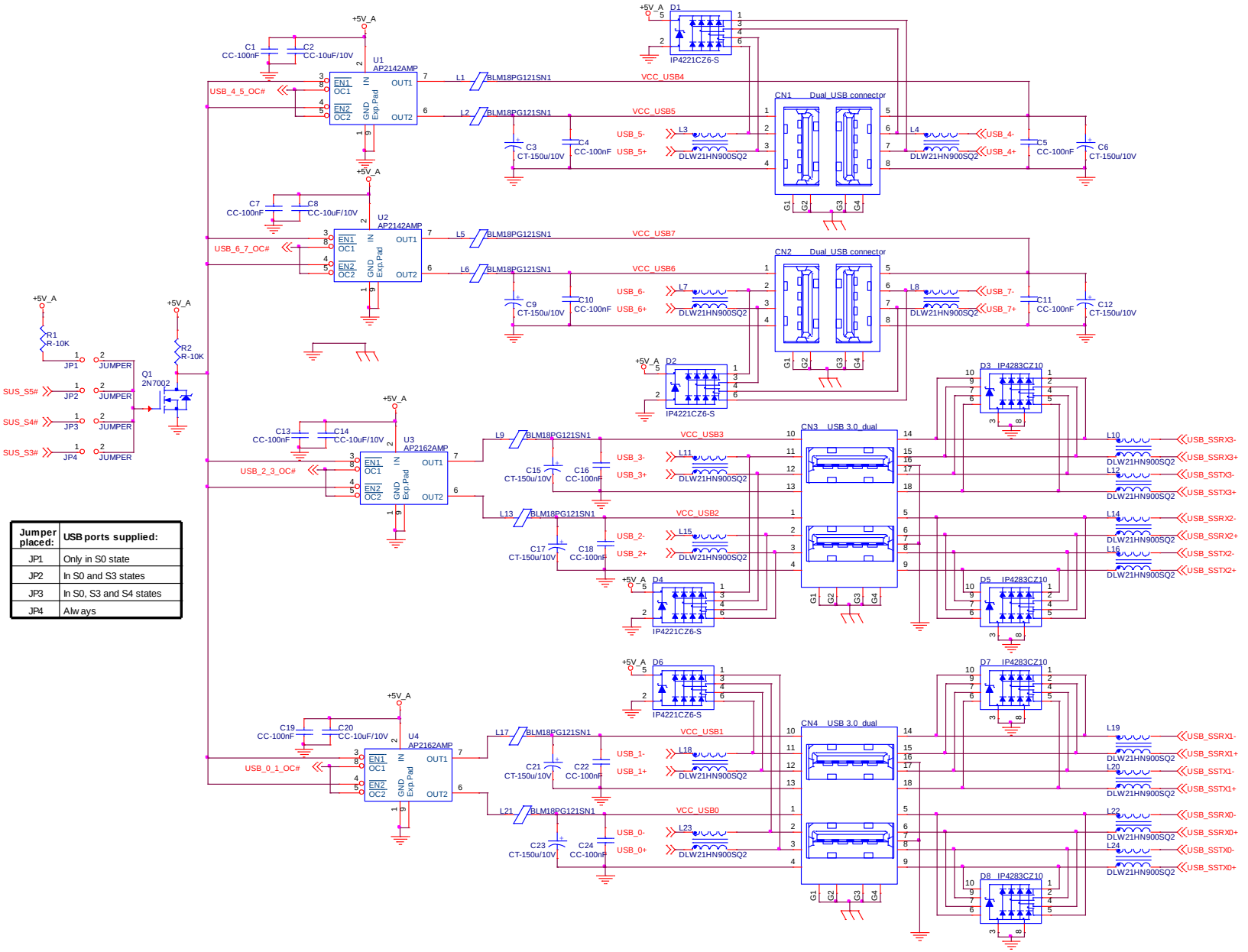
USB_6_7_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #6 and/or #7 of COMe-953-BT6 module.

100nF AC series decoupling capacitors are placed on each receiving line of USB Super speed differential pairs.

Please notice that for correct management of Overcurrent signals, power distribution switches are needed on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

The schematics in the following page show an example of implementation on the Carrier Board. In there, USB ports #4, #5, #6 and #7 are carried out to standard USB 2.0 Type A receptacles, while USB 2.0 port #0, #1, #2 and 3 along with the corresponding Superspeed USB ports, are carried to standard USB 3.0 Type A receptacles. Always remember that, for correct implementation of USB 3.0 connections, any Superspeed port must be paired with corresponding number of USB 2.0 port (i.e. USB 2.0 port#0 must be paired with USB 3.0 port #0 and so on).



Jumper placed:	USB ports supplied:
JP1	Only in S0 state
JP2	In S0 and S3 states
JP3	In S0, S3 and S4 states
JP4	Always

3.2.3.8 LVDS Flat Panel signals

The Intel® iCore 4th generation family of CPUs offers a native embedded Display Port (eDP). Conversely, the LVDS interface, which is frequently used in many application fields, is not directly supported by these CPUs.

For this reason, considering that LVDS interface can be multiplexed on the same pin with the eDP interface, on COMe-953-BT6 module can be implemented an eDP to LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hz (dual channel mode).

> **!** Please remember that LVDS interface is not native for iCore 4th generation family of CPUs, it is derived from an optional eDP-to-LVDS bridge. Depending on the factory option purchased, on the same pins it is possible to have available LVDS first channel **or** eDP interface.
>
> Please take care of specifying if LVDS interface or eDP is needed, before placing an order of COMe-953-BT6 module.

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Channel #A differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Channel #A differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Channel #A differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Channel #A differential data pair #3.

LVDS_A_CLK+/LVDS_A_CLK-: LVDS Channel #A differential clock.

LVDS_B0+/LVDS_B0-: LVDS Channel #B differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Channel #B differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Channel #B differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Channel #B differential data pair #3.

LVDS_B_CLK+/LVDS_B_CLK-: LVDS Channel #B differential Clock

LVDS_VDD_EN: +3.3V_S electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display.

LVDS_BKLT_EN: +3.3V_S electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display.

LVDS_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

LVDS_I2C_DAT: DisplayID DDC Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

LVDS_I2C_CK: DisplayID DDC Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

Please be aware that External EDID through LVDS_I2C-xxx signals is actually not supported by COMe-953-BT6 module

3.2.3.9 Embedded Display Port (eDP) signals

As described in the previous paragraph, the Intel® iCore 4th generation family of CPUs offers a native 2-lanes embedded Display Port (eDP) interface.

When the board is not configured with the eDP-to-LVDS bridge, then on COM Express connector AB is available this eDP interface, which allows supporting displays with a resolution up to 1920 x 1200 @ 60Hz.

Here following the signals related to eDP management:

eDP_TX0+/eDP_TX0-: eDP channel differential data pair #0. AC coupled though 100nF ceramic capacitors on both lines.

eDP_TX1+/eDP_TX1-: eDP channel differential data pair #1. AC coupled though 100nF ceramic capacitors on both lines.

eDP_AUX+/eDP_AUX-: eDP channel differential auxiliary channel. AC coupled though 100nF ceramic capacitors on both lines.

eDP_HPD: eDP channel Hot Plug Detect. Active High Signal, +3.3V_S electrical level input with 100kΩ pull-down resistor.

eDP_VDD_EN: +3.3V_S electrical level output, Panel Power Enable signal. It can be used to turn On/Off the connected display.

eDP_BKLT_EN: +3.3V_S electrical level output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected display.

eDP_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

3.2.3.10 LPC interface signals

According to COM Express® specifications rel. 2.0, on the on COM Express connector AB there are 8 pins that are used for implementation of Low Pin Count (LPC) Bus interface.

The following signals are available:

LPC_AD[0÷3]: LPC address, command and data bus, bidirectional signal, +3.3V_S electrical level.

LPC_CLK: LPC Clock Output line, +3.3V_S electrical level. Since only a clock line is available, if more LPC devices are available on the carrier board, then it is necessary to provide for a zero-delay clock buffer to connect all clock lines to the single clock output of COM Express module.

LPC_DRQ[0÷1]#: LPC Serial DMA request, +3.3V_S electrical level input signals, active low. These signals are used to request DMA or bus master access.

LPC_FRAME#: LPC Frame indicator, active low output line, +3.3V_S electrical level. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

LPC_SERIRQ: LPC Serialised IRQ request, bidirectional line, +3.3V_S electrical level. This signal is used only by peripherals requiring Interrupt support.

3.2.3.11 SPI interface signals

The Intel® QM87 Chipset offers also one dedicated controller for Serial Peripheral Interface (SPI), which can be used for connection of Serial Flash devices. Please be aware that this interface can be used exclusively to support platform firmware (BIOS).

Signals involved with SPI management are the following:

SPI_CS#: SPI Chip select, active low output signal (+3.3V_S electrical level). It can be internally multiplexed, depending on configuration of BIOS Disable x# signals, to be connected to the chipset's SPI_CS0# or SPI_CS1# signal

SPI_MISO: SPI Master In Slave Out, Input to COM Express® module from SPI devices embedded on the Carrier Board. Electrical level +3.3V_S.

SPI_MOSI: SPI Master Out Slave In, Output from COM Express® module to SPI devices embedded on the Carrier Board. Electrical level +3.3V_S.

SPI_CLK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +3.3V_S. Supported clock frequencies are 20, 33 and 50 MHz.

SPI_POWER: Power Supply Output for carrier board's SPI devices. Electrical level +3.3V_S.

BIOS_DIS[0÷1]#: BIOS Disable strap signals. These two signals are inputs of the COM Express® Module, that on the carrier board can be left floating or pulled down in order to select which SPI Flash device has to be used for module's boot. Please refer to table 4.13 of COM Express® Module Base Specifications rel. 2.1 for the meaning of possible configurations of these two signals.

3.2.3.12 Analog VGA interface

The Intel® QM87 Chipset offers one Analog display interface, which can be used for the connection of older VGA/CRT displays.

Signals dedicated to VGA interface are are the following:

VGA_RED: QM87 Chipset's internal DAC's Red Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_GRN: QM87 Chipset's internal DAC's Green Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_BLU: QM87 Chipset's internal DAC's Blue Signal video output. A 150Ω pull-down resistor is placed on the line.

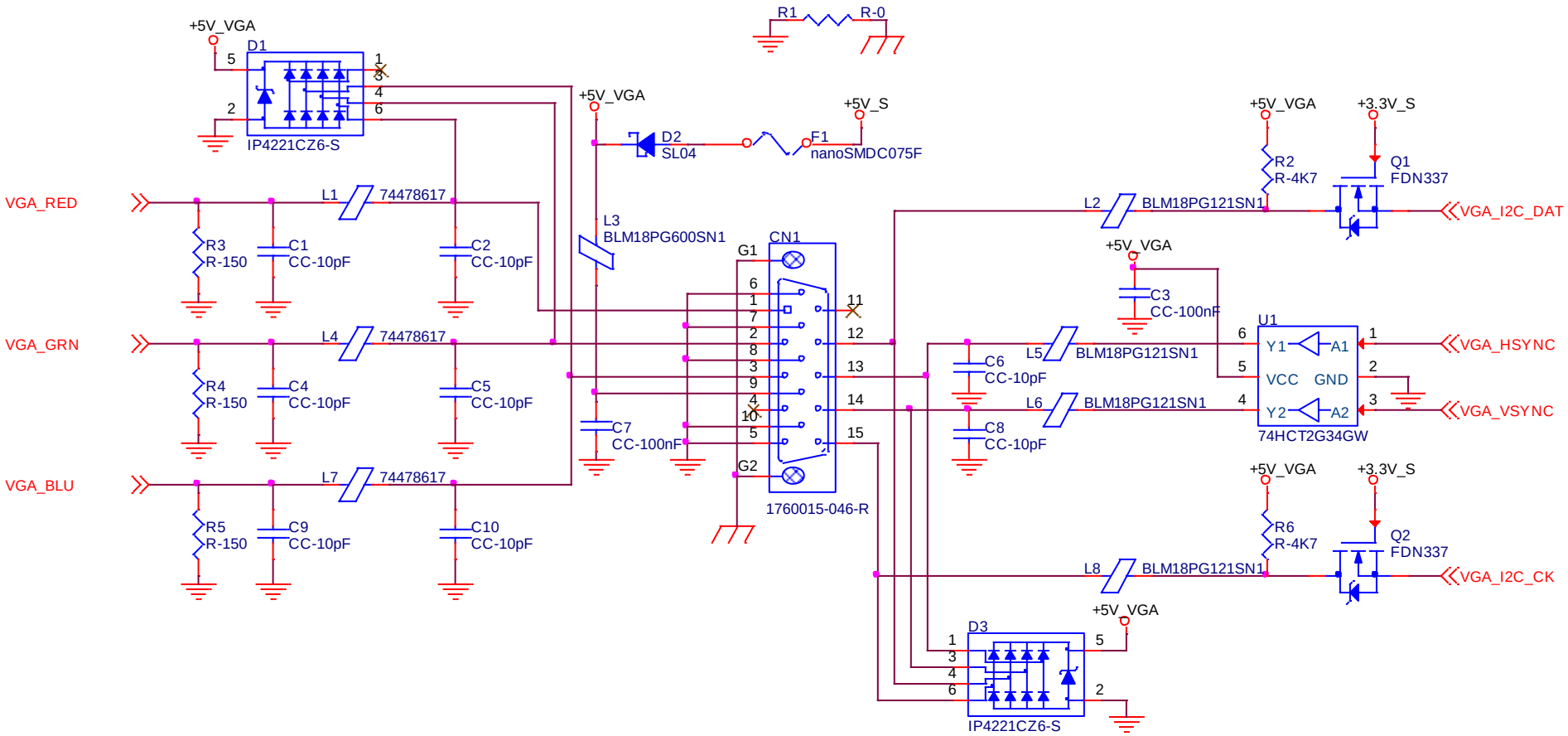
VGA_HSYNC: QM87 Chipset's internal DAC's Horizontal Synchronization output signal.

VGA_VSYNC: QM87 Chipset's internal DAC's Vertical Synchronization output signal.

VGA_I2C_CK: internal DAC's DDC Clock line for VGA displays detection. Output signal, electrical level +3.3V_S with 2K2Ω pull-up resistor.

VGA_I2C_DAT: internal DAC's DDC Clock line for VGA displays detection. Bidirectional signal, electrical level +3.3V_S with 2K2Ω pull-up resistor.

Please be aware that for the connection to external VGA displays, on the carrier board it is necessary to provide for filters and ESD protection like in the following example schematics.


+5V_VGA
D1
IP4221CZ6-S
R1
R-0
D2
SL04
F1
nanoSMDC075F
+5V_S
L3
BLM18PG600SN1
CN1
1760015-046-R
VGA_RED
VGA_GRN
VGA_BLU
L1
L4
L7
74478617
R3
R-150
C1
CC-10pF
C2
CC-10pF
R4
R-150
C4
CC-10pF
C5
CC-10pF
R5
R-150
C9
CC-10pF
C10
CC-10pF
C7
CC-100nF
L2
L5
L6
L8
BLM18PG121SN1
R2
R-4K7
Q1
FDN337
+3.3V_S
VGA_I2C_DAT
C3
CC-100nF
C6
CC-10pF
C8
CC-10pF
U1
74HCT2G34GW
VGA_HSYNC
VGA_VSYNC
R6
R-4K7
Q2
FDN337
VGA_I2C_CK
D3
IP4221CZ6-S

3.2.3.13 Digital Display interfaces

The Intel® HD Graphics 4600 controller, embedded inside the Intel® iCore 4th generation CPUs, offer three Digital Display interfaces, which can be used for the implementation, on the carrier board, of HDMI/DVI or Multimode Display Port interfaces.

Switching between HDMI/DVI (or, more correctly, TMDS) and Display Port is dynamic, i.e. the interfaces coming out from COM Express® module can be used to implement a multimode Display Port interface (and in this way only AC coupling capacitors are needed on the carrier board) or a HDMI/DVI interface (an in this case TMDS level shifters are needed).

This is reached by multiplexing DP/HDMI interfaces on the same pins.

Depending by the interface chosen, therefore, on COM Express connector CD there will be available the following signals:

Digital Display Interfaces - Pin multiplexing					
		Multimode Display Port mode		TMDS (HDMI/DVI) mode	
Pin nr.	Pin name	Signal	Description	Signal	Description
D26	DDI1_PAIR0+	DP1_LANE0+	DP1 Differential pair #0 non-inverting line	TMDS1_DATA2+	TMDS1 Differential pair #2 non-inverting line
D27	DDI1_PAIR0-	DP1_LANE0-	DP1 Differential pair #0 inverting line	TMDS1_DATA2-	TMDS1 Differential pair #2 inverting line
D29	DDI1_PAIR1+	DP1_LANE1+	DP1 Differential pair #1 non-inverting line	TMDS1_DATA1+	TMDS1 Differential pair #1 non-inverting line
D30	DDI1_PAIR1-	DP1_LANE1-	DP1 Differential pair #1 inverting line	TMDS1_DATA1-	TMDS1 Differential pair #1 inverting line
D32	DDI1_PAIR2+	DP1_LANE2+	DP1 Differential pair #2 non-inverting line	TMDS1_DATA0+	TMDS1 Differential pair #0 non-inverting line
D33	DDI1_PAIR2-	DP1_LANE2-	DP1 Differential pair #2 inverting line	TMDS1_DATA0-	TMDS1 Differential pair #0 inverting line
D36	DDI1_PAIR3+	DP1_LANE3+	DP1 Differential pair #3 non-inverting line	TMDS1_CLK+	TMDS1 Differential clock non-inverting line
D37	DDI1_PAIR3-	DP1_LANE3-	DP1 Differential pair #3 inverting line	TMDS1_CLK-	TMDS1 Differential clock inverting line
C24	DDI1_HPD	DP1_HPD	DP1 Hot Plug Detect signal	HDMI1_HPD	HDMI #1 Hot Plug Detect signal
D15	DDI1_CTRLCLK_AUX+	DP1_AUX+	DP1 Auxiliary channel non-inverting line	HDMI1_CTRLCLK	DDC Clock line for HDMI panel #1.
D16	DDI1_CTRLDATA_AUX-	DP1_AUX-	DP1 Auxiliary channel inverting line	HDMI1_CTRLDATA	DDC Data line for HDMI panel #1.
D34	DDI1_DDC_AUX_SEL	DDI#1 DP or TMDS interface selector: pull this signal low or leave it floating for DP++ interface, pull high (+3.3V_S) for TMDS interface			
D39	DDI2_PAIR0+	DP2_LANE0+	DP2 Differential pair #0 non-inverting line	TMDS2_DATA2+	TMDS2 Differential pair #2 non-inverting line
D40	DDI2_PAIR0-	DP2_LANE0-	DP2 Differential pair #0 inverting line	TMDS2_DATA2-	TMDS2 Differential pair #2 inverting line
D42	DDI2_PAIR1+	DP2_LANE1+	DP2 Differential pair #1 non-inverting line	TMDS2_DATA1+	TMDS2 Differential pair #1 non-inverting line
D43	DDI2_PAIR1-	DP2_LANE1-	DP2 Differential pair #1 inverting line	TMDS2_DATA1-	TMDS2 Differential pair #1 inverting line
D46	DDI2_PAIR2+	DP2_LANE2+	DP2 Differential pair #2 non-inverting line	TMDS2_DATA0+	TMDS2 Differential pair #0 non-inverting line

D47	DDI2_PAIR2-	DP2_LANE2-	DP2 Differential pair #2 inverting line	TMDS2_DATA0-	TMDS2 Differential pair #0 inverting line
D49	DDI2_PAIR3+	DP2_LANE3+	DP2 Differential pair #3 non-inverting line	TMDS2_CLK+	TMDS2 Differential clock non-inverting line
D50	DDI2_PAIR3-	DP2_LANE3-	DP2 Differential pair #3 inverting line	TMDS2_CLK-	TMDS2 Differential clock inverting line
D44	DDI2_HPD	DP2_HPD	DP2 Hot Plug Detect signal	HDMI2_HPD	HDMI #2 Hot Plug Detect signal
C32	DDI2_CTRLCLK_AUX+	DP2_AUX+	DP2 Auxiliary channel non-inverting line	HDMI2_CTRLCLK	DDC Clock line for HDMI panel #2..
C33	DDI2_CTRLDATA_AUX-	DP2_AUX-	DP2 Auxiliary channel inverting line	HDMI2_CTRLDATA	DDC Data line for HDMI panel #2.
C34	DDI2_DDC_AUX_SEL	DDI#2 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_S) for TMDS interface			
C39	DDI3_PAIR0+	DP3_LANE0+	DP3 Differential pair #0 non-inverting line	TMDS3_DATA2+	TMDS3 Differential pair #2 non-inverting line
C40	DDI3_PAIR0-	DP3_LANE0-	DP3 Differential pair #0 inverting line	TMDS3_DATA2-	TMDS3 Differential pair #2 inverting line
C42	DDI3_PAIR1+	DP3_LANE1+	DP3 Differential pair #1 non-inverting line	TMDS3_DATA1+	TMDS3 Differential pair #1 non-inverting line
C43	DDI3_PAIR1-	DP3_LANE1-	DP3 Differential pair #1 inverting line	TMDS3_DATA1-	TMDS3 Differential pair #1 inverting line
C46	DDI3_PAIR2+	DP3_LANE2+	DP3 Differential pair #2 non-inverting line	TMDS3_DATA0+	TMDS3 Differential pair #0 non-inverting line
C47	DDI3_PAIR2-	DP3_LANE2-	DP3 Differential pair #2 inverting line	TMDS3_DATA0-	TMDS3 Differential pair #0 inverting line
C49	DDI3_PAIR3+	DP3_LANE3+	DP3 Differential pair #3 non-inverting line	TMDS3_CLK+	TMDS3 Differential clock non-inverting line
C50	DDI3_PAIR3-	DP3_LANE3-	DP3 Differential pair #3 inverting line	TMDS3_CLK-	TMDS3 Differential clock inverting line
C44	DDI3_HPD	DP3_HPD	DP3 Hot Plug Detect signal	HDMI3_HPD	HDMI #3 Hot Plug Detect signal
C36	DDI3_CTRLCLK_AUX+	DP3_AUX+	DP3 Auxiliary channel non-inverting line	HDMI3_CTRLCLK	DDC Clock line for HDMI panel #3.
C37	DDI3_CTRLDATA_AUX-	DP3_AUX-	DP3 Auxiliary channel inverting line	HDMI3_CTRLDATA	DDC Data line for HDMI panel #3.
C38	DDI3_DDC_AUX_SEL	DDI#3 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_S) for TMDS interface			

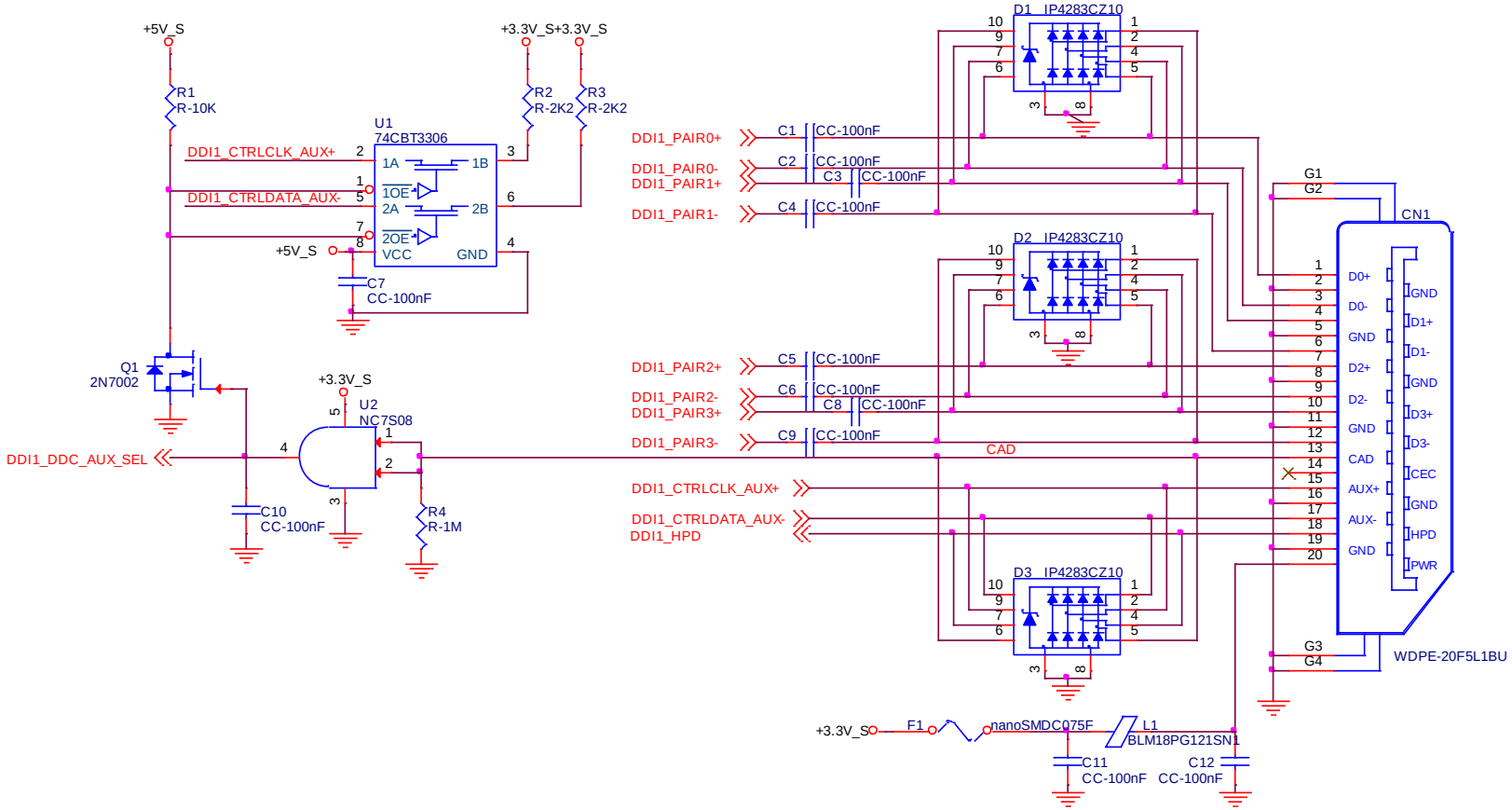
All Hot Plug Detect Input signals (valid both for DP++ and TMDS interface) are +3.3V_S electrical level signal, active high with 1MΩ pull-down resistors.

All HDMI Control signals (CTRLCLK and CTRLDATA) are bidirectional signal, electrical level +3.3V_S with a 100kΩ pull-up resistor

Please be aware that for correct implementation of HDMI/DVI interfaces, it is necessary to implement, on the Carrier board, voltage level shifter for TMDS differential pairs, for Control data/Clock signals and for Hot Plug Detect signal.

Voltage clamping diodes are also highly recommended on all signal lines for ESD suppression.

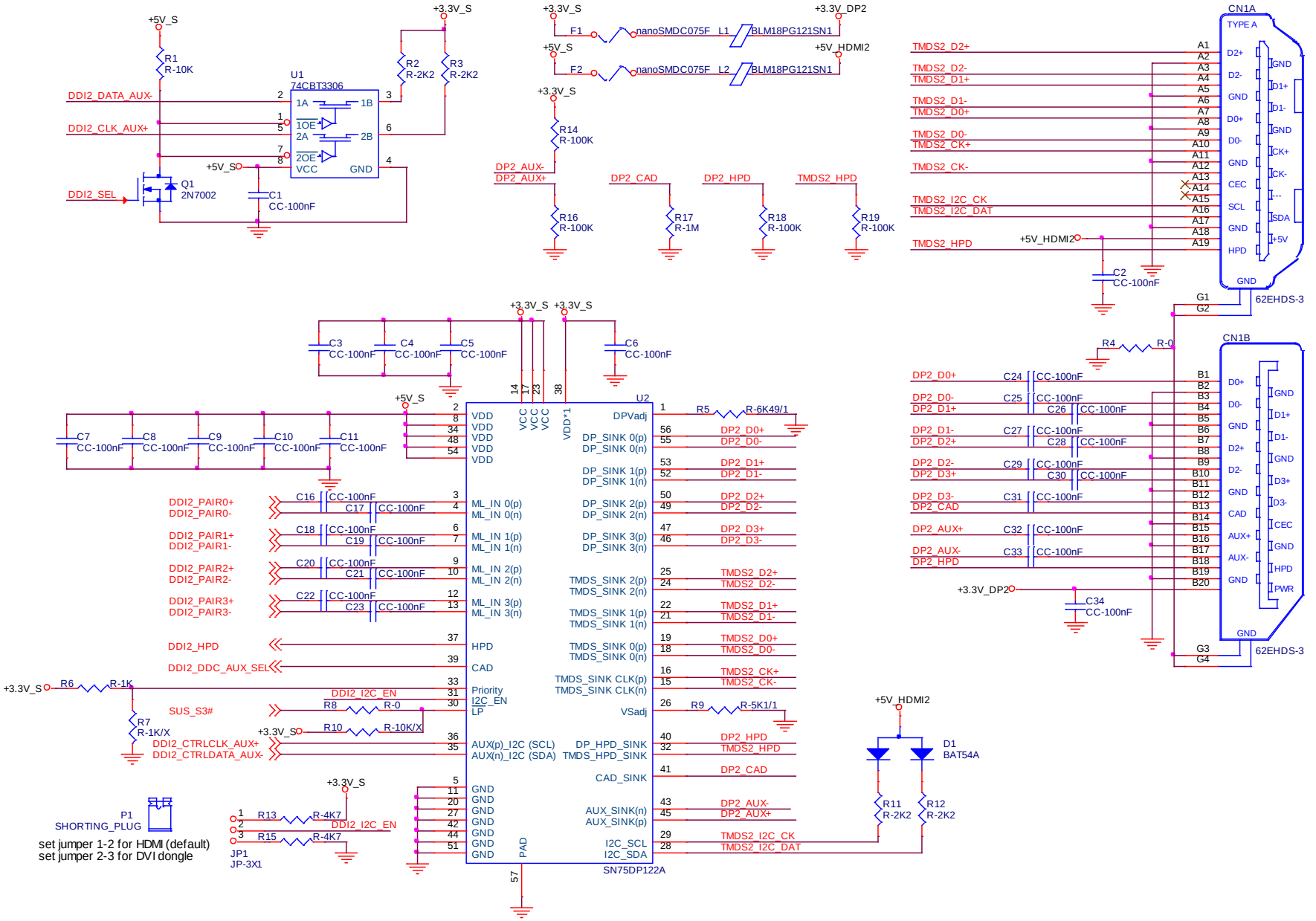
Here following an example of implementation of multimode Display Port on the carrier board. In this example, are used signals related to Digital Display interface #1, but any DDI interface can be used.



The example schematics in the following page, instead, shows the implementation (using DDI interface #2, but any DDI can be used for this purpose) of a double connector DP++ and HDMI, managed using a DisplayPort 1:2 Switch with Integrated TMDS Translator, which provides to TMDS voltage level shifter for HDMI/DVI connection.

By implementing such a schematic, the module can configure itself automatically to work with external HDMI/DVI or multimode Display Port interfaces, depending on the cable connected. In case both an HDMI and a DP are connected, the HDMI interface will take priority automatically. This order can be changed by removing resistor R6 and mounting resistor R7.

The jumper JP1 is used to enable or disable switch's I2C internal registers, for use of TMDS interface, respectively, for HDMI or DVI displays.


+5V_S
+3.3V_S
+3.3V_DP2
+5V_HDMI2
R1
R-10K
R2
R-2K2
R3
R-2K2
U1
74CBT3306
1A
1B
1OE
2A
2B
2OE
VCC
GND
DDI2_DATA_AUX-
DDI2_CLK_AUX+
DDI2_SEL
Q1
2N7002
C1
CC-100nF
F1
F2
nanoSMDC075F
L1
L2
BLM18PG121SN1
R14
R-100K
R16
R-100K
R17
R-1M
R18
R-100K
R19
R-100K
DP2_AUX-
DP2_AUX+
DP2_CAD
DP2_HPD
TMDS2_HPD
CN1A
TYPE A
TMDS2_D2+
TMDS2_D2-
TMDS2_D1+
TMDS2_D1-
TMDS2_D0+
TMDS2_D0-
TMDS2_CK+
TMDS2_CK-
TMDS2_I2C_CK
TMDS2_I2C_DAT
C2
CC-100nF
G1
G2
62EHDS-3
C3
C4
C5
C6
CC-100nF
U2
DPVadj
DP_SINK 0(p)
DP_SINK 0(n)
DP_SINK 1(p)
DP_SINK 1(n)
DP_SINK 2(p)
DP_SINK 2(n)
DP_SINK 3(p)
DP_SINK 3(n)
TMDS_SINK 2(p)
TMDS_SINK 2(n)
TMDS_SINK 1(p)
TMDS_SINK 1(n)
TMDS_SINK 0(p)
TMDS_SINK 0(n)
TMDS_SINK CLK(p)
TMDS_SINK CLK(n)
VSadj
DP_HPD_SINK
TMDS_HPD_SINK
CAD_SINK
AUX_SINK(n)
AUX_SINK(p)
I2C_SCL
I2C_SDA
SN75DP122A
R5
R-6K49/1
R9
R-5K1/1
R4
R-0
CN1B
C7
C8
C9
C10
C11
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
DDI2_PAIR0+
DDI2_PAIR0-
DDI2_PAIR1+
DDI2_PAIR1-
DDI2_PAIR2+
DDI2_PAIR2-
DDI2_PAIR3+
DDI2_PAIR3-
DDI2_HPD
DDI2_DDC_AUX_SEL
SUS_S3#
DDI2_I2C_EN
DDI2_CTRLCLK_AUX+
DDI2_CTRLDATA_AUX-
R6
R-1K
R7
R-1K/X
R8
R-0
R10
R-10K/X
P1
SHORTING_PLUG
set jumper 1-2 for HDMI (default)
set jumper 2-3 for DVI dongle
R13
R-4K7
R15
R-4K7
JP1
JP-3X1
D1
BAT54A
R11
R-2K2
R12
R-2K2

3.2.3.14 UART interface signals

According to COM Express® Rel. 2.1 specifications, since the COMe-953-BT6 is a Type 6 module, it can offer two UART interfaces, which are managed by the EXAR XR28V382 Dual LPC UART.

Here following the signals related to UART interface:

SER0_TX: UART Interface #0, Serial data Transmit (output) line, 3.3V_S electrical level.

SER0_RX: UART Interface #0, Serial data Receive (input) line, 3.3V_S electrical level.

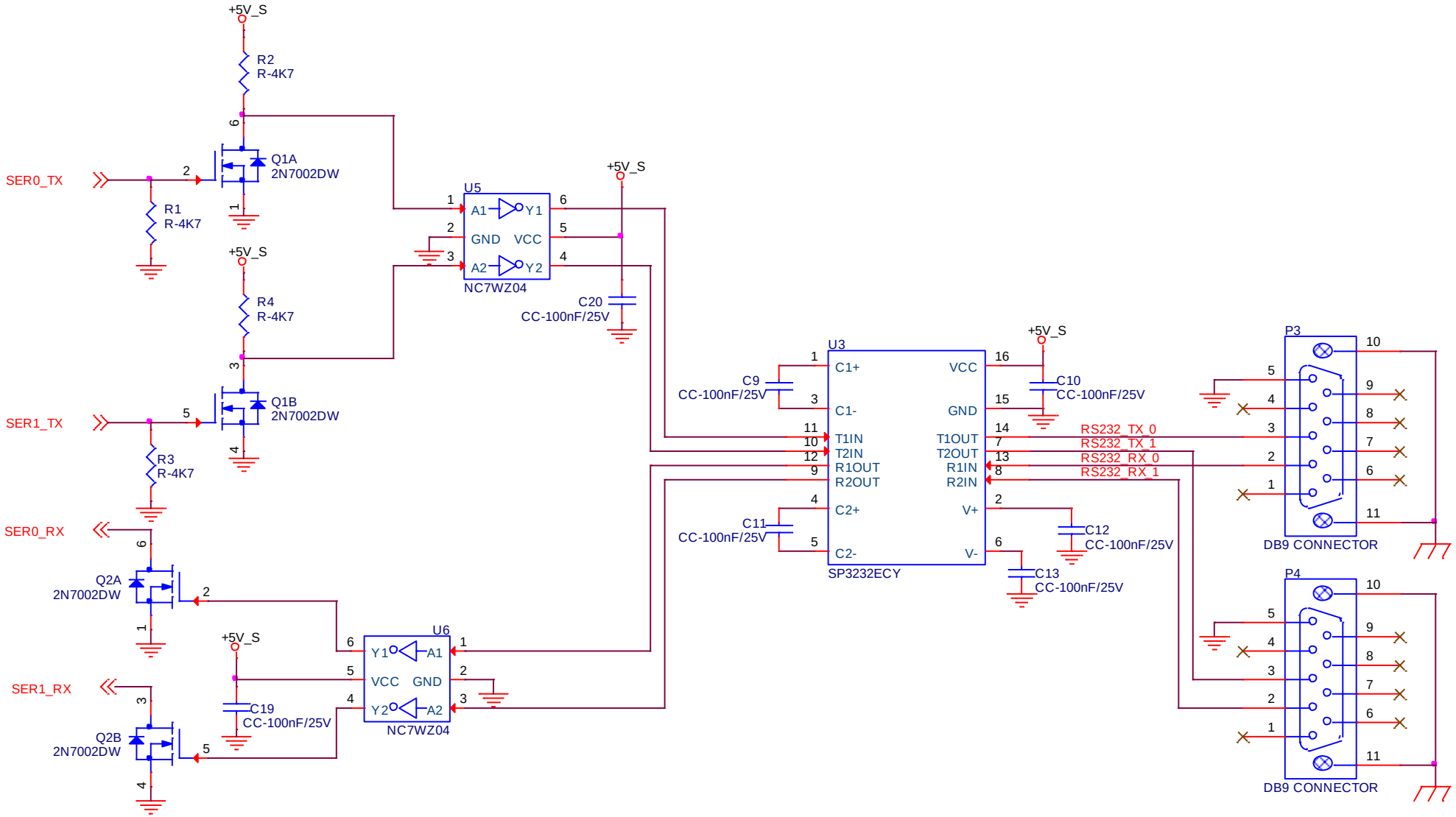
SER1_TX: UART Interface #1, Serial data Transmit (output) line, 3.3V_S electrical level.

SER1_RX: UART Interface #1, Serial data Receive (input) line, 3.3V_S electrical level.

In COM Express® specifications prior to Rel. 2.0, the pins dedicated to these two UART interfaces were dedicated to $+12V_{IN}$ power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then Schottky-diodes have been added on UART interfaces' TX and RX lines so that they are +12V Tolerant.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it is not explicitly necessary to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The schematic on the next page shows an example of implementation of RS-232 transceiver for the Carrier board.


+5V_S
R2
R-4K7
Q1A
2N7002DW
SER0_TX
R1
R-4K7
U5
A1
Y1
GND
VCC
A2
Y2
NC7WZ04
C20
CC-100nF/25V
R4
R-4K7
Q1B
2N7002DW
SER1_TX
R3
R-4K7
SER0_RX
Q2A
2N7002DW
U6
C19
CC-100nF/25V
SER1_RX
Q2B
2N7002DW
U3
C1+
C1-
T1IN
T2IN
R1OUT
R2OUT
C2+
C2-
VCC
GND
T1OUT
T2OUT
R1IN
R2IN
V+
V-
SP3232ECY
C9
CC-100nF/25V
C10
CC-100nF/25V
C11
CC-100nF/25V
C12
CC-100nF/25V
C13
CC-100nF/25V
RS232_TX_0
RS232_TX_1
RS232_RX_0
RS232_RX_1
P3
P4
DB9 CONNECTOR
DB9 CONNECTOR

3.2.3.15 I2C interface signals

This interface is managed by the embedded microcontroller.

Signals involved are the following

I2C_CK: general purpose I2C Bus clock line. Bidirectional signal, electrical level +3.3V_A with a 2K2Ω pull-up resistor.

I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3.3V_A with a 2K2Ω pull-up resistor.

3.2.3.16 Miscellaneous signals

Here following, a list of COM Express® compliant signals that complete the features of COMe-953-BT6 module.

SPKR: Speaker output, +3.3V_S voltage signal, managed by Intel® QM87 Chipset's embedded counter 2.

WDT: Watchdog event indicator Output. It is an active high signal, +3.3V_S voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW. This signal is managed by the module's embedded microcontroller.

FAN_PWM_OUT*: PWM output for FAN speed management, +3.3V_S voltage signal. It is managed by the module's embedded microcontroller.

FAN_TACHOIN*: External FAN Tachometer Input. +3.3V_S voltage signal, directly managed by the module's embedded microcontroller.

TPM_PP: Trusted Platform Module (TPM) Physical Presence pin. This signal is used to indicate Physical Presence to the optional TPM device onboard. It is an active high input signal. Please be aware that if the module purchased doesn't have the TPM module, this pin will result not connected.

THRM#: Thermal Alarm Input. Active Low +3.3V_S voltage signal with 10kΩ pull-up resistor, directly managed by the module's embedded microcontroller. This input gives the possibility, to carrier board's hardware, to indicate to the main module an overheating situation, so that the CPU can begin thermal throttling.

THRMTRIP#: Active Low +3.3V_S voltage output signal with 10kΩ pull-up resistor. This signal is used to communicate to the carrier board's devices that, due to excessive overheating, the CPU began the shutdown in order to prevent physical damages.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to FAN management were dedicated to $+12V_{IN}$ power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then protection circuitry has been added on FAN_PWM_OUT and FAN_TACHOIN lines so that they are +12V Tolerant.

3.2.3.17 Power Management signals

According to COM Express® specifications, on the connector AB there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWRBTN#: Power Button Input, active low, +3.3V_A buffered voltage signal with 10kΩ pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

SYS_RESET#: Reset Button Input, active low, +3.3V_S voltage signal with 10kΩ pull-up resistor. This signal can be connected to a momentary push-button: a pulse to GND of this signal will reset the COMe-953-BT6 module.

CB_RESET#: System Reset Output, active low, +3.3V_A voltage buffered signal. It can be used directly to drive externally a single RESET Signal. In case it is necessary to supply Reset signal to multiple devices, a buffer on the carrier board is recommended.

PWR_OK: Power Good Input, +3.3V_S active high signal with 10kΩ pull-up resistor. It must be driven by the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

SUS_STAT#: Suspend status output, active low +3.3V_A electrical voltage signal. This output can be used to report to the devices on the carrier board that the module is going to enter in one of possible ACPI low-power states.

SUS_S3#: S3 status output, active low +3.3V_A electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S4#: S4 status output, active low +3.3V_A electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S4 (Suspend to Disk) power state.

SUS_S5#: S5 status output, active low +3.3V_A electrical voltage signal. This signal is used, on the carrier board, to shut off the power supply to all the devices that must become inactive only during S5 (Soft Off) power state.

WAKE0#: PCI Express Wake Input, active low +3.3V_A electrical voltage signal with 1kΩ pull-up resistor. This signal can be driven low, on the carrier board, to report that a Wake-up event related to PCI Express has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

WAKE1#: General Purpose Wake Input, active low +3.3V_A electrical voltage signal. It can be driven low, on the carrier board, to report that a general Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used. While WAKE0# signal is managed directly by the QM87 Chipset, WAKE1#signal is managed by the Embedded microcontroller (with an internal pull-up resistor).

BATLOW#: Battery Low Input, active low, +3.3V_A voltage signal with 10kΩ pull-up resistor. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. It can be left unconnected if not used.

LID# *: LID button Input, active low +3.3V_A electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

SLEEP# *: Sleep button Input, active low +3.3V_A electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to LID# and SLEEP# inputs were dedicated to +12V_{IN} power rail. Protection circuitry has been added on LID# and SLEEP# so that they are +12V Tolerant. This has been made in order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then

3.2.3.18 SMBus signals

This interface is managed by the embedded microcontroller.

Signals involved are the following:

SMB_CK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_A with a 2k2Ω pull-up resistor.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_A with a 2k2Ω pull-up resistor.

SMB_ALERT#: SM Bus Alert line for System Management. Input signal, electrical level +3.3V_A with a 2k2Ω pull-up resistor. Any device place on the SM Bus can drive this signal low to signal an event on the bus itself.

3.2.3.19 GPIO/SDIO interface signals

According to COM Express® specifications rel. 2.0, there are 8 pins that can be used as General Purpose Inputs and Outputs **OR** as a SDIO interface.

However, neither the Intel® iCore 4th generation CPUs, nor the Intel® QM87 Chipset have an embedded SD Card controller. For this reason, the COMe-953-BT6 module use these pins only for the connection of four General Purpose Inputs and four General Purpose Outputs, which are managed though the embedded microcontroller.

Signals involved are the following:

GPI[0÷3]: General Purpose Inputs, electrical level +3.3V_A with 10kΩ pull-up resistor each.

GPO[0÷3]: General Purpose Outputs, electrical level +3.3V_A with 10kΩ pull-down resistor each.

3.2.4 BOOT Strap Signals

Configuration straps are signals that, during system reset, are set as inputs (independently by their behaviour during normal operations) in order to allow the proper configuration of the processor / chipset. For this reason, on COMe-953-BT6 are placed the pull-up or pull-down resistors that are necessary to configure the board properly.

The customer must avoid to place, on the carrier board, pull-up or pull-down resistors on signals that are used as strap signal, since it could result in malfunctions of COMe-953-BT6 module.

The following signals are used as configuration straps by COMe-953-BT6 module at system reset.

HDA_SDOUT: pin A33 of connector AB. Used to disable Flash Descriptor Security. Signal at +3.3V_S voltage level with a 1kΩ pull-down resistor.

SPKR: pin B32 of connector AB. +3.3V_S voltage signal with chipset's internal weak pull-down. Used to disable the chipset's "No Reboot" mode.

DPB_DATA_AUX_N: pin D16 of connector CD. When the Display Port B is used in HDMI mode, this signal is used to detect (and therefore, to enable) the port. Signal at +3.3V_S voltage level with a 100kΩ pull-up resistor.

DPC_DATA_AUX_N: pin C33 of connector CD. When the Display Port C is used in HDMI mode, this signal is used to detect (and therefore, to enable) the port. Signal at +3.3V_S voltage level with a 100kΩ pull-up resistor.

DPD_DATA_AUX_N: pin C37 of connector CD. When the Display Port D is used in HDMI mode, this signal is used to detect (and therefore, to enable) the port. Signal at +3.3V_S voltage level with a 100kΩ pull-up resistor.

Chapter 4.
BIOS SETUP

- InsydeH2O setup Utility
- Main setup menu
- Advanced menu
- Security menu
- Power menu
- Boot menu
- Exit menu

4.1 InsydeH2O setup Utility

Basic setup of the board can be done using Insyde Software Corp. ''InsydeH2O Setup Utility'', that is stored inside an onboard SPI Serial Flash.

It is possible to access to InsydeH2O Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select ''SCU'' icon.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
<F5> / <F6>	<F5> and <F6> keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows to display the General Help screen.
<F9>	<F9> key allows loading Setup Defaults for the board. After pressing <F9> BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<F10>	<F10> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows to discard any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow to display the setup sub- screens.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only three options can be configured:

4.2.1 Language

Use this option to select the language that the Setup utility must use. Possible options are English, French.

4.2.2 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Peripheral Configuration	See submenu	Configures the peripherals
SATA configuration	See submenu	Select the SATA controller and hard disk drive type installed in the system
Thermal Configuration	See submenu	Configures thermal parameters
Video Configuration	See submenu	Configures the options for video section
USB Configuration	See submenu	Configures USB Section
Active Management Technology Support	See submenu	Configures AMT parameters
PCI Express Configuration	See submenu	Configures PCI Express related parameters
Intel Rapid Start Technology	See submenu	Configures rapidStart
BIOS Event Log Configuration	See submenu	Configures settings for BIOS Events log

4.3.1 Peripheral configuration submenu

Menu Item	Options	Description
Numlock	On / Off	Allows to choose whether NumLock Key at system boot must be turned On or Off
HD Audio Controller	Disabled Auto	Auto: Auto detect and enable (if available) the HD Audio Codec available on the Carrier Board Disabled: Disable the HD Audio Controller
Internal LAN Controller	Disabled Enabled	Enabled: Enable the onboard Gigabit Ethernet controller. Disabled: Disable the onboard Gigabit Ethernet controller.

4.3.2 SATA configuration submenu

Menu Item	Options	Description
SATA Controller	Disabled Enabled	Enabled: Enable the internal SATA controller. Disabled: Disable the internal SATA controller.
HDC Configure As	IDE AHCI RAID	This menu item can be changed only when “SATA Controller” is Enabled. Set SATA Configuration type With AHCI, is not possible to install/boot UEFI O.S., only Legacy OS can be installed (a simpler driver is required). Setting to IDE, the controller is managed as a PCI device, so addresses reallocation and INT line sharing is possible. Setting it to RAID, the controller will enable both AHCI and RAID functionalities. The BIOS will also load the RAID setup utility which can be accessed at boot time.
Software Feature Mask Configuration	See next item	This menu item is available only when “SATA Controller” is Enabled and HDC is configured to “AHCI”.
HDD Unlock	Disabled Enabled	This item appears when entering the previous voice. It allows to enable the support for HDD password unlock from the O.S.
Aggressive LPM Support	Disabled Enabled	This menu item can be changed only when “SATA Controller” is Enabled and HDC is configured to “AHCI”. Enables or disables the support for Aggressive Link Power Management (SALP), which allows the SATA controller entering a low-power state when idle, thus saving energy.
Alternate ID	Disabled Enabled	This menu item can be changed only when “SATA Controller” is Enabled and HDC is configured to “RAID”. Report an Alternate Device ID
Serial ATA Port 0 / 1 / 2 / 3	See submenu	Shows information and allows settings of eventual devices connected to SATA ports 0, 1, 2 and 3

4.3.2.1 Serial ATA Port x configuration submenu

Menu Item	Options	Description
SATA Port	Disabled / Enabled	Allows enabling or disabling the single SATA Port
Hot-Plug	Disabled / Enabled	Enables or disables the support for Hot-Plug on this SATA Port
Spin-Up Device	Disabled / Enabled	Enables or disables the support for Staggered Spin-Up of SATA disks
Device Type	Hard Disk Drive Solid State Drive	Configures the SATA port in order to manage Hard Disks or Solid State Disks

4.3.3 Thermal configuration submenu

Menu Item	Options	Description
Automatic Reporting	Disabled Enabled	When Enabled, configures the Critical trip Point, the Active Trip Point 0 and the Passive Trip Point automatically based on values recommended in BWG's Thermal Reporting for Thermal managent settings. Set to disabled for manual configuration.
Critical Trip Point	85°C / 90°C / 100°C / 105°C	This menu item can be changed only when "Automatic Reporting" is Disabled. ACPI Critical Trip Point - the point at which the OS will shut down the system.
Active Trip Point 0	70°C / 75°C / 80°C / 85°C / 90°C / 100°C / 105°C	This menu item can be changed only when "Automatic Reporting" is Disabled. ACPI Active Trip Point 0: the point at which the OS will turn the processor fan to High Speed.
Fan Intermediate Speed	0 ÷ 100	This value must be between 0 (Fan off) and 100 (Max Fan Speed). This is the speed at which fan will run when the temperature is between Active Trip Point 0 and 1
Active Trip Point 1	45°C / 50°C / 55°C / 60°C / 65°C / 70°C / 75°C / 80°C / 85°C / 90°C / 100°C / 105°C	ACPI Active Trip Point 1: the point at which the OS will turn the processor fan to Low Speed
Passive Trip Point	60°C / 65°C / 70°C / 75°C / 80°C / 85°C / 90°C / 100°C / 105°C	This menu item can be changed only when "Automatic Reporting" is Disabled. Set the CPU temperature point of Throttle On
System Fan Boot Speed	0 ÷ 100	This value must be between 0 (Fan Off) and 100 (Max fan speed). This is the speed at which the system fan will run during boot phase
Bi-Directional PROCHOT#	Disabled Enabled	PROCHOT# is the signal used to start thermal throttling. This signal can be driven by any processor cores' to signal that the processor will begin thermal throttling. If bi-directional signaling is enabled, then external components can also drive PROCHOT# signal in order to start throttling.

4.3.4 Video configuration submenu

Menu Item	Options	Description
Primary Display	Auto / IGFX / PEG / PCIE	Allows to select if Internal Graphics controller (IGFX), external PCI-e Graphic Controller x16 (PEG) or external Graphic controller on a PCI-e x1 lane (PCIE) should be used as a Primary display. Auto allows the automatic configuration based on the devices that are found connected.
Internal Graphic Device	See submenu	Configures the options for the internal Graphics controller
PCI Express Graphic	See submenu	Configures the options for the external PCI-Express Graphics controller
SA DMI Configuration	See submenu	Configures some DMI parameters

4.3.4.1 Internal Graphic Device configuration submenu

Menu Item	Options	Description
Integrated Graphics Device	Auto / Disabled / Enabled	Enabled: enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disabled: always disable IGD Auto: Enable if no other Display Device is found
HDMI Internal Audio Codec	Disabled Enabled	Enable or Disable the internal Audio Codec used with HDMI
RC6 (Render Standby)	Disabled Enabled	Permits to enable the render standby features, which allows the onboard graphics entering in standby mode to decrease power consumption
Deep Render Standby	Disabled Enabled	Similar to the previous item, this option allows entering lower stand-by voltage states, therefore decreasing furthermore the power consumption.
IGD - Gtt Size	1MB / 2MB	Select the GTT (Graphics Translation Table) Size
IGD - Aperture Size	128MB / 256MB / 512MB	Use this item to set the total size of Memory that must be left to the GFX Engine
IGD - DVMT Pre-Allocated	0 MB / 32MB / 64MB / 96MB / 128MB / 160MB / 192MB / 224MB / 256MB / 288MB / 320MB / 352MB / 384MB / 416MB / 448MB / 480MB / 512MB / 1024MB	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphic Device
IGD - DVMT Size	128MB / 256MB / MAX	Select the size of DVMT (Dynamic Video Memory) 5.0 that the Internal Graphics Device will use

IGD - Boot Type	VBIOS Default - CRT - eDP/LVDS - DDI1 - DDI2 - DDI3	Select the video Device that will be activated during POST phase. "VBIOS default" automatically selects also the secondary device. The detection order is CRT → eDP/LVDS → DDI1 → DDI2 → DDI3
LFP eDP/LVDS device	Enabled / Disabled	Enable or disable the LFP (Local Flat Panel) eDP or LVDS device
LFP Panel Type	640x480 / 800x480 800x600 / 1024x600 / 1024x768 / 1280x720 / 1280x800 / 1280x1024 / 1366x768 / 1440x900 / 1600x900 / 1680x1050 / 1920x1080	Select a software resolution (EDID settings) to be used for the internal flat panel.
LFP Color Depth	24 bit VESA / 24 bit JEIDA 18 bit	Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.
LFP BUS mode	Single Channel Dual Channel	Allows configuration of LVDS interface in Single or Dual channel mode
LFP Spreading Depth	No Spreading / 0.5% / 1.0% / 1.5% / 2.0% / 2.5%	LVDS Clock frequency center spreading depth
LFP Output Swing	150mV / 200mV / 250mV / 300mV / 350mV / 400mV / 450 mV	LVDS differential output swing level
Backlight Control	PWM Inverted / PWM Normal	This option allows selecting if PWM control of the backlight must be with normal or inverted polarity.

4.3.4.2 PCI Express Graphic configuration submenu

Menu Item	Options	Description
PCIE Reset Delay	Disabled / 50 ms / 100 ms / 200 ms /300 ms	Allows setting a delay time for PCI Express Graphics reset. Select longer times in case that the PEG device doesn't work properly.
ASPM	Disabled / L0s / L1 / L0s & L1 / Auto	Manages PCI Express Graphics (PEG) L0s and L1 power states, for OSs able to handle Active State Power Management (ASPM)
Max Speed	Auto / Gen1 / Gen2 / Gen3	Allows forcing the PCI-Express Graphics bus to support specific generation's architecture. Auto means that the speed is adapted to the attached device (default).
Always Enable PEG	Disabled / Enabled	Use this item to leave the PEG always enabled even if there isn't any attached device.

4.3.4.3 SA DMI configuration submenu

Menu Item	Options	Description
DMI Link ASPM Control	Disabled / L0s / L1 / L0s & L1 / Auto	Configures the support for L0s and L1 power states of DMI Bus, on CPU, for OSs able to handle Active State Power Management (ASPM)
DMI Extended Synch Control	Disabled / Enabled	Enables or disables the extended synchronization on DMI bus
DMI Gen2	Disabled / Enabled	Enables or disables Gen2 support on DMI bus

4.3.5 USB configuration submenu

Menu Item	Options	Description
USB BIOS Support	Disabled / Enabled / UEFI only	This option allows enabling USB support for Keyboard / mouse / Storage on DOS and UEFI environments. UEFI will be supported only if the item is set to “UEFI only”
USB Precondition	Disabled / Enabled	Allows enabling or disabling the USB preconditioning, which works on USB host controller and root ports for a faster enumeration
xHCI	Enabled / Disabled / Auto	Enables or disabled xHCI controller, which manages all USB ports, including USB 3.0. When disabled, USB 3.0 ports will not be usable. Auto and Smart Auto need an ACPI and USB 3.0 aware OS.
Per-Port Control	Disabled / Enabled	Allows to enable / disable singularly each of USB ports #0 ÷ #7
USB Port0 / USB Port 1 / USB Port2 / USB Port3 / USB Port4 / USB Port5 / USB Port6 / USB Port7	Disabled / Enabled	Available only when “Per-Port Control” is Enabled Allows to enable / disable individually each of the USB 2.0 port

4.3.6 Active Management Technology Support submenu

Menu Item	Options	Description
Intel AMT Support	Enabled / Disabled	Enables or disables the Intel® Active Management Technology BIOS Extension. Note: Intel® AMT Hardware remains always enabled, this option controls just the BIOS extension execution.
MEBx Selection Screen	Enabled / Disabled	Enables or disables the Intel® Management Engine BIOS Extension (Intel® MEBX) Selection screen
Hide Un-Configure Prompt	Enabled / Disabled	Hide Un-configure ME without password confirmation prompt.
MEBx Debug Message Output	Enabled / Disabled	Enables or disables MEBx Debug Message Output.
Un-Configure ME	Enabled / Disabled	Un-configure ME without password.
Intel AMT Password Write	Enabled / Disabled	Enables or disables Intel AMT Password write. Password can be written when this item is set to enabled.
AMT CIRA Request Trig	Enabled / Disabled	Triggers the AMT CIRA (Client Initiated Remote Access) boot
AMT USB Configure	Enabled / Disabled	Enables / Disables the USB configure function.
PET Progress	Enabled / Disabled	Enables or disables the PET (Platform Event Trap) Progress Event
AMT CIRA Timeout	0 ÷ 100	OEM defined timeout for establishing a MPS (Manageability Presence Server) connection.
ASF Support	Enabled / Disabled	Enable / Disable Alert Specification format
Watchdog Support	Enabled / Disabled	Enable / Disable Watchdog Timer.
OS Timer	0 ÷ 100	This item can be changed only when Watchdog Support is “Enabled”. Set OS Watchdog Timeout
BIOS Timer	0 ÷ 100	This item can be changed only when Watchdog Support is “Enabled”. Set BIOS Watchdog Timeout

4.3.7 PCI Express Configuration submenu

Menu Item	Options	Description
PCI Express Clock gating	Disabled / Enabled	Enable or Disable PCI Express Clock Gating for each root port
DMI Link ASPM Control	Disabled / Enabled	Enables or disables the Active State Power Management (ASPM) control of DMI link
DMI Extended Synch Control	Disabled / Enabled	Enables or disables the extended synchronization on DMI bus
PCI Express Root Port 1 PCI Express Root Port 2 PCI Express Root Port 3 PCI Express Root Port 4 PCI Express Root Port 5 PCI Express Root Port 7 PCI Express Root Port 8	See submenu	

4.3.7.1 PCI Express Root Port #x configuration submenus

Menu Item	Options	Description
PCI Express Root Port x	Disabled / Enabled	Enable or Disable single PCI Express Root Port #x. When disbaled, all following menu items will be not present. Please be aware that disabling PCI Express Root Port 1 will result in disabling all PCI Express Root Ports
Automatic ASPM	Disabled / L0s / L1 / L0s & L1 / Auto	Enables or disables Root Port #x L0s and L1 power states, for OSs able to handle Active State Power Management (ASPM)
URR	Disabled / Enabled	Enables or disable PCI Express Unsupported Request Reporting.
FER	Disabled / Enabled	Enables or disable PCI Express device Fatal Error Reporting.
NFER	Disabled / Enabled	Enables or disable PCI Express device Non-Fatal Error Reporting.
CER	Disabled / Enabled	Enables or disable PCI Express device Correctable Error Reporting.
CTO	Default / 16-55 ms / 65-210ms / 260-900ms / 1-3.5ms / Disabled	Sets or disable PCI Express Completion Timer TO.
SEFE	Disabled / Enabled	Enables or disables reporting a System Error on Fatal Error

SENFE	Disabled / Enabled	Enables or disables reporting a System Error on Non-Fatal Error
SECE	Disabled / Enabled	Enables or disables reporting a System Error on Correctable Error
PME Interrupt	Disabled / Enabled	Enables or disables triggering of an interrupt on a PME (Power Management Event).
PME SCI	Disabled / Enabled	Enables or disables use of ACPI SCI (System Control interrupt) on a PME (Power Management Event).
Hot Plug	Disabled / Enabled	Enables or disables PCI Express Hot Plug capability
PCIe Speed	Auto / Gen1 / Gen2	Allows automatic detection or forcing of PCI express link's speed

4.3.8 Intel Rapid Start Technology submenu

Menu Item	Options	Description
Rapid Start Support	Enabled / Disabled	Enables or disables the Intel® Rapid Start Feature for a quicker Startup or Resume from Hybernate. When disabled, all the following menu items will not be visible
Entry on S3 RTC wake	Enabled / Disabled	Enables or disables Rapid Start invocation when in S3 (stand-by) State
Entry After	Immediately / 1 minutes / 2 minutes / 5 minutes / 10 minutes / 15 minutes / 30 minutes / 1 hour / 2 hours / 12 hours / 24 hours	This menu item is available only when "Entry on S3 RTC wake" is enabled. Allows the selection of a timeout for Rapid Start invocation when in S3 state
Entry on S3 critical battery event	Enabled / Disabled	Enables or disables Rapid Start invocation when a critical battery event occurs during S3 (stand-by) State
Critical battery wake threshold (%)	10 / 20 / 30 / 40 / 50 / 60 / 70 / 80 / 90 / 100	Sets the battery capacity threshold for the critical battery event
Active Page Threshold Support	Enabled / Disabled	Enables or disables support for Rapid Start technology with small disk partitions
Active Memory Threshold	*Numeric value*	This menu item is available only when "Active Page Threshold Support" is enabled. Used to support Rapid Start Technology each time that the partition size is more than Active Memory Threshold size (in MB). When this value is set to zero, RST will work in AUTO mode and check if partition's size is enough when entering S3 state.
Hybrid Hard Disk Support	Enabled / Disabled	Enables or disables support for Hybrid Hard Disks
RapidStart Display Save/Restore	Enabled / Disabled	Enables or disables the feature that allows saving and restoring Intel Rapid Start Display screen when the system enters in and exit from sleep mode

4.3.9 BIOS Event Log Configuration submenu

Menu Item	Options	Description
Log Event To	ALL / BIOS / BMC SEL / MEMORY	Allows selection of storage destination of BIOS Events
Event Log Full option	Overwrite / Clear All / Stop Logging	Allows setting of the behavior to adopt when the Log Event storage area is Full. With “overwrite”, older data will be overwritten by the newer ones. With “Clear All”, all old data will be cleared before continue logging. “Stop logging” will stop the events logging
Event log viewer	See following options	This item is used to view event logs of all storage areas.
Memory Event Log viewer		View event logs stored in memory
BIOS Event Log viewer		View event logs stored in BIOS
Clear Memory Event Log		Clear all event logs stored in Memory
Clear BIOS Event Log		Clear all event logs stored in BIOS

4.4 Security menu

Menu Item	Options	Description
Select TPM Device	TPM 1.2 / TPM 2.0	Select TPM Device to initialize
TPM Operation	No Operation Disable and Deactivate Enable and Activate	Enable / Disable TPM Function. This option will automatically return to “No Operation” after the reboot
TPM Force Clear	Enabled / Disabled	This option is only available when TPM Operation is set to “Enable and Activate” Clears the TPM when enabled.
Set Supervisor Password		Install or Change the password for supervisor. Length of password must be greater than one character.
Power on Password	Enabled / Disabled	Available only when Supervisor Password has been set. Enabled: System will ask to input a password during P.O.S.T. phase. Disabled: system will ask to input a password only for entering Setup utility

4.5 Power menu

Menu Item	Options	Description
Advanced CPU Control	See submenu	These items control various CPU parameters
LPC Clock run	Enabled / Disabled	When Enabled, the CLKRUN# logic can be used to stop the LPC clocks.
Wake on PME	Enabled / Disabled	Determines whether the system must wake up or not when the system power is off and occurs a PCI Power Management Enable wake-up event.
Power Fail Resume Type	Always ON Always OFF Last State	Determine the System Behavior after a power failure event. In case the option is “Always ON”, the board will start every time the power supply is present. When the option is “Always OFF”, the board will not start automatically when the power supply returns. Finally, if this option is set to “Last State”, the board will remember the state it had when the power supply went down: so, if the board was on, it will start again when the power returns, and will remain off if the board was in this state when the power went down.
LID# Configuration	Force Open Force Closed Normal Polarity Inverted Polarity	Configure LID_BTN# Signal as always open or closed (i.e., Force Open / Force Closed), no matter the pin level, or configures the signal polarity: “Normal Polarity” means the signal goes High when open, “Inverted Polarity” means the signal goes Low when open
LID# Wake Configuration	No Wake Only From S3 Wake From S3/S4/S5	This item can be changed only when “LID # Configuration” is not set to Force Open or Force Closed. Configure LID # Wake capability. According to the pin configuration, when the LID is open it can cause a system wake from a sleep state
Batteryless Operation	Enabled / Disabled	This item has to be enabled in case that the RTC battery is not present on the Carrier board
Watchdog Configuration	See submenu	Configures various parameters for Watchdog

4.5.1 Advanced CPU control submenu

Menu Item	Options	Description
Hardware prefetcher	Enabled / Disabled	CPU Hardware prefetcher analyzes the code in execution, and tries to anticipate CPU requirements, by pre-loading data and instructions from memory into Level L2 cache, in order to reduce latencies associated with memory read. This feature can be disabled or enabled, to increase performances.
P-States (IST)	Enabled / Disabled	Enable or disable processor management of performance states (P-states)
Active Processor cores	All Cores / 1 Core / 2 Core / 3 Core	Number of Cores to enable in each processor package
HT Support	Auto / Disabled	Disables or automatically enables (if available) the support for Hyper Threading
Execute Disable Bit	Enabled / Disabled	This item allows enabling or disabling the XD feature flag, i.e. it allows enabling or disabling the hardware feature needed for data execution prevention. This option can be used only with newer OSes that support this feature
Intel (VMX) Virtualization Technology	Enabled / Disabled	Enable this feature to allow Virtual Machines to use all the Hardware capabilities offered by Intel® Virtualization Technology.
Boot Performance Mode	Max Non-Turbo Max Power Saving Turbo Performance	Select the performance state that the BIOS will set before OS handoff.
C-States	Enabled / Disabled	Enable processor idle power saving states (C-States).
ACPI 5.0 CPPC Support	Enabled / Disabled	Enables ACPI 5.0 Collaborative Processor Performance Control (CPCC) support. When enabled, the Platform exposes CPCC interfaces to the OS. When Disabled, the Platform exposes legacy (non-CPCC) processor interfaces to the OS.
ACPI 5.0 CPPC Platform SCI	Enabled / Disabled	Only available when “ACPI 5.0 CPPC Support” is enabled. Enables the platform generation of a SCI (System Control Interrupt) on a CPCC command completion. When enabled, the platform will generate a GPE (General Purpose Event) /SCI. When disabled, the platform will not generate GPE/SCI and OS must poll for command completion.

4.5.2 Watchdog Configuration submenu

Menu Item	Options	Description
Watchdog Status	Disabled/ Enabled	Enables or disables the Watchdog Timer Mechanism. When disabled, all remaining menu options will be not accessible.
Event Action	Raise WDT signal Power Button Pulse None	Select the action that will performed when the Watchdog event time-out expires
Reset Action	System Reset Power Button Override Raise WDT Signal	Select the action that will performed when the Watchdog Reset time-out expires
Watchdog Delay	0 / 1 / 2 / 4 / 8 / 16 / 32 / 64	It specifies the minutes of delay, after system power up, before the watchdog Event timeout starts counting. During the delay timeout, a refresh operation will immediately trigger to normal operations.
Event time-out	0 / 1 / 2 / 4 / 8 / 16 / 32 / 64	It specifies the minutes without being refreshed before the Event action triggers. A refresh will restart this timeout
Reset time-out	1 / 2 / 4 / 8 / 16 / 32 / 64	It specifies the minutes without being refreshed before the reset action triggers. A refresh will restart to the beginning of the event Timeout.

4.6 Boot menu

Menu Item	Options	Description
Boot type	Dual boot Type Legacy Boot Type UEFI Boot Type	Allows to select if the OS must be booted using Legacy Boot Mode, UEFI Boot mode or indifferently using both modalities (depending on the OS)
Quick Boot	Enabled / Disabled	Skip certain tests while booting. This will decrease the time needed to boot the system.
Quiet Boot	Enabled / Disabled	Disables or enables booting in Text Mode.
Network Stack	Enabled / Disabled	This submenu is available only when “Boot Type” is set to “UEFI Boot type” or “Dual Boot type”. When enabled, this option will make available the following Network Stack services: Windows 8 BitLocker Unlock UEFI IPv4/IPv6 PXE Legacy PXE OpROM
PXE Boot Capability	Disabled UEFI: IPv4 UEFI: IPv6 UEFI: IPv4/IPv6 Legacy	This submenu is available only when “Network Stack” is Enabled Specifies the PXE (Preboot Execution Environment) Boot possibilities. When Disabled, Network Stack is supported For UEFI, it is possible to support IPv4, IPv6 or both of them In Legacy mode, only Legacy PXE OpROM is supported
PXE Boot to LAN	Enabled / Disabled	This submenu is available only when “Boot Type” is set to “Legacy Boot type”. Disables or enables the possibility for the PXE to perform the boot from LAN.
Power Up in Standby Support	Enabled / Disabled	Disable or enable Power Up in Standby Support. The PUIS feature set allows devices to be powered-up in the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.
Add Boot options	First / Last / Auto	Specifies the position in Boot Order for Shell, Network and Removable Disks
ACPI selection	Acpi1.0B / Acpi3.0 / Acpi4.0 / Acpi5.0	Using this menu item is possible to select to which specifications release the ACPI tables must be compliant.
USB Boot	Enabled / Disabled	Disables or enables booting from USB boot devices.
EFI Device First	Enabled / Disabled	Determine if boot must happen first through EFI devices or through legacy devices. When enabled, it will happen first from EFI devices. When disabled, it will happen first from Legacy devices.

Windows® 8 Fast Boot	Enabled / Disabled	This submenu is available only when “Boot Type” is set to UEFI Boot Type. If enabled, the system firmware does not initialize keyboard and check for firmware menu key.
USB Hot Key Support	Enabled / Disabled	This submenu is available only when “Boot Type” is set to UEFI Boot Type and “Windows® 8 Fast Boot” is Enabled. Enable or disable the support for USB HotKeys while booting. This will decrease the time needed to boot the system
Timeout	0 ÷ 300	The number of seconds that the firmware will wait before booting the original default boot selection.
Automatic Failover	Enabled / Disabled	When this item is enabled, if boot from the default device fails, then the system will attempt directly to boot from the next device on the Boot devices list When this item is disabled, in case of failure from booting from the first boot device, then a Warning Message will pop up and subsequently enter into Firmware UI.
EFI	See Submenu	This submenu is available only when “Boot Type” is not set to “Legacy Boot type”. Entering the submenu, will show a list of EFI boot devices. Use F5 and F6 key to change order for boot priority.
Legacy	See Submenu	This submenu is available only when “Boot Type” is not set to “UEFI Boot type”.

4.6.1 Legacy submenu

Menu Item	Options	Description
Boot Menu	Normal / Advance	When set to Normal, this submenu will allow configuring all possible options for Legacy boot. When set to Advance, it will be possible to configure Boot Order only for bootable devices found in the system
Boot Type Order	Floppy Drive / Hard Disk Drive CD/DVD-ROM Drive / USB / Others	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will allows selecting the boot from different devices. Use the + and - Keys to change the boot order priority
Hard Disk Drive	*List of HD Drives found connected*	This voice will be selectable only when “Boot menu” is set to “Normal” and if there are HD drives connected. The list shown under this item will show different Disk drives found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority
USB	*List of HD Drives found connected*	This voice will be selectable only with “Boot menu” set to “Normal” and if there are USB disks connected. The list shown under this item will show different USB disks found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority

4.7 Exit menu

Menu Item	Options	Description
Exit Saving Changes		Exit system setup after saving the changes. F10 key can be used for this operation.
Save Change Without Exit		Save all changes made, but doesn't exit from setup utility.
Exit Discarding Changes		Exit system setup without saving any changes. ESC key can be used for this operation.
Load Optimal Defaults		Load Optimal Default values for all the setup items. F9 key can be used for this operation.
Load Custom Defaults		Load Custom Default values for all the setup items.
Save Custom Defaults		Save Custom Default values for all the setup items.
Discard Changes		Discard all changes made without exiting BIOS utility

Chapter 5.
Appendices

- Thermal Design

5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like COMe-953-BT6 module, offer to the user very good performances in minimal spaces, therefore allowing the system's minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

COM Express® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the COM Express® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsink with fan in some situation can represent the cooling solution. Indeed, when using COMe-953-BT6 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with FAN could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide COMe-953-BT6 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions. Please ask SECO for specific ordering codes.

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