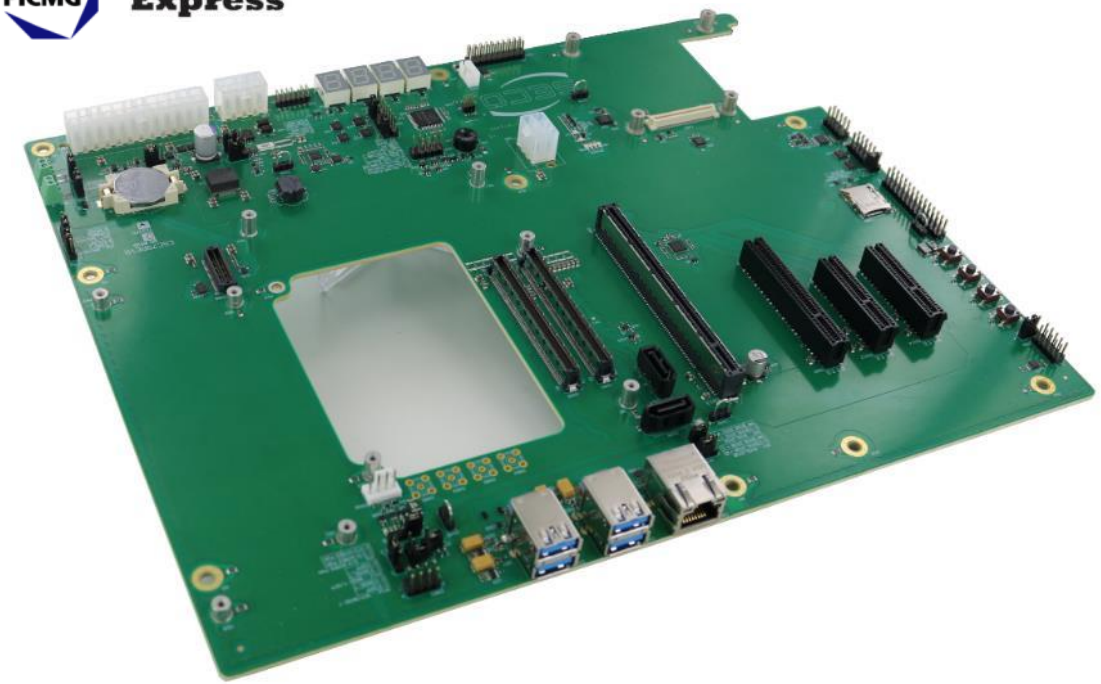
Com express

User Manual



CCOMe-C79

Carrier Board for COM-Express™ Type 7 Module
on ATX form factor

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	2nd August 2021	First release	AR

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at https://www.seco.com/ (registration required).

Our team is ready to assist you.

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Chapter 1.
INTRODUCTION

- Warranty
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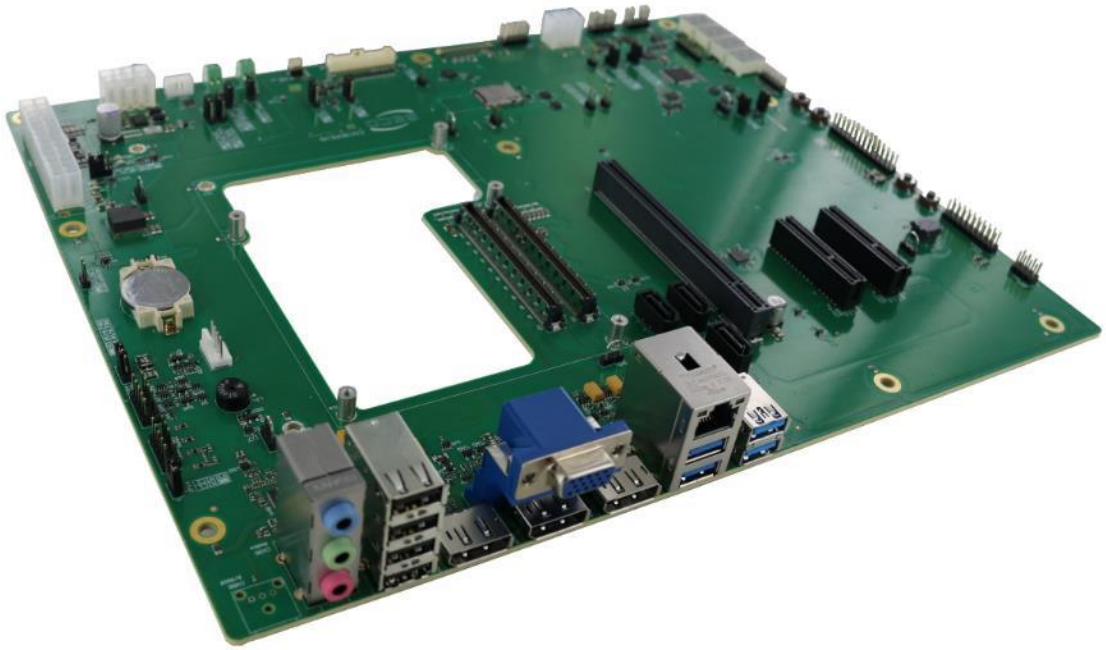


1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/eu/support/online-rma.html (Online RMA). The RMA Authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following after a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty.

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit https://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be released within 1 working day (only for on-line RMA requests).

1.4 Safety

The CCOMe-C79 board uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The CCOMe-C79 board, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

Whenever handling a CCOMe-C79 board, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The CCOMe-C79 board is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Policy

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, the CCOMe-C79 Carrier Board shall be:

- used inside a fire enclosure made of non-combustible material or V-1 material
- used inside an enclosure provided with the symbol IEC 60417-5041(element 1a according to clause 9.5.2 of the IEC 62368-1) on the external part;
- installed inside an enclosure compliant with all applicable IEC 62368-1 requirements;

The manufacturer which includes a CCOMe-C79 Carrier Board in his end-user product shall:

- verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition
- prescribe temperature and humidity range for operating, transport and storage conditions;
- prescribe to perform maintenance on the board only when it is off and has already cooled down;
- prescribe that the connections from or to the board have to be compliant to ES1 requirements;
- the board in its enclosure must be evaluated for temperature and airflow considerations.

1.8 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
GbE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
JTAG	Joint Test Action Group, common name of IEEE1149.1 standard for testing printed circuit boards and integrated circuits through the Debug port
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
N.A.	Not Applicable
N.C.	Not Connected
OS	Operating System
PCI-e	Peripheral Component Interface Express
PWM	Pulse Width Modulation
PWR	Power
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows use the use of the same SD interface to drive different Input/Output

	devices, like cameras, GPS, Tuners and so on
SIM	Subscriber Identity Module, a card which stores all data of the owner necessary to allow him accessing to mobile communication networks
SM Bus	System Management Bus, a subset of the I2C bus protocol dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UIM	User Identity Module, an extension of SIM modules.
USB	Universal Serial Bus
V_REF	Voltage reference Pin

1.9 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
Com Express™	https://www.picmg.org/openstandards/com-express/
Com Express™ Carrier Design Guide	https://www.picmg.org/wp-content/uploads/PICMG_COMDG_2.0-RELEASED-2013-12-061.pdf
DDC	https://www.vesa.org/
DP, eDP	https://www.vesa.org/
Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/docs/en/user-guide/UM10204.pdf
Intel® Front Panel I/O connectivity DG	http://www.formfactors.org/developer/specs/A2928604-005.pdf
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/lit/ug/snla187/snla187.pdf
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SD Card Association	https://www.sdcard.org
SM Bus	http://www.smbus.org/specs
TMDS	http://www.latticesemi.com/view_document?document_id=38351
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb20_docs/usb_20_080117.zip
USB 3.0	http://www.usb.org/developers/docs/usb_31_080117.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram

2.1 Introduction

CCOMe-C79 is a carrier board, designed in ATX form factor, intended for the use with COM-Express™ Type 7 CPU modules.

COM-Express™ is an open industry standard defined specifically for COMs (computer on modules). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today.

COM Express™ CPU modules integrate all the core components of a typical PC-like architecture, and make all interface available through two standardized connectors, so that COM Express™ modules become scalable. This means that once an application has been created, there is the ability to diversify the product range through the use of different performance class or form factor size modules.

Baseboard designers can use just the I/O interfaces that really need, providing, on the carrier board, the routing to the adequate interface connectors.

This versatility allows the designer to create a dense and optimised package, which results in a more reliable product while simplifying system integration.

CCOMe-C79 board can be used both as an evaluation module, to test the functionality of your COM-Express™ module and design an application specific carrier board for it, or as a complete carrier board, already suited for standard purposes, with a small space consumption.

In any case, the solutions so realised is fully scalable, and allows to the user to keep his own-designed system continuously up-to-date, since the system can be updated simply replacing the COM-Express™ module with a newer one, just unplugging the module and replacing it, without the need of redesigning it.

The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

2.2 Technical Specifications

Supported Modules
- COM Express™ Type 7 compliant modules

Mass Storage interfaces
- 2x SATA 7p M connectors
- µSD Card slot (interface multiplexed with GPIO header)

Networking
- 1x RJ-45 connector
- 4x 10Gbase-KR interfaces on OCP Type-C connector
- 4x MDIO / I2C interfaces on internal pin header
- 4x SDP interfaces on SMA RF connectors

USB
- 4 x USB 3.1 Host ports on Dual Type-A sockets

PCI-e
- 2x PCI-e x4 Slots
- 1x PCI-e x8 Slot
- 1x PCI-e x16 Slot

Serial Ports
- 2 x RS-232 ports on dedicated pin header (from module)

Other Interfaces
- BMC connector with SM Bus, I2C, LPC, 1x USB 2.0, 1x PCI-e x1, NCSI signals
- 4 x GPI + 4 x GPO pin header (interface multiplexed with µSD slot)
- SPI Flash Socket
- Button / LEDs front panel header
- 4-pin tachometric FAN connector
- I2C + SM Bus on feature Pin header
- I2C Flash Socket
- SM Bus Smart Battery Connector
- 4 x 7-segment LCD displays for POST codes
- LPC/eSPI internal header
- USB Overcurrent header
- JTAG connector
- FuSa header
- SPI Flash header
- Buzzer

Power supply: ATX 24 poles connector for carrier board working only
Auxiliary 12V connector for carrier board working only
12 V_{DC} power in connector for COM Express™ module's working
Coin-cell holder for RTC

Operating temperature: 0°C ÷ +60°C * (Commercial version)

Dimensions: 305x244mm (ATXform factor, 12" x 9.6")

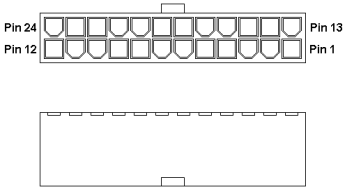
! ** Temperature ranges indicated mean that all components available onboard are certified for working with a Tcase included in these temperature ranges. This means that it is customer's responsibility to ensure that all components' Tcases remain in the range above indicated. Please also check paragraph 4.1.*

2.3 Electrical Specifications

CCOMe-C79 board needs to be supplied using a standard ATX Power Supply, which can, however, also be configured to work in AT mode.

ATX / AT Power Connector – CN10			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V_RUN	13	+3.3V_RUN
2	+3.3V_RUN	14	---
3	GND	15	GND
4	+5V_RUN	16	PS_ON#
5	GND	17	GND
6	+5V_RUN	18	GND
7	GND	19	GND
8	PWR_OK_ATX	20	---
9	+5V_ALW	21	+5V_RUN
10	+12V_RUN	22	+5V_RUN
11	+12V_RUN	23	+5V_RUN
12	+3.3V_RUN	24	GND

Power Connector CN10 is type Molex Mini-Fit Jr. connector, p/n 39-28-1243, or equivalent, with the pin-out indicated in the table here on the left (it is the standard 24-pin ATX pin-out).



Mating Connector, MOLEX p/n 39-01-2240 or equivalent, with female crimp terminal MOLEX series 5566.

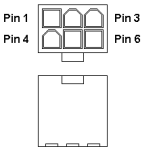
PS_ON#: this signal is present only if the board is configured, via CN11 and J2, to work in ATX mode. If working in AT mode, this pin is connected directly to Ground.

Power connector can be set to work in ATX mode or AT mode by using dedicated jumpers CN11 and J2, which are a standard pin headers, P2.54mm, 1x3 pin.

CN11 position	J2 position	Power mode
2-3	Not Care	AT mode
1-2	1-2	ATX mode
1-2	2-3	AT mode

Auxiliary Power Connector – CN7			
Pin	**Signal**	**Pin**	**Signal**
1	+12V_RUN	5	GND
2	+12V_RUN	6	GND
3	+12V_RUN	7	GND

The board has an Auxiliary Power connector CN7 providing +12V_RUN for the carrier board section only, in case multiple PCI-e modules are connected.



CN7 is 6-poles connector, type MOLEX mini-Fit Jr. p/n 39-28-1063 or equivalent.

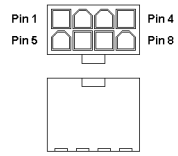
Mating Connector, MOLEX p/n 39-01-2060 or equivalent, with female crimp terminal MOLEX series 5566.

CPU Power Connector – CN8			
Pin	Signal	Pin	Signal
1	GND	5	+12V_RUN
2	GND	6	+12V_RUN
3	GND	7	+12V_RUN
4	GND	8	+12V_RUN

The board has a CPU Power Connector CN8 providing +12V_RUN for the COM Express™ module only.

CN8 is a Molex Mini-Fit jr. 8 poles connector, p/n 39-28-1083 or equivalent.

Mating Connector, MOLEX p/n 39-01-2080 or equivalent, with female crimp terminal MOLEX series 5566.



The use of wires with section 18 AWG is recommended, in order to ensure the proper amperage of the power section.

JP2 position	+5V_ALW Current monitor selector
Not inserted	Current measurement enabled
Inserted	Current measurement disabled

The power consumption on +5V_ALW can be monitored by removing 2 way jumper JP2 and inserting a tester set as ammeter.

Alternatively, the consumption on +5V_ALW can be monitored by inserting a tester set as ammeter between pin 1 and 2 of +5V_ALW Sense Connector CN4.

CN4 is a dedicated 2 position Wire to Board Terminal Block, type Wurth p/n 691210910002.

CN3 position	Power Ok management
1-2	PSU PWR_OK enabled
2-3	PWR_OK always high

The COM Express™ card edge connector has a PWR_OK signal from main power supplied by Carrier Board to the module, indicating that all the power supplies to the Module are stable within specified ranges. The Module will typically not power up until the PWR_OK signal goes active.

CN3 is a standard pin header, P2.54mm, 1x3 pin, dedicated to manage this power status signal for the Module. For normal operation, set the jumper in 1-2 position, otherwise set in 2-3 position to fix its level high and have it always activated.

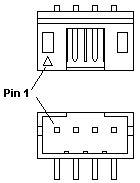
Diode LED D17 is present on Carrier Board to notify the system has been correctly powered-up, directly driven through an High-Speed Buffer by PWR_OK signal.

Another diode LED D16, complementary to D17, is used to notify the Reset Output from Module to Carrier Board, directly driven through an High-Speed Buffer by CB_RESET# signal.

2.3.1 Smart Battery SM Bus Connector

Smart Battery SM Bus Connector – CN29			
Pin	Signal	Pin	Signal
1	SB_SMB_CLK	3	SMB_ALERT#
2	SB_SMB_DAT	4	GND

The SM bus coming from COM Express™ module is carried directly both to the Feature header (see par.3.3.8) and to a JST 4-pin connector CN29, p/n B4B-PH-K-S(LF)(SN), or equivalent, which can be used for the connection of external Smart battery controllers. Pinout as indicated in the left table.



SB_SMB_CLK: Smart Battery System Management bus bidirectional clock line, +3.3V_ALW electrical level with 10kΩ pull up resistor derived by SMB_CK signal

SB_SMB_DAT: Smart Battery System Management bus bidirectional data line, +3.3V_ALW electrical level with 10kΩ pull up resistor derived by SMB_DAT signal

SMB_ALERT#: System Management Bus Alert, active low input to the module that can be used to generate an Interrupt or to wake the system

2.3.2 RTC Battery

For the occurrences when the System (Carrier board + COM Express™ module) is not powered with an external power supply, on board there is a RTC Coin Cell Battery holder CN9, for the use of standard coin battery type CR2032 with a nominal capacity of 220mAh, to supply, with a 3V voltage, the Real Time Clock and CMOS memory mounted on the COM Express™ module.

The batteries should only be replaced with devices of the same type. Always check the orientation before inserting and make sure that they are aligned correctly and are not damaged or leaking.

! CAUTION: handling batteries incorrectly or replacing with not-approved devices may present a risk of fire or explosion.

Never allow the batteries to become short-circuited during handling. Batteries supplied with C79 board are compliant to requirements of European Directive 2006/66/EC regarding batteries and accumulators. When putting out of order C79 board, remove the batteries from the board in order to collect and dispose them according to the requirement of the same European Directive above mentioned. Even when replacing the batteries, the disposal has to be made according to these requirements.

CN6 position	RTC Battery enable
1-2	Battery disconnected
2-3	Battery connected
NO jumper	Current measurement

It is possible to monitor the consumption on VCC_RTC battery by removing the jumper from CN6 connector and inserting a tester in series set as ammeter between 2-3 position.

Alternatively, the consumption on VCC_RTC can be monitored by inserting a tester set as ammeter between pin 1 and 2 of RTC Battery Sense Connector CN5.

CN5 is a dedicated 2 position Wire to Board Terminal Block, type Wurth p/n 691210910002

RTC battery can be enabled/disabled using dedicated jumper on CN6, which is a standard pin header, P2.54mm, 1x3 pin.

JP1 position	Battery Low Indicator enable
Not inserted	Indicator disabled
Inserted	Indicator enabled

The RTC battery voltage level is monitored through a comparator inside the board. Battery low status signal (BATLOW#) is carried to COM-express™ module to be managed.

JP1 is a 2-way jumper to enable/disable this indicator.

2.3.3 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

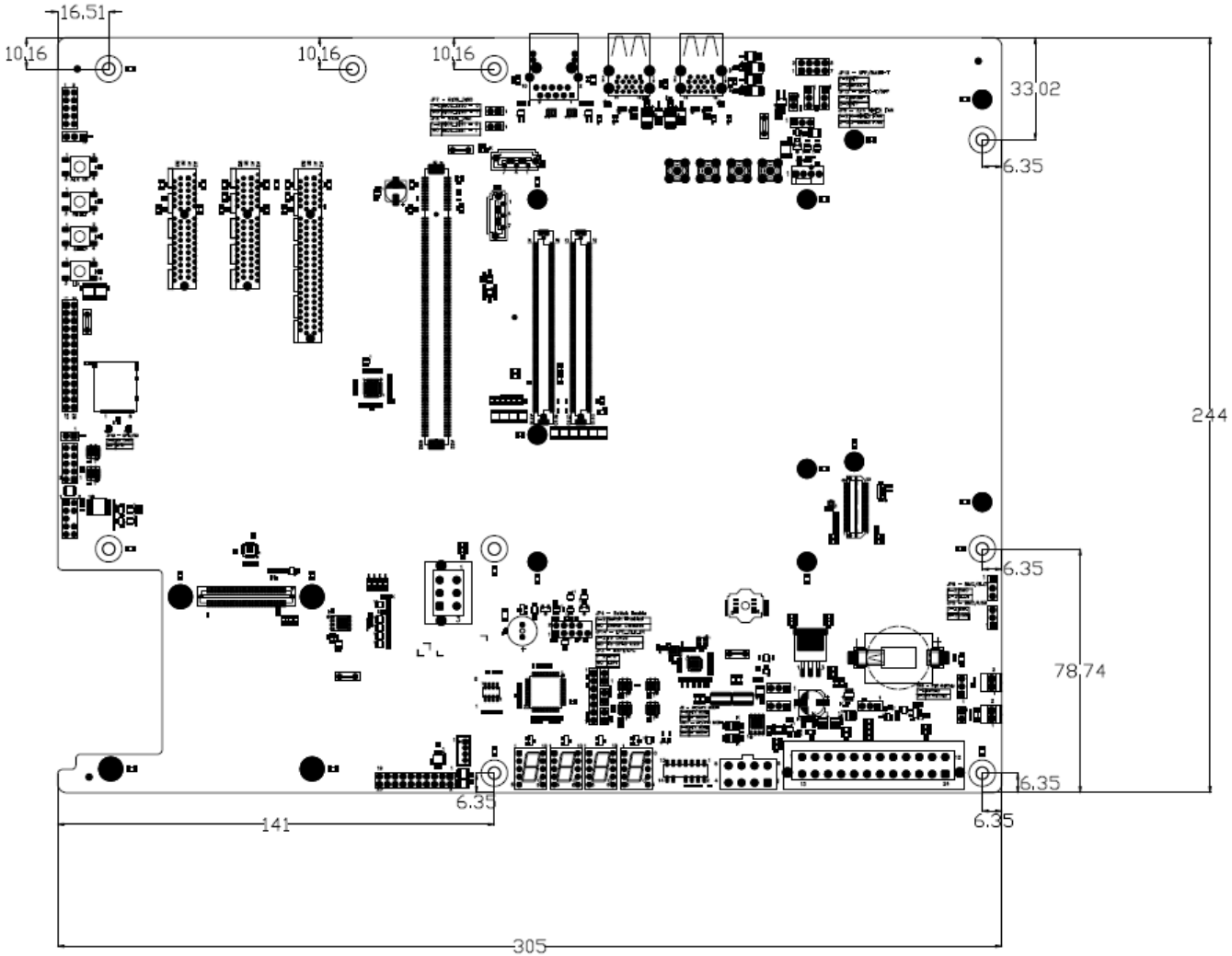
_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

2.4 Mechanical Specifications

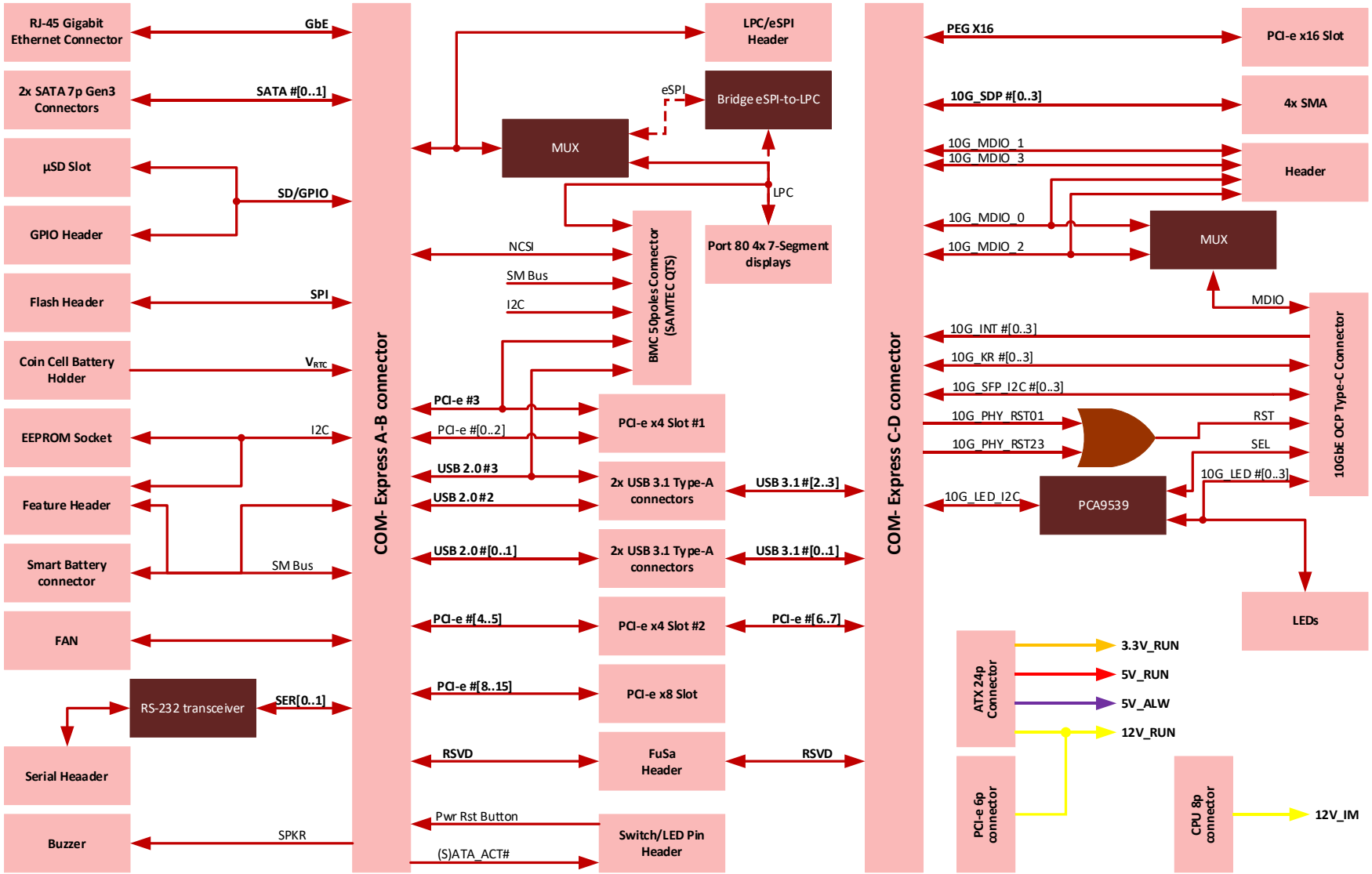
According to ATX form factor, board dimensions are 305 x 244 mm (12” x 9.6”).

The printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

In order to fix the COM Express™ module to the carrier board, on CCOMe-C79 have been soldered six metallic spacers, height 8mm, 2.5mm diameter.



2.5 Block Diagram



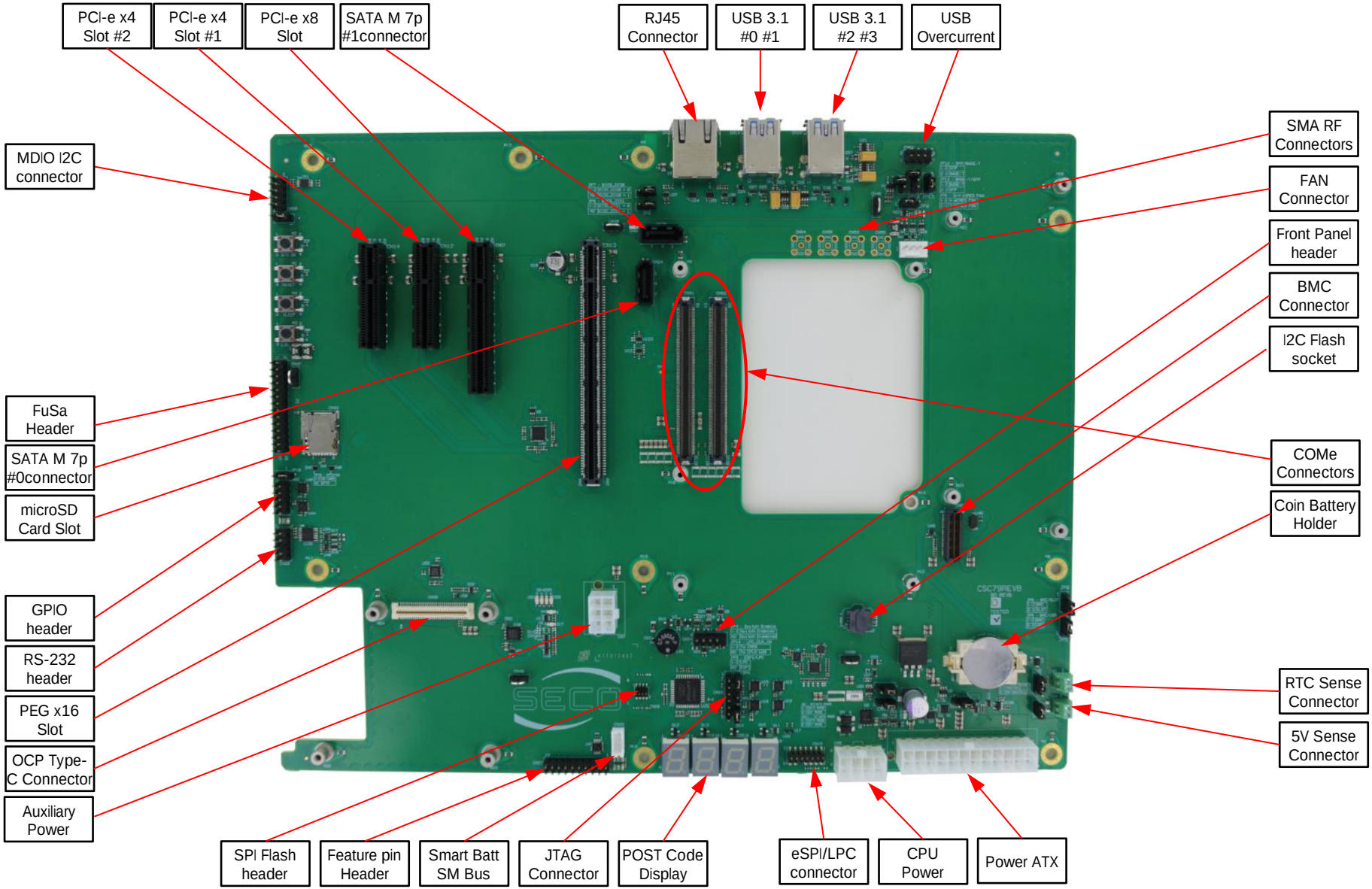
Chapter 3.
CONNECTORS

- Connectors placement
- Connectors overview
- Connectors description

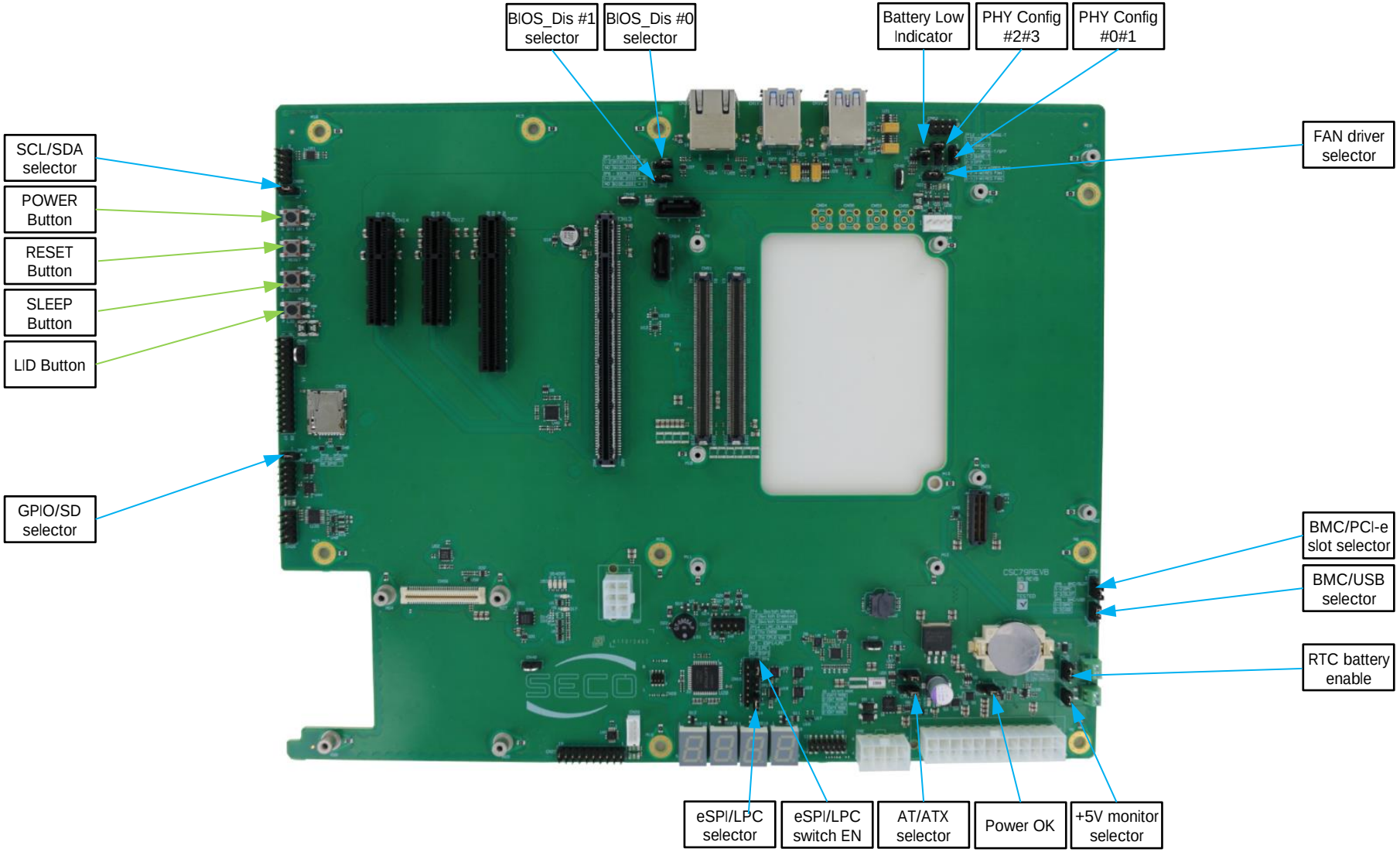
3.1 Connectors placement

On CCOMe-C79 carrier board, there are several connectors. Some of them are standard connectors, like Gigabit Ethernet, USB ports, and are placed on the same side of the board, so that they can be placed on a panel of a possible enclosure.

In the following picture it is possible to see the position of each connector.



JUMPER POSITION



3.2 Connectors overview

3.2.1 Connectors list

Name	Description	Name	Description
CN4	+5V_ALW Sense Connector	CN32	FAN Connector
CN5	RTC Battery Sense Connector	CN33	microSD Card Slot
CN7	Auxiliary Power Connector	CN34	Front Panel Header
CN8	CPU Power Connector	CN51	Com Express, A-B rows connector
CN9	RTC Coin Cell Battery connector	CN52	Com Express, C-D rows connector
CN10	Power ATX connector	CN53	SMA RF Connector for Software Definable Pin (SDP) #0 interface
CN12	PCI-e x4 slot #1	CN54	SMA RF Connector for Software Definable Pin (SDP) #2 interface
CN13	PCI-e x16 Slot / PEG (PCI Express Graphics x16) Connector	CN55	SMA RF Connector for Software Definable Pin (SDP) #1 interface
CN14	PCI-e x4 slot #2	CN56	SMA RF Connector for Software Definable Pin (SDP) #3 interface
CN15	eSPI/LPC Debug Connector	CN57	PCI-e x8 slot
CN16	JTAG Connector	CN58	BMC Connector
CN18	USB 3.1 ports #0 #1 Dual Type-A socket	CN59	10Gbase-KR OCP Type-C Connector
CN19	USB 3.1 ports #2 #3 Dual Type-A socket	CN60	MDIO / I2C Connector
CN23	RJ-45 Gigabit Ethernet Connector	CN62	External EEPROM I2C Flash socket
CN24	SATA M 7-p #0 Connector	CN63	USB Overcurrent header
CN25	SATA M 7-p #1 Connector	J1	FuSa Header
CN26	RS-232 ports Internal pin Header		
CN27	Feature pin Header		
CN28	External BIOS SPI Flash Header		
CN29	Smart Battery SM Bus Connector		
CN31	GPIO pin header		

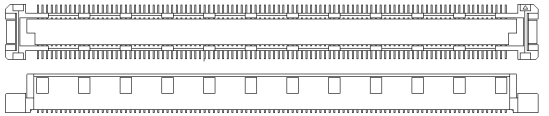
3.2.2 Jumpers and switch list

Name	Description
CN3	Power OK management
CN6	RTC Battery enable
CN11 / J2	AT/ATX mode selectors
JP1	Battery Low Indicator enable
JP2	+5V_ALW Current monitor selector
JP3	eSPI/LPC selector
JP4	eSPI/LPC switch enable
JP5	BMC/USB selector
JP6	BMC/PCI-e slot selector
JP7 / JP8	BIOS Boot selectors
JP9	FAN driver mode selector
JP10	GPIO/SD Card selector
JP11	MDIO/I2C interfaces selector
JP12	Set for 10G_PHY_CAP_23
JP13	Set for 10G_PHY_CAP_01

3.3 Connectors description

3.3.1 COM Express™ module connectors

For the connection of COM Express™ CPU modules, on board there are two connectors, type TYCO 3-6318491-6 (220 pin dual row plug, ultra thin, 0.5mm pitch, h=8mm), as requested by COM Express™ specifications.



The pinout of these connectors will be briefly described in the following paragraphs. Please refer to COM Express™ standard for a better description of each signal.

COM Express™ Connector CN51 - Rows A & B

Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
Power Ground	GND	A1	B1	GND	Power Ground
GbEthernet Differential pair 3-	GBE0_MDI3-	A2	B2	GBE0_ACT#	GbEth Activity indicator
GbEthernet Differential pair 3+	GBE0_MDI3+	A3	B3	LPC_FRAME# / ESPI_CS0#	LPC Frame Indicator / eSPI Chip Select
GbEthernet 100Mb/s link ind.	GBE0_LINK100#	A4	B4	LPC_AD0 / ESPI_IO_0	LPC Address / Data Bus 0 eSPI Master Data Input / Output 0
GbEthernet 1000Mb/s link ind.	GBE0_LINK1000#	A5	B5	LPC_AD1 / ESPI_IO_1	LPC Address / Data Bus 1 eSPI Master Data Input / Output 1
GbEthernet differential pair 2-	GBE0_MDI2-	A6	B6	LPC_AD2 / ESPI_IO_2	LPC Address / Data Bus 2 eSPI Master Data Input / Output 2
GbEthernet Differential pair 2+	GBE0_MDI2+	A7	B7	LPC_AD3 / ESPI_IO_3	LPC Address / Data Bus 3 eSPI Master Data Input / Output 3
GbEthernet link ind.	GBE0_LINK#	A8	B8	LPC_DRQ0# / ESPI_ALERT0#	LPC serial DMA request eSPI Alert request service signal
GbEthernet Differential pair 1-	GBE0_MDI1-	A9	B9	N.C.	Not connected
GbEthernet Differential pair 1+	GBE0_MDI1+	A10	B10	LPC_CLK / ESPI_CK	LPC Clock Output 33MHz eSPI Master Clock Output
Power Ground	GND	A11	B11	GND	Power Ground
GbEthernet Differential pair 0-	GBE0_MDI0-	A12	B12	PWRBTN#	Power Button
GbEthernet Differential pair 0+	GBE0_MDI0+	A13	B13	SMB_CK	SM Bus Clock
GbEthernet Reference Voltage	GBE0_CTREF	A14	B14	SMB_DAT	SM Bus Data
Suspend to RAM (S3) signal	SUS_S3#	A15	B15	SMB_ALERT#	SM Bus Alert signal

SATA0 Transmit Data +	SATA0_TX+	A16	B16	SATA1_TX+	SATA1 Transmit Data +
SATA0 Transmit Data -	SATA0_TX-	A17	B17	SATA1_TX-	SATA1 Transmit Data -
Suspend to Disk (S4) signal	SUS_S4#	A18	B18	SUS_STAT# / ESPI_RESET#	LPC Suspend Mode Indicator eSPI Reset
SATA0 Receive Data +	SATA0_RX+	A19	B19	SATA1_RX+	SATA1 Receive Data +
SATA0 Receive Data -	SATA0_RX-	A20	B20	SATA1_RX-	SATA1 Receive Data -
Power Ground	GND	A21	B21	GND	Power Ground
PCI-E lane 15 transmit +	PCIE_TX15+	A22	B22	PCIE_RX15+	PCI-E lane 15 receive +
PCI-E lane 15 transmit -	PCIE_TX15-	A23	B23	PCIE_RX15-	PCI-E lane 15 receive -
Soft Off (S5) Signal	SUS_S5#	A24	B24	PWR_OK	Power OK signal
PCI-E lane 14 transmit +	PCIE_TX14+	A25	B25	PCIE_RX14+	PCI-E lane 14 receive +
PCI-E lane 14 transmit -	PCIE_TX14-	A26	B26	PCIE_RX14-	PCI-E lane 14 receive -
Low Battery Status Indicator Input	BATLOW#	A27	B27	WDT	Watchdog Event indicator Output
SATA LED	SATA_ACT#	A28	B28	RSVD#B28	Reserved Purpose Signal
Reserved Purpose Signal	RSVD#A29	A29	B29	RSVD#B29	Reserved Purpose Signal (Not connected)
Reserved Purpose Signal	RSVD#A30	A30	B30	RSVD#B30	Reserved Purpose Signal (Not connected)
Power Ground	GND	A31	B31	GND	Power Ground
Reserved Purpose Signal	RSVD#A32	A32	B32	SPKR	Speaker
Reserved Purpose Signal	RSVD#A33	A33	B33	I2C_CK	I2C Clock
BIOS boot device select 0 signal	BIOS_DIS0#	A34	B34	I2C_DAT	I2C Data
Thermal shutdown Status Indicator Output	THRMTRIP#	A35	B35	THRM#	Thermal Alarm Input
PCI-E lane 13 transmit +	PCIE_TX13+	A36	B36	PCIE_RX13+	PCI-E lane 13 receive +
PCI-E lane 13 transmit -	PCIE_TX13-	A37	B37	PCIE_RX13-	PCI-E lane 13 receive -
Power Ground	GND	A38	B38	GND	Power Ground
PCI-E lane 12 transmit +	PCIE_TX12+	A39	B39	PCIE_RX12+	PCI-E lane 12 receive +
PCI-E lane 12 transmit -	PCIE_TX12-	A40	B40	PCIE_RX12-	PCI-E lane 12 receive -
Power Ground	GND	A41	B41	GND	Power Ground
USB Data Port 2 -	USB2-	A42	B42	USB3-	USB Data Port 3-
USB Data Port 2 +	USB2+	A43	B43	USB3+	USB Data Port 3+
USB Over Current Ports 2/3	USB_2_3_OC#	A44	B44	USB_0_1_OC#	USB Over Current Ports 0/1

USB Data Port 0 -	USB0-	A45	B45	USB1-	USB Data Port 1-
USB Data Port 0 +	USB0+	A46	B46	USB1+	USB Data Port 1+
Real Time Clock power line	VCC_RTC	A47	B47	ESPI_EN#	eSPI enable Input
Reserved Purpose Signal	RSVD#A48	A48	B48	N.C.	Not Connected
Not Connected	N.C.	A49	B49	SYS_RESET#	Reset Button Input
LPC serial interrupt request	LPC_SERIRQ	A50	B50	CB_RESET#	Board Reset Output
Power Ground	GND	A51	B51	GND	Power Ground
PCI-E lane 5 transmit +	PCIE_TX5+	A52	B52	PCIE_RX5+	PCI-E lane 5 receive +
PCI-E lane 5 transmit -	PCIE_TX5-	A53	B53	PCIE_RX5-	PCI-E lane 5 receive -
GP Input 0 / SDIO data signal 0	GPI0/SD_DATA0	A54	B54	GPO1/SD_CMD	GP Output 1 / SDIO CMD output
PCI-E lane 4 transmit +	PCIE_TX4+	A55	B55	PCIE_RX4+	PCI-E lane 4 receive +
PCI-E lane 4 transmit -	PCIE_TX4-	A56	B56	PCIE_RX4-	PCI-E lane 4 receive -
Power Ground	GND	A57	B57	GPO2/SD_WP	GP Output 2 / SDIO WP input
PCI-E lane 3 transmit +	PCIE_TX3+	A58	B58	PCIE_RX3+	PCI-E lane 3 receive +
PCI-E lane 3 transmit -	PCIE_TX3-	A59	B59	PCIE_RX3-	PCI-E lane 3 receive -
Power Ground	GND	A60	B60	GND	Power Ground
PCI-E lane 2 transmit +	PCIE_TX2+	A61	B61	PCIE_RX2+	PCI-E lane 2 receive +
PCI-E lane 2 transmit -	PCIE_TX2-	A62	B62	PCIE_RX2-	PCI-E lane 2 receive -
GP Input 1 / SDIO data signal 1	GPI1/SD_DATA1	A63	B63	GPO3/SD_CD#	GP Output 3 / SDIO CD# input
PCI-E lane 1 transmit +	PCIE_TX1+	A64	B64	PCIE_RX1+	PCI-E lane 1 receive +
PCI-E lane 1 transmit -	PCIE_TX1-	A65	B65	PCIE_RX1-	PCI-E lane 1 receive -
Power Ground	GND	A66	B66	WAKE0#	PCI-express wake up signal
GP Input 2 / SDIO data signal 2	GPI2/SD_DATA2	A67	B67	WAKE1#	General purpose wake up signal
PCI-E lane 0 transmit +	PCIE_TX0+	A68	B68	PCIE_RX0+	PCI-E lane 0 receive +
PCI-E lane 0 transmit -	PCIE_TX0-	A69	B69	PCIE_RX0-	PCI-E lane 0 receive -
Power Ground	GND	A70	B70	GND	Power Ground
PCI-E lane 8 transmit +	PCIE_TX8+	A71	B71	PCIE_RX8+	PCI-E lane 8 receive +
PCI-E lane 8 transmit -	PCIE_TX8-	A72	B72	PCIE_RX8-	PCI-E lane 8 receive -
Power Ground	GND	A73	B73	GND	Power Ground
PCI-E lane 9 transmit +	PCIE_TX9+	A74	B74	PCIE_RX9+	PCI-E lane 9 receive +

PCI-E lane 9 transmit -	PCIE_TX9-	A75	B75	PCIE_RX9-	PCI-E lane 9 receive -
Power Ground	GND	A76	B76	GND	Power Ground
PCI-E lane 10 transmit +	PCIE_TX10+	A77	B77	PCIE_RX10+	PCI-E lane 10 receive +
PCI-E lane 10 transmit -	PCIE_TX10-	A78	B78	PCIE_RX10-	PCI-E lane 10 receive -
Power Ground	GND	A79	B79	GND	Power Ground
Power Ground	GND	A80	B80	GND	Power Ground
PCI-E lane 11 transmit +	PCIE_TX11+	A81	B81	PCIE_RX11+	PCI-E lane 11 receive +
PCI-E lane 11 transmit -	PCIE_TX11-	A82	B82	PCIE_RX11-	PCI-E lane 11 receive -
Power Ground	GND	A83	B83	GND	Power Ground
NC-SI Transmit enable	NCSI_TX_EN	A84	B84	+5V_ALW	+5V Standby power line
GP Input 3 / SDIO data signal 3	GPI3/SD_DATA3	A85	B85	+5V_ALW	+5V Standby power line
Reserved Purpose Signal	RSVD#A86	A86	B86	+5V_ALW	+5V Standby power line
Reserved Purpose Signal	RSVD#A87	A87	B87	+5V_ALW	+5V Standby power line
PCI-E Clock reference +	PCIE_CK_REF+	A88	B88	BIOS_DIS1#	BIOS boot device select 1 signal
PCI-E Clock reference -	PCIE_CK_REF-	A89	B89	NCSI_RX_ER	NC-SI Receive error
Power Ground	GND	A90	B90	GND	Power Ground
Power supply for Carrier Board SPI Device	SPI_POWER	A91	B91	NCSI_CLK_IN	NC-SI Clock reference
Data in to Module from Carrier SPI Device	SPI_MISO	A92	B92	NCSI_RXD1	NC-SI Receive Data
GP Output 0 / SDIO Clock	GPO0 / SD_CLK	A93	B93	NCSI_RXD0	NC-SI Receive Data
Clock from Module to Carrier SPI Device	SPI_CLK	A94	B94	NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid
Data out from Module to carrier SPI device	SPI_MOSI	A95	B95	NCSI_TXD1	NC-SI Transmit Data
TPM Physical Presence pin, Active High Input for optional on-board TPM device	TPM_PP	A96	B96	NCSI_TXD0	NC-SI Transmit Data
Type10 signal: Not connected	Type10#	A97	B97	SPI_CS#	SPI Chip Select signal
Module's serial port 0 TX	SER0_TX	A98	B98	NCSI_ARB_IN	NC-SI hardware arbitration input
Module's serial port 0 RX	SER0_RX	A99	B99	NCSI_ARB_OUT	NC-SI hardware arbitration output
Power Ground	GND	A100	B100	GND	Power Ground
Module's serial port 1 TX	SER1_TX	A101	B101	FAN_PWMOUT	FAN Speed control
Module's serial port 1 RX	SER1_RX	A102	B102	FAN_TACHIN	FAN tachometer input
LID button input	LID#	A103	B103	SLEEP#	Sleep Button Input
+12V switched power supply	+12V_RUN	A104	B104	+12V_RUN	+12V switched power supply

+12V switched power supply	+12V_RUN	A105	B105	+12V_RUN	+12V switched power supply
+12V switched power supply	+12V_RUN	A106	B106	+12V_RUN	+12V switched power supply
+12V switched power supply	+12V_RUN	A107	B107	+12V_RUN	+12V switched power supply
+12V switched power supply	+12V_RUN	A108	B108	+12V_RUN	+12V switched power supply
+12V switched power supply	+12V_RUN	A109	B109	+12V_RUN	+12V switched power supply
Power Ground	GND	A110	B110	GND	Power Ground

COM Express™ Connector CN52 - Rows C & D

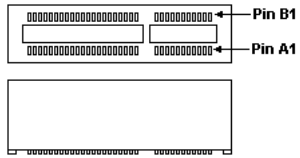
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
Power Ground	GND	C1	D1	GND	Power Ground
Power Ground	GND	C2	D2	GND	Power Ground
SuperSpeed USB receive pair 0-	USB_SSRX0-	C3	D3	USB_SSTX0-	SuperSpeed USB transmit pair 0-
SuperSpeed USB receive pair 0+	USB_SSRX0+	C4	D4	USB_SSTX0+	SuperSpeed USB transmit pair 0+
Power ground	GND	C5	D5	GND	Power ground
SuperSpeed USB receive pair 1-	USB_SSRX1-	C6	D6	USB_SSTX1-	SuperSpeed USB transmit pair 1-
SuperSpeed USB receive pair 1+	USB_SSRX1+	C7	D7	USB_SSTX1+	SuperSpeed USB transmit pair 1+
Power ground	GND	C8	D8	GND	Power ground
SuperSpeed USB receive pair 2-	USB_SSRX2-	C9	D9	USB_SSTX2-	SuperSpeed USB transmit pair 2-
SuperSpeed USB receive pair 2+	USB_SSRX2+	C10	D10	USB_SSTX2+	SuperSpeed USB transmit pair 2+
Power Ground	GND	C11	D11	GND	Power Ground
SuperSpeed USB receive pair 3-	USB_SSRX3-	C12	D12	USB_SSTX3-	SuperSpeed USB transmit pair 3-
SuperSpeed USB receive pair 3+	USB_SSRX3+	C13	D13	USB_SSTX3+	SuperSpeed USB transmit pair 3+
Power Ground	GND	C14	D14	GND	Power Ground
10GbE	10G_PHY_MDC_SCL3	C15	D15	10G_PHY_MDIO_SDA3	10GbE
10GbE	10G_PHY_MDC_SCL2	C16	D16	10G_PHY_MDIO_SDA2	10GbE
10GbE	10G_SDP2	C17	D17	10G_SDP3	10GbE
Power Ground	GND	C18	D18	GND	Power Ground
PCI Express Receive Pair 6+	PCIE_RX6+	C19	D19	PCIE_TX6+	PCI Express Transmit Pair 6+
PCI Express Receive Pair 6-	PCIE_RX6-	C20	D20	PCIE_TX6-	PCI Express Transmit Pair 6-
Power Ground	GND	C21	D21	GND	Power Ground
PCI Express Receive Pair 7+	PCIE_RX7+	C22	D22	PCIE_TX7+	PCI Express Transmit Pair 7+

PCI Express Receive Pair 7-	PCIE_RX7-	C23	D23	PCIE_TX7-	PCI Express Transmit Pair 7-
10GbE	10G_INT2	C24	D24	10G_INT3	10GbE
Power Ground	GND	C25	D25	GND	Power Ground
10GbE	10G_KR_RX3+	C26	D26	10G_KR_TX3+	10GbE
10GbE	10G_KR_RX3-	C27	D27	10G_KR_TX3-	10GbE
Power Ground	GND	C28	D28	GND	Power Ground
10GbE	10G_KR_RX2+	C29	D29	10G_KR_TX2+	10GbE
10GbE	10G_KR_RX2-	C30	D30	10G_KR_TX2-	10GbE
Power Ground	GND	C31	D31	GND	Power Ground
10GbE	10G_SFP_SDA3	C32	D32	10G_SFP_SCL3	10GbE
10GbE	10G_SFP_SDA2	C33	D33	10G_SFP_SCL2	10GbE
10GbE	10G_PHY_RST_23	C34	D34	10G_PHY_CAP_23	10GbE
10GbE	10G_PHY_RST_01	C35	D35	10G_PHY_CAP_01	10GbE
10GbE	10G_LED_SDA	C36	D36	RSVD#D36	Reserved Purpose Signal
10GbE	10G_LED_SCL	C37	D37	RSVD#D37	Reserved Purpose Signal
10GbE	10G_SFP_SDA1	C38	D38	10G_SFP_SCL1	10GbE
10GbE	10G_SFP_SDA0	C39	D39	10G_SFP_SCL0	10GbE
10GbE	10G_SDP0	C40	D40	10G_SDP1	10GbE
Power Ground	GND	C41	D41	GND	Power Ground
10GbE	10G_KR_RX1+	C42	D42	10G_KR_TX1+	10GbE
10GbE	10G_KR_RX1-	C43	D43	10G_KR_TX1-	10GbE
Power Ground	GND	C44	D44	GND	Power Ground
10GbE	10G_PHY_MDC_SCL1	C45	D45	10G_PHY_MDIO_SDA1	10GbE
10GbE	10G_PHY_MDC_SCL0	C46	D46	10G_PHY_MDIO_SDA0	10GbE
10GbE	10G_INT0	C47	D47	10G_INT1	10GbE
Power Ground	GND	C48	D48	GND	Power Ground
10GbE	10G_KR_RX0+	C49	D49	10G_KR_TX0+	10GbE
10GbE	10G_KR_RX0-	C50	D50	10G_KR_TX0-	10GbE
Power Ground	GND	C51	D51	GND	Power Ground
PCI Express Receive Pair 16+	PCIE_RX16+	C52	D52	PCIE_TX16+	PCI Express Transmit Pair 16+

PCI Express Receive Pair 16-	PCIE_RX16-	C53	D53	PCIE_TX16-	PCI Express Transmit Pair 16-
Type0 signal: +5V_ALW	TYPE0#	C54	D54	RSVD#D54	Reserved Purpose Signal
PCI Express Receive Pair 17+	PCIE_RX17+	C55	D55	PCIE_TX17+	PCI Express Transmit Pair 17+
PCI Express Receive Pair 17-	PCIE_RX17-	C56	D56	PCIE_TX17-	PCI Express Transmit Pair 17-
Type1 signal: Not Connected	TYPE1#	C57	D57	TYPE2#	Type2 signal: +5V_ALW
PCI Express Receive Pair 18+	PCIE_RX18+	C58	D58	PCIE_TX18+	PCI Express Transmit Pair 18+
PCI Express Receive Pair 18-	PCIE_RX18-	C59	D59	PCIE_TX18-	PCI Express Transmit Pair 18-
Power Ground	GND	C60	D60	GND	Power Ground
PCI Express Receive Pair 19+	PCIE_RX19+	C61	D61	PCIE_TX19+	PCI Express Transmit Pair 19+
PCI Express Receive Pair 19-	PCIE_RX19-	C62	D62	PCIE_TX19-	PCI Express Transmit Pair 19-
Reserved Purpose Signal	RSVD#C63	C63	D63	RSVD#D63	Reserved Purpose Signal
Reserved Purpose Signal	RSVD#C64	C64	D64	RSVD#D64	Reserved Purpose Signal
PCI Express Receive Pair 20+	PCIE_RX20+	C65	D65	PCIE_TX20+	PCI Express Transmit Pair 20+
PCI Express Receive Pair 20-	PCIE_RX20-	C66	D66	PCIE_TX20-	PCI Express Transmit Pair 20-
Not Connected	N.C.	C67	D67	GND	Power Ground
PCI Express Receive Pair 21+	PCIE_RX21+	C68	D68	PCIE_TX21+	PCI Express Transmit Pair 21+
PCI Express Receive Pair 21-	PCIE_RX21-	C69	D69	PCIE_TX21-	PCI Express Transmit Pair 21-
Power Ground	GND	C70	D70	GND	Power Ground
PCI Express Receive Pair 22+	PCIE_RX22+	C71	D71	PCIE_TX22+	PCI Express Transmit Pair 22+
PCI Express Receive Pair 22-	PCIE_RX22-	C72	D72	PCIE_TX22-	PCI Express Transmit Pair 22-
Power Ground	GND	C73	D73	GND	Power Ground
PCI Express Receive Pair 23+	PCIE_RX23+	C74	D74	PCIE_TX23+	PCI Express Transmit Pair 23+
PCI Express Receive Pair 23-	PCIE_RX23-	C75	D75	PCIE_TX23-	PCI Express Transmit Pair 23-
Power Ground	GND	C76	D76	GND	Power Ground
Reserved Purpose Signal	RSVD#C77	C77	D77	RSVD#D77	Not Connected
PCI Express Receive Pair 24+	PCIE_RX24+	C78	D78	PCIE_TX24+	PCI Express Transmit Pair 24+
PCI Express Receive Pair 24-	PCIE_RX24-	C79	D79	PCIE_TX24-	PCI Express Transmit Pair 24-
Power Ground	GND	C80	D80	GND	Power Ground
PCI Express Receive Pair 25+	PCIE_RX25+	C81	D81	PCIE_TX25+	PCI Express Transmit Pair 25+
PCI Express Receive Pair 25-	PCIE_RX25-	C82	D82	PCIE_TX25-	PCI Express Transmit Pair 25-

Reserved Purpose Signal	RSVD#C83	C83	D83	RSVD#D83	Not Connected
Power Ground	GND	C84	D84	GND	Power Ground
PCI Express Receive Pair 26+	PCIE_RX26+	C85	D85	PCIE_TX26+	PCI Express Transmit Pair 26+
PCI Express Receive Pair 26-	PCIE_RX26-	C86	D86	PCIE_TX26-	PCI Express Transmit Pair 26-
Power Ground	GND	C87	D87	GND	Power Ground
PCI Express Receive Pair 27+	PCIE_RX27+	C88	D88	PCIE_TX27+	PCI Express Transmit Pair 27+
PCI Express Receive Pair 27-	PCIE_RX27-	C89	D89	PCIE_TX27-	PCI Express Transmit Pair 27-
Power Ground	GND	C90	D90	GND	Power Ground
PCI Express Receive Pair 28+	PCIE_RX28+	C91	D91	PCIE_TX28+	PCI Express Transmit Pair 28+
PCI Express Receive Pair 28-	PCIE_RX28-	C92	D92	PCIE_TX28-	PCI Express Transmit Pair 28-
Power Ground	GND	C93	D93	GND	Power Ground
PCI Express Receive Pair 29+	PCIE_RX29+	C94	D94	PCIE_TX29+	PCI Express Transmit Pair 29+
PCI Express Receive Pair 29-	PCIE_RX29-	C95	D95	PCIE_TX29-	PCI Express Transmit Pair 29-
Power Ground	GND	C96	D96	GND	Power Ground
Reserved Purpose Signal	RSVD#C97	C97	D97	RSVD#D97	Not Connected
PCI Express Receive Pair 30+	PCIE_RX30+	C98	D98	PCIE_TX30+	PCI Express Transmit Pair 30+
PCI Express Receive Pair 30-	PCIE_RX30-	C99	D99	PCIE_TX30-	PCI Express Transmit Pair 30-
Power Ground	GND	C100	D100	GND	Power Ground
PCI Express Receive Pair 31+	PCIE_RX31+	C101	D101	PCIE_TX31+	PCI Express Transmit Pair 31+
PCI Express Receive Pair 31-	PCIE_RX31-	C102	D102	PCIE_TX31-	PCI Express Transmit Pair 31-
Power Ground	GND	C103	D103	GND	Power Ground
+12V switched power supply	+12V_RUN	C104	D104	+12V_RUN	+12V switched power supply
+12V switched power supply	+12V_RUN	C105	D105	+12V_RUN	+12V switched power supply
+12V switched power supply	+12V_RUN	C106	D106	+12V_RUN	+12V switched power supply
+12V switched power supply	+12V_RUN	C107	D107	+12V_RUN	+12V switched power supply
+12V switched power supply	+12V_RUN	C108	D108	+12V_RUN	+12V switched power supply
+12V switched power supply	+12V_RUN	C109	D109	+12V_RUN	+12V switched power supply
Power Ground	GND	C110	D110	GND	Power Ground

3.3.2 PCI-e Slots



CCOMe-C79 board offer a possibility of expansion through two standard PCI-e x4 and one standard PCI-e x8 card edge connectors, PCI-e x4 card edge connectors are type WINWIN p/n WPES-064AN41B22UWC or equivalent, with the pinout shown in the following table.

PCI-e x8 card edge connectors are type WINWIN p/n WPES-098AN41B22UWC or equivalent, with the pinout shown in the following table.

On first slot CN12, are carried out PCI-e lanes #0..#3 coming from COM Express™ connector (rows A-B).

On second slot CN14, are carried out PCI-e lanes #4..#7 coming from COM Express™ connector (rows A-B-C-D).

On second slot CN57, are carried out PCI-e lanes #8..#15 coming from COM Express™ connector (rows A-B).

Please be aware that availability of all sixteen PCI express lanes depends on the COM Express™ module used.

Please check the User Manual of the COM Express™ module used for details about the availability of these lanes and all possible groupings that can be applied to these lanes.

On CCOMe-C79 carrier board, the PCI-express compatibility is ensured with devices up to Gen3.

PCI-e x 4 Slot CN12					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	PRSNT1#	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	Not connected
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	Not connected
Power Ground	GND	B7	A7	JTAG4	Not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	Not connected
Not Connected	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx4_1_RST#	Reset signal to the add-in card, derived by

					CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIEx4_1_CLK_P	PCI-e reference clock lane +, derived by PCIE_CK_REF+ using a Clock Buffer
PCI-e Transmitter lane 0+	PCIE_TX0+	B14	A14	PCIEx4_1_CLK_N	PCI-e reference clock lane +, derived by PCIE_CK_REF- using a Clock Buffer
PCI-e Transmitter lane 0-	PCIE_TX0-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX0+	PCI-e Receiver lane 0+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX0-	PCI-e Receiver lane 0-
Power Ground	GND	B18	A18	GND	Power Ground
PCI-e Transmitter lane 1+	PCIE_TX1+	B19	A19	RSVD	Not Connected
PCI-e Transmitter lane 1-	PCIE_TX1-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX1+	PCI-e Receiver lane 1+
Power Ground	GND	B22	A22	PCIE_RX1-	PCI-e Receiver lane 1-
PCI-e Transmitter lane 2+	PCIE_TX2+	B23	A23	GND	Power Ground
PCI-e Transmitter lane 2-	PCIE_TX2-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX2+	PCI-e Receiver lane 2+
Power Ground	GND	B26	A26	PCIE_RX2-	PCI-e Receiver lane 2-
PCI-e Transmitter lane 3+. Signal available to this slot by setting jumper JP6 in 2-3 position.	PCIE_TX3+	B27	A27	GND	Power Ground
PCI-e Transmitter lane 3-. Signal available to this slot by setting jumper JP6 in 2-3 position.	PCIE_TX3-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX3+	PCI-e Receiver lane 3+. Signal available to this slot by setting jumper JP6 in 2-3 position.
Not Connected	RSVD	B30	A30	PCIE_RX3-	PCI-e Receiver lane 3-. Signal available to this slot by setting jumper JP6 in 2-3 position.
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a	PRSNT2#	B31	A31	GND	Power Ground

10kΩ pull down resistor.					
Power Ground	GND	B32	A32	RSVD	Not Connected
PCI-e x 4 Slot CN14					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	PRSNT1#	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	Not connected
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	Not connected
Power Ground	GND	B7	A7	JTAG4	Not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	Not connected
Not Connected	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx4_2_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIEx4_2_CLK_P	PCI-e reference clock lane +, derived by PCIE_CK_REF+ using a Clock Buffer
PCI-e Transmitter lane 4+	PCIE_TX4+	B14	A14	PCIEx4_2_CLK_N	PCI-e reference clock lane +, derived by PCIE_CK_REF- using a Clock Buffer
PCI-e Transmitter lane 4-	PCIE_TX4-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX4+	PCI-e Receiver lane 4+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX4-	PCI-e Receiver lane 4-

Power Ground	GND	B18	A18	GND	Power Ground
PCI-e Transmitter lane 5+	PCIE_TX5+	B19	A19	RSVD	Not Connected
PCI-e Transmitter lane 5-	PCIE_TX5-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX5+	PCI-e Receiver lane 5+
Power Ground	GND	B22	A22	PCIE_RX5-	PCI-e Receiver lane 5-
PCI-e Transmitter lane 6+	PCIE_TX6+	B23	A23	GND	Power Ground
PCI-e Transmitter lane 6-	PCIE_TX6-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX6+	PCI-e Receiver lane 6+
Power Ground	GND	B26	A26	PCIE_RX6-	PCI-e Receiver lane 6-
PCI-e Transmitter lane 7+	PCIE_TX7+	B27	A27	GND	Power Ground
PCI-e Transmitter lane 7-	PCIE_TX7-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX7+	PCI-e Receiver lane 7+
Not Connected	RSVD	B30	A30	PCIE_RX7-	PCI-e Receiver lane 7-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not Connected

Please be aware that PCI-e management on CCOMe-C79 carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

PCI-e x 8 Slot CN52					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	PRSNT1#	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	Not connected
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	Not connected
Power Ground	GND	B7	A7	JTAG4	Not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	Not connected
Not Connected	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx8_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIEx8_CLK_P	PCI-e reference clock lane +, derived by PCIE_CK_REF+ using a Clock Buffer
PCI-e Transmitter lane 8+	PCIE_TX8+	B14	A14	PCIEx8_CLK_N	PCI-e reference clock lane +, derived by PCIE_CK_REF- using a Clock Buffer
PCI-e Transmitter lane 8-	PCIE_TX8-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX8+	PCI-e Receiver lane 8+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX8-	PCI-e Receiver lane 8-
Power Ground	GND	B18	A18	GND	Power Ground
PCI-e Transmitter lane 9+	PCIE_TX9+	B19	A19	RSVD	Not Connected

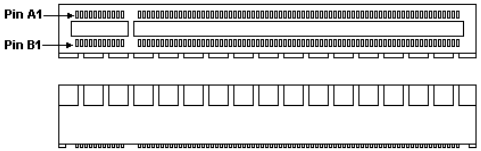
PCI-e Transmitter lane 9-	PCIE_TX9-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX9+	PCI-e Receiver lane 9+
Power Ground	GND	B22	A22	PCIE_RX9-	PCI-e Receiver lane 9-
PCI-e Transmitter lane 10+	PCIE_TX10+	B23	A23	GND	Power Ground
PCI-e Transmitter lane 10-	PCIE_TX10-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX10+	PCI-e Receiver lane 10+
Power Ground	GND	B26	A26	PCIE_RX10-	PCI-e Receiver lane 10-
PCI-e Transmitter lane 11+	PCIE_TX11+	B27	A27	GND	Power Ground
PCI-e Transmitter lane 11-	PCIE_TX11-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX11+	PCI-e Receiver lane 11+
Not Connected	RSVD	B30	A30	PCIE_RX11-	PCI-e Receiver lane 11-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not Connected
PCI-e Transmitter lane 12+	PCIE_TX12+	B33	A33	RSVD	Not Connected
PCI-e Transmitter lane 12-	PCIE_TX12-	B34	A34	GND	Power Ground
Power Ground	GND	B35	A35	PCIE_RX12+	PCI-e Receiver lane 12+
Power Ground	GND	B36	A36	PCIE_RX12-	PCI-e Receiver lane 12-
PCI-e Transmitter lane 13+	PCIE_TX13+	B37	A37	GND	Power Ground
PCI-e Transmitter lane 13-	PCIE_TX13-	B38	A38	GND	Power Ground
Power Ground	GND	B39	A39	PCIE_RX13+	PCI-e Receiver lane 13+
Power Ground	GND	B40	A40	PCIE_RX13-	PCI-e Receiver lane 13-
PCI-e Transmitter lane 14+	PCIE_TX14+	B41	A41	GND	Power Ground
PCI-e Transmitter lane 14-	PCIE_TX14-	B42	A42	GND	Power Ground
Power Ground	GND	B43	A43	PCIE_RX14+	PCI-e Receiver lane 14+
Power Ground	GND	B44	A44	PCIE_RX14-	PCI-e Receiver lane 14-
PCI-e Transmitter lane 15+	PCIE_TX15+	B45	A45	GND	Power Ground
PCI-e Transmitter lane 15-	PCIE_TX15-	B46	A46	GND	Power Ground
Power Ground	GND	B47	A47	PCIE_RX15+	PCI-e Receiver lane 15+

Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B48	A48	PCIE_RX15-	PCI-e Receiver lane 15-
Power Ground	GND	B49	A49	GND	Power Ground

! Please be aware that PCI-e management on CCOMe-C79 carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B48/B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B48 or B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

3.3.3 PCI-e x16 Slot / PEG (PCI Express Graphics x16) Connector



CCOMe-C79 board offer a possibility of additional expansion through one standard PCI-e x16 card edge connector CN13.

PCI-e x16 card edge connector is type LOTES p/n APCI0599-P002C01or equivalent, with the pinout shown in the following table.

On this CN13 slot, are carried out PCI-e lanes #16..#31 coming from COM Express™ connector (rows C-D).

It is also possible to use this connector to add the graphical capabilities of the board by using PCI-e lanes #16..#31 as PCI Express Graphics x16 bus (PEG) interface.

Please be aware that availability of these PCI express lanes depends on the COM Express™ module used.

Please check the User Manual of the COM Express™ module used for details about the availability of these lanes and all possible groupings that can be applied to these lanes.

PCI Express Graphics x16 Slot- CN13					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	GND	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	TCK, tied to GND with 4K7Ω resistor
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	TDI, tied to +3.3V_RUN with 4K7Ω resistor
Power Ground	GND	B7	A7	JTAG4	Test Data Out, not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	TMS, tied to +3.3V_RUN with 4K7Ω resistor
TRST#, tied to GND with 4K7Ω resistor	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx16_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground

Power Ground	GND	B13	A13	PCIEx16_CLK_P	PCI-e reference clock lane +, derived by PCIE_CK_REF+ using a Clock Buffer
PCI Express Transmit Pair 16+	PCIE_TX16+	B14	A14	PCIEx16_CLK_N	PCI-e reference clock lane +, derived by PCIE_CK_REF- using a Clock Buffer
PCI Express Transmit Pair 16-	PCIE_TX16-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX16+	PCI Express Receive Pair 16+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX16-	PCI Express Receive Pair 16-
Power Ground	GND	B18	A18	GND	Power Ground
PCI Express Transmit Pair 17+	PCIE_TX17+	B19	A19	RSVD	Not connected
PCI Express Transmit Pair 17-	PCIE_TX17-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX17+	PCI Express Receive Pair 17+
Power Ground	GND	B22	A22	PCIE_RX17-	PCI Express Receive Pair 17-
PCI Express Transmit Pair 18+	PCIE_TX18+	B23	A23	GND	Power Ground
PCI Express Transmit Pair 18-	PCIE_TX18-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX18+	PCI Express Receive Pair 18+
Power Ground	GND	B26	A26	PCIE_RX18-	PCI Express Receive Pair 18-
PCI Express Transmit Pair 19+	PCIE_TX19+	B27	A27	GND	Power Ground
PCI Express Transmit Pair 19-	PCIE_TX19-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX19+	PCI Express Receive Pair 19+
Not Connected	RSVD	B30	A30	PCIE_RX19-	PCI Express Receive Pair 19-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not connected
PCI Express Transmit Pair 20+	PCIE_TX20+	B33	A33	RSVD	Not connected
PCI Express Transmit Pair 20-	PCIE_TX20-	B34	A34	GND	Power Ground
Power Ground	GND	B35	A35	PCIE_RX20+	PCI Express Receive Pair 20+
Power Ground	GND	B36	A36	PCIE_RX20-	PCI Express Receive Pair 20-

PCI Express Transmit Pair 21+	PCIE_TX21+	B37	A37	GND	Power Ground
PCI Express Transmit Pair 21-	PCIE_TX21-	B38	A38	GND	Power Ground
Power Ground	GND	B39	A39	PCIE_RX21+	PCI Express Receive Pair 21+
Power Ground	GND	B40	A40	PCIE_RX21-	PCI Express Receive Pair 21-
PCI Express Transmit Pair 22+	PCIE_TX22+	B41	A41	GND	Power Ground
PCI Express Transmit Pair 22-	PCIE_TX22-	B42	A42	GND	Power Ground
Power Ground	GND	B43	A43	PCIE_RX22+	PCI Express Receive Pair 22+
Power Ground	GND	B44	A44	PCIE_RX22-	PCI Express Receive Pair 22-
PCI Express Transmit Pair 23+	PCIE_TX23+	B45	A45	GND	Power Ground
PCI Express Transmit Pair 23-	PCIE_TX23-	B46	A46	GND	Power Ground
Power Ground	GND	B47	A47	PCIE_RX23+	PCI Express Receive Pair 23+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B48	A48	PCIE_RX23-	PCI Express Receive Pair 23-
Power Ground	GND	B49	A49	GND	Power Ground
PCI Express Transmit Pair 24+	PCIE_TX24+	B50	A50	RSVD	Not connected
PCI Express Transmit Pair 24-	PCIE_TX24-	B51	A51	GND	Power Ground
Power Ground	GND	B52	A52	PCIE_RX24+	PCI Express Receive Pair 24+
Power Ground	GND	B53	A53	PCIE_RX24-	PCI Express Receive Pair 24-
PCI Express Transmit Pair 25+	PCIE_TX25+	B54	A54	GND	Power Ground
PCI Express Transmit Pair 25-	PCIE_TX25-	B55	A55	GND	Power Ground
Power Ground	GND	B56	A56	PCIE_RX25+	PCI Express Receive Pair 25+
Power Ground	GND	B57	A57	PCIE_RX25-	PCI Express Receive Pair 25-
PCI Express Transmit Pair 26+	PCIE_TX26+	B58	A58	GND	Power Ground
PCI Express Transmit Pair 26-	PCIE_TX26-	B59	A59	GND	Power Ground
Power Ground	GND	B60	A60	PCIE_RX26+	PCI Express Receive Pair 26+
Power Ground	GND	B61	A61	PCIE_RX26-	PCI Express Receive Pair 26-
PCI Express Transmit Pair 27+	PCIE_TX27+	B62	A62	GND	Power Ground
PCI Express Transmit Pair 27-	PCIE_TX27-	B63	A63	GND	Power Ground
Power Ground	GND	B64	A64	PCIE_RX27+	PCI Express Receive Pair 27+

Power Ground	GND	B65	A65	PCIE_RX27-	PCI Express Receive Pair 27-
PCI Express Transmit Pair 28+	PCIE_TX28+	B66	A66	GND	Power Ground
PCI Express Transmit Pair 28-	PCIE_TX28-	B67	A67	GND	Power Ground
Power Ground	GND	B68	A68	PCIE_RX28+	PCI Express Receive Pair 28+
Power Ground	GND	B69	A69	PCIE_RX28-	PCI Express Receive Pair 28-
PCI Express Transmit Pair 29+	PCIE_TX29+	B70	A70	GND	Power Ground
PCI Express Transmit Pair 29-	PCIE_TX29-	B71	A71	GND	Power Ground
Power Ground	GND	B72	A72	PCIE_RX29+	PCI Express Receive Pair 29+
Power Ground	GND	B73	A73	PCIE_RX29-	PCI Express Receive Pair 29-
PCI Express Transmit Pair 30+	PCIE_TX30+	B74	A74	GND	Power Ground
PCI Express Transmit Pair 30-	PCIE_TX30-	B75	A75	GND	Power Ground
Power Ground	GND	B76	A76	PCIE_RX30+	PCI Express Receive Pair 30+
Power Ground	GND	B77	A77	PCIE_RX30-	PCI Express Receive Pair 30-
PCI Express Transmit Pair 31+	PCIE_TX31+	B78	A78	GND	Power Ground
PCI Express Transmit Pair 31-	PCIE_TX31-	B79	A79	GND	Power Ground
Power Ground	GND	B80	A80	PCIE_RX31+	PCI Express Receive Pair 31+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B81	A81	PCIE_RX31-	PCI Express Receive Pair 31-
Not Connected	RSVD	B82	A82	GND	Power Ground

!

Please be aware that PCI-e management on CCOMe-C79 carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B81/B48/B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B81 or B48 or B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

3.3.4 eSPI/LPC Debug Connector

eSPI/LPC Debug Connector – CN15			
Pin	Signal	Pin	Signal
1	LPC_CLK/ESPI_CK	2	SUS_STAT#/ESPI_RESET#
3	LPC_RST#	4	+3.3V_RUN
5	LPC_AD0/ESPI_IO_0	6	LPC_DRQ0#/ESPI_ALERT0#
7	LPC_AD1/ESPI_IO_1	8	LPC_SERIRQ#/ESPI_CS1#
9	LPC_AD2/ESPI_IO_2		
11	LPC_AD3/ESPI_IO_3	12	GND
13	LPC_FRAME#/ESPI_CS0#	14	GND

The COM Express™ card edge connector shares on the same pins both the LPC and the eSPI interface. Please check the COM Express™ module to see whether LPC or eSPI interface is made available.

The signals of these pins are first of all carried directly to an internal dual row 6+7 pin header CN15, type NELTRON p/n 2208SM-14G-E10-CR or equivalent, with the pinout shown in the table on the left.

If LPC bus is available from selected COM Express™ module, then following signals will be present:

LPC_CLK: LPC Clock Output 33MHz

LPC_RST#: when jumper JP3 is inserted, this signal is derived by CB_RESET# signal or simply by biasing it using a Ultra High Speed CMOS buffer. When jumper JP3 is not inserted, this signal is derived by an eSPI to LPC bridge placed on carrier board.

LPC_AD[0:3]: LPC address, command and data bus, bidirectional signal

LPC_FRAME#: LPC Frame indicator, active low output signal. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

SUS_STAT#: Signal indicating suspend status output. It is used to notify LPC devices that the module is going to enter in one of possible ACPI low-power states

LPC_DRQ0#: LPC serial DMA request input signal

LPC_SERIRQ#: LPC Serialised IRQ request, bidirectional signal

Otherwise, if eSPI interface is available from selected COM Express™ module, then following signals will be present:

ESPI_CK: eSPI Master Clock Output

ESPI_IO_[0:3]: eSPI Master Data Input / Outputs. These are bi-directional input/output signals used to transfer data between master and slaves

ESPI_CS0#: eSPI Master Chip Select #0. Active low output signal

ESPI_CS1#: eSPI Master Chip Select #1. Active low output signal

ESPI_RESET#: eSPI Reset Signal for both master and slaves devices

ESPI_ALERT0#: eSPI signal used by eSPI slave to request service from the eSPI master

JP4 position	JP3 position	eSPI/LPC interface
Not inserted	Not Care	eSPI/LPC interface disabled
Inserted	Not inserted	eSPI interface from COM Express™ module
Inserted	Inserted	LPC interface from COM Express™ module

LPC /eSPI interface, in addition to eSPI/LPC Debug Connector CN15, is carried to the rest of the carrier board and its routing is managed by JP3 and JP4 selection 2-way jumpers.

JP4 selection jumper is used to enable / disable the eSPI/LPC interface for the rest of the carrier board, meaning that when not inserted this interface is made available only at CN15 debug connector.

If the eSPI/LPC interface is enabled with JP4 inserted, JP3 is the selector for the type of interface coming from COM Express™ module. When not inserted, meaning that eSPI interface is available from COM Express™ module, LPC bus is implemented by using an eSPI-to-LPC bridge. Otherwise, when inserted, meaning that LPC bus is directly available, without the need of the bridge.

For both cases, this LPC bus is carried to BMC connector CN58 (par. 3.3.18), and to a CPLD, which manages four seven-segment LCD display, used to show the POST codes transmitted on ports 80h and 84h.

3.3.5 RS232 ports Internal pin Headers

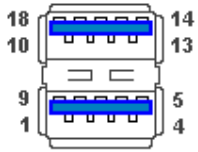
RS232 Internal pin Header- CN26			
Pin	Signal	Pin	Signal
1	UART0_232_RX	2	UART1_232_RX
3	UART0_232_TX	4	UART1_232_TX
5	GND		
7	N.C.	8	N.C.
9	N.C.	10	N.C.

COM Express™ modules foresee a maximum of 2 Serial Ports with only Tx and Rx signals (SER #0 and SER #1).

These two ports are managed though a single RS-232 transceiver, type MaxLinear p/n SP3232EEY-L, and the output is available on an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E06 or equivalent.

3.3.6 USB ports

USB 3.1 ports #0 / #1- CN18			
Pin	**Signal**	**Pin**	**Signal**
1	$+5V_{USB0}$	10	$+5V_{USB1}$
2	USB0-	11	USB1-
3	USB0+	12	USB1+
4	GND	13	GND
5	USB_SSRX0-	14	USB_SSRX1-
6	USB_SSRX0+	15	USB_SSRX1+
7	GND	16	GND
8	USB_SSTX0-	17	USB_SSTX1-
9	USB_SSTX0+	18	USB_SSTX1+



The CCOMe-C79 Carrier board offers the possibility of using all the possible USB ports that are foreseen for COM Express™ Type 7 modules.

The signals of USB 3.0 ports #0 ÷ #1 are carried to a double type-A USB 3.1 stacked receptacle, type Winning p/n WDU3R-18F1B4PBUW3 or equivalent.

More specifically, USB 3.1 port #0 is carried to the lower USB receptacle of CN18, while USB 3.1 port #1 is carried to the upper USB receptacle of CN18.

Since this connector is a standard type receptacle, it can be connected to all types of USB 1.1 / USB 2.0 / USB 3.0 devices using Standard-A USB 3.0 or USB 2.0 plugs.

For USB 3.0 connections it is mandatory the use of SuperSpeed certified cables, whose SuperSpeed differential pairs are individually shielded inside the global cable's external shielding.

Signal description:

USB0+/USB0-: USB 2.0 Port #0 differential pair

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair

USB1+/USB1-: USB 2.0 Port #1 differential pair

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair

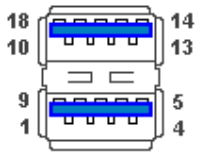
USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair

Common mode chokes are placed on all USB differential pairs for EMI compliance.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

$+5V_{USB0}$ and $+5V_{USB1}$ are derived from +5V_ALW through a 1A current limited power switch.

USB 3.1 ports #2 / #3- CN19			
Pin	Signal	Pin	Signal
1	$+5V_{USB2}$	10	$+5V_{USB3}$
2	USB2-	11	USB3-
3	USB2+	12	USB3+
4	GND	13	GND
5	USB_SSRX2-	14	USB_SSRX3-
6	USB_SSRX2+	15	USB_SSRX3+
7	GND	16	GND
8	USB_SSTX2-	17	USB_SSTX3-
9	USB_SSTX2+	18	USB_SSTX3+



The signals of USB 3.0 ports #2 ÷ #3 are carried to another double type-A USB 3.1 stacked receptacle, type Winning p/n WDU3R-18F1B4PBUW3 or equivalent.

More specifically, USB 3.1 port #2 is carried to the lower USB receptacle of CN19, while USB 3.1 port #3 is carried to the upper USB receptacle of CN19.

Since this connector is a standard type receptacle, it can be connected to all types of USB 1.1 / USB 2.0 / USB 3.0 devices using Standard-A USB 3.0 or USB 2.0 plugs.

For USB 3.0 connections it is mandatory the use of SuperSpeed certified cables, whose SuperSpeed differential pairs are individually shielded inside the global cable's external shielding.

Signal description:

USB2+/USB2-: USB 2.0 Port #2 differential pair

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair

USB3+/USB3-: USB 2.0 Port #3 differential pair

USB_SSRX3+/USB_SSRX3-: USB Super Speed Port #3 receive differential pair

USB_SSTX3+/USB_SSTX3-: USB Super Speed Port #3 transmit differential pair

Common mode chokes are placed on all USB differential pairs for EMI compliance

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

$+5V_{USB2}$ and $+5V_{USB3}$ are derived from +5V_ALW through a 1A current limited power switch.

! Please be aware that USB 3.0 connectivity can be obtained only in case that it is supported by the COM Express™ module plugged onto the Carrier Board.

In case the COM Express™ module used doesn't offer USB 3.0 ports, it will be always possible to use USB 2.0 ports, simply by plugging an USB 2.0 cable. Avoid using USB 3.0 cables if the COM Express™ module used doesn't offer such an interface.

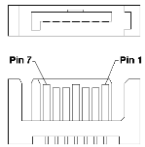
USB Overcurrent header – CN63			
Pin	Signal	Pin	Signal
1	GND	2	USB_0_1_OC#
3	GND	4	USB_2_3_OC#
5	GND	6	N.C.
7	GND	8	N.C.

For debugging purposes, onboard it is also available an 8-pin connector, type Adimpex p/n LE008208-R or equivalent, for the connection of USBx_EN_OC# signals.

USB_0_1_OC#: USB over-current sense signal for USB channels #0 and #1. Active Low Input Signal, electrical level +3.3V_ALW, manged by COM Express™ module.

USB_2_3_OC#: USB over-current sense signal for USB channels #2 and #3. Active Low Input Signal, electrical level +3.3V_ALW, manged by COM Express™ module.

3.3.7 S-ATA Connectors



For the connection of external Mass Storage Devices, there are two standard male 7 poles SATA connectors,CN24,CN25, type WINNING p/n WATM-07ABN4B2B8UW or equivalent.

These connectors carry out directly SATA port #0 and SATA port #1 signals coming from COM Express™ module's connector.

Each SATA channel is composed by two differential pairs, SATA_TxX and SATA_RxX.

Please notice that each SATA connector will work only in case the COM Express™ module carries out SATA Channel #0 and #1 on COM Express™ connector.

In case the COM Express™ module used doesn't have these signals connected, then one or more of these connectors will not be usable.

SATA #0 Connector – CN24	
Pin	**Signal**
1	GND
2	SATA0_Tx+
3	SATA0_Tx-
4	GND
5	SATA0_Rx-
6	SATA0_Rx+
7	GND

SATA #1 Connector – CN25	
Pin	**Signal**
1	GND
2	SATA1_Tx+
3	SATA1_Tx-
4	GND
5	SATA1_Rx-
6	SATA1_Rx+
7	GND

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair.

SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair.

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair.

3.3.8 Feature pin Header

Feature internal pin header – CN27			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V_ALW (with 1.5 resettable fuse)	2	+3.3V_RUN (with 1.5 resettable fuse)
3	SMB_CK	4	I2C_CK
5	SMB_DAT	6	I2C_DAT
7	GND	8	GND
9	THRMTRIP#	10	THRM#
11	BUF_SUS_S5#	12	BUF_SUS_S4#
13	BUF_SUS_S3#	14	WDT
15	PWRBTN#	16	WAKE1#
17	SLEEP#	18	TPM_PP
19	GND	20	GND

For further expandability of the system, on board there is an expansion connector, which carries out the signals related to I2C bus, SM Bus, Watchdog and Power Management signals. These signals allow implementing, through external expansion modules, further functionalities that are not already realised by the carrier board.

For this purpose, it is available a dual row, 20 pin, P2.54mm standard pin header, type ADIMPEX p/n LE008220-R or equivalent, with the pinout shown in the table on the left.

All the signals available on this connector come out directly from the COM Express™ connector.

Signal description:

SMB_CK: SM Bus control clock line for System Management, bidirectional signal

SMB_DAT: SM Bus control data line for System Management, bidirectional signal

I2C_CK: General purpose I2C port clock output

I2C_DAT: General purpose I2C port data I/O line

THRMTRIP#: Active low output signal. This signal is used to communicate that, due to excessive overheating, the CPU has entered thermal shutdown in order to prevent physical damages

THRM#: Thermal Alarm Input from off-Module temperature sensor indicating an overheating situation, so that the CPU can begin thermal throttling. Active Low Input signal

BUF_SUS_S3#: this signal, in reality, doesn't come directly from COM Express™ module, it is biased using a Ultra High Speed CMOS buffer. Active Low Output Signal, +3.3V_ALW electrical level with 100kΩ pull down resistor, indicating that the system is in Suspend to RAM (S3) state.

BUF_SUS_S4#: this signal, in reality, doesn't come directly from COM Express™ module, it is biased using a Ultra High Speed CMOS buffer. Active Low Output Signal, +3.3V_ALW electrical level with 100kΩ pull down resistor, indicating that the system is in Suspend to Disk (S4) state.

BUF_SUS_S5#: this signal, in reality, doesn't come directly from COM Express™ module, it is biased using a Ultra High Speed CMOS buffer. Active Low Output Signal, +3.3V_ALW electrical level with 100kΩ pull down resistor, indicating that the system is in Soft Off (S5) state.

WDT: Watchdog event indicator Output. When this signal goes high (active), it reports that internal Watchdog's timer expired without being triggered, neither via HW nor via SW. It is an active high signal

PWRBTN#: Power Button event signal input, used to bring a system out of S5 soft off and other suspend states, as well as powering the system down. Active low output signal. This signal can be directly driven by M2 pushbutton (par.3.3.20) and upon its pressure, the pulse of this signal will let the switched voltage rails turn on or off.

WAKE1#: General Purpose Input wake up signal used to report that a general Wake-up event has occurred, and consequently the module must turn itself on. Active Low Input signal

SLEEP#: Sleep Button event signal input, used to bring a system in sleep state or wake it up again. Active Low Input signal. This signal can be directly driven by M4 pushbutton (par. 3.3.203.3.20) and upon its pressure, the pulse of this signal will let the transition of the module from Working to Sleep status, or vice versa.

TPM_PP: Trusted Platform Module (TPM) Physical Presence, Active high Input Signal

3.3.9 External BIOS SPI Flash header

External BIOS Flash Header – CN28			
Pin	**Signal**	**Pin**	**Signal**
1	SPI_CS#	2	SPI_POWER
3	SPI_MISO	4	SPI_HOLD#
5	SPI_WP#	6	SPI_CLK
7	GND	8	SPI_MOSI

In case that an external Flash is needed, then on the carrier board it is provided access to this interface through a dual-row 8-pin SMT male pin-header, p. 1.27mm, type TOWNES P1035-2*04MGF-084-D or equivalent, with pinout shown in the table on the left.

Signal description:

SPI_CS#: Chip Select Signal for SPI device, Active Low Output Signal, SPI_POWER electrical level

SPI_MISO: Data in to COM Express™ Module from Carrier SPI device

SPI_WP#: this signal is tied, through a 10kΩ resistor, to SPI_POWER signal. This means that when the Flash is powered, the protection from writing is automatically removed.

SPI_POWER: Dedicated Power supply sourced from COM Express™ Module for SPI devices. +3.3V or +1.8V electrical level depending on the module.

SPI_HOLD#: this signal too is tied, through a 10kΩ resistor, to SPI_POWER signal. This means that when the Flash is powered, the Hold condition of serial communication is automatically removed.

SPI_CLK: Clock from COM Express™ Module to Carrier SPI device

SPI_MOSI: Data out from COM Express™ Module to Carrier SPI device

3.3.10 BIOS disable signals

According to COM Express™ Specifications rev. 3.0, there are two jumpers on board JP7 and JP8, which allow configuring the BIOS_DIS[0..1]# signals according to the table below.

JP8 position	JP7 position	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	BIOS Entry
Not inserted	Not inserted	Module	Module	High	Module	SPI0/SPI1
Not inserted	Inserted	Module	Module	High	Module	Carrier FWH
Inserted	Not inserted	Module	Carrier	SPI0	Carrier	SPI0/SPI1
Inserted	Inserted	Carrier	Module	SPI1	Module	SPI0/SPI1

3.3.11 FuSa Header

FuSa Header – J1			
Pin	**Signal**	**FuSa Interface**	**Raw FuSa Interface**
1	+5V_ALW (with 1.5 resettable fuse)		
2	+12V_RUN (with 1.5 resettable fuse)		
3	GND		
4	GND		
5	RSVD#D36	FUSA_OKNOK0	FUSA_ERR0
6	RSVD#D37	FUSA_OKNOK1	FUSA_ERR1
7	RSVD#D54	FUSA_ALERT#	FUSA_ERR2
8	RSVD#D63	FUSA_SPIS_CS#	FUSA_SPI_CS#
9	RSVD#D64	FUSA_SPIS_SCLK	FUSA_SPI_SCLK
10	RSVD#D77	FUSA_SPIS_MISO	FUSA_SPI_MISO
11	RSVD#D83	FUSA_SPIS_MOSI	FUSA_SPI_MOSI
12	RSVD#D97	FUSA_CHXPMICEN_IN	FUSA_CHXPMICEN_IN
13	RSVD#A29	FUSA_CHXPMIC_EN	
14	RSVD#B28	FUSA_CHXRLYSWITCH	
15	RSVD#A30	FUSA_CHXOKNOK0	FUSA_GPP_U5
16	RSVD#C83	FUSA_CHXOKNOK1	FUSA_GPP_U4
17	RSVD#A32	FUSA_SPIM_CS#	FUSA_I2C_CLK
18	RSVD#C97	FUSA_SPIM_SCLK	FUSA_I2C_DAT
19	RSVD#A33	FUSA_SPIM_MISO	FUSA_DIAGTEST_MODE
20	RSVD#C63	FUSA_SPIM_MOSI	FUSA_DIAGTEST_EN
21	RSVD#A48	FUSA_PROCHOT	FUSA_PROCHOT#
22	RSVD#C64	FUSA_THERMTRIP	FUSA_THERMTRIP#
23	RSVD#A86		FUSA_CATERR#

According to COM Express™ Specifications rev. 3.0, the COM Express™ card edge connector does provide additional reserved signals intended to be used for future use.

On CCOMe-C79 Carrier Board, these signals are carried out to a dual row, 28 pin, P2.54mm standard pin header, type ADIMPEX p/n LE008228-R, with the pinout shown in the table on the left.

This connector is used to provide functional safety functions for FuSa applications through signals listed in left table.

Please be aware that FuSa functionality can be obtained only in case that it is supported by the COM Express™ module plugged onto the Carrier Board.

Please refer to specific COM Express™ module for a signal description related to this section.

24	RSVD#C77		FUSA_PCHHOT#
25	RSVD#A87	FUSA_POWERFAIL#	FUSA_POWERFAIL#
26	SYS_RESET#		
27	PS_ON#		
28	PWRBTN#		

3.3.12 GPIO pin header / microSD Card Slot

GPIO pin header – CN31			
Pin	**Signal**	**Pin**	**Signal**
1	GPO0	2	+3.3V_ALW (with 1.5 resettable fuse)
3	GPO1	4	GPI0
5	GPO2	6	GPI1
7	GPO3	8	GPI2
9	GND	10	GPI3

JP10 position	GPIO/microSD selector
Not inserted	GPIO
Inserted	microSD

According to the release 3.0 of COM Express™ specifications, on the same pins are multiplexed the signals necessary for the implementation of 4-bit SD cards with four General Purpose Inputs plus four general Purpose Outputs. Effective support of GPI+GPO signals or SDIO interface depends on the module used. Please refer to the User Manual of the COM Express™ module used for a detail about the interface support.

The selection between SD Card interface and GPI/O interface is made using jumper JP10, according to the table on the left.

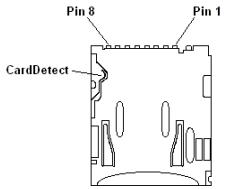
If supported by the COM Express™ module installed on CCOMe-C79, the GPIO interface, is available on CN31, which is a dual row, 10 pin, P2.54mm standard pin header, type ADIMPEX p/n LE008210-R, with the pinout shown in the table on the left. To redirect the signal coming directly from COM Express™ module to GPIO header, jumper JP10 doesn't have to be inserted.

GPO[0:3]: General purpose output signals

GPI[0:3]: General purpose input signals

µSD Card Slot – CN33	
Pin	**Signal**
1	SDIO_DAT2
2	SDIO_DAT3
3	SDIO_CMD
4	+3.3V_RUN
5	SDIO_CLK
6	GND
7	SDIO_DAT0
8	SDIO_DAT1
CardDetect	SD_CD#

The SD interface is carried to a standard µSD card slot (CN33), soldered on bottom side of the module, push-push type, H=1.68 mm, type JST DM3AT-SF-PEJM5 or equivalent. When this interface is available, this card slot is accessible with jumper JP10 inserted.



Signals description

SD_CD#: Card Detect Input. This signal is grounded when the card is inserted.

SD_CLK: SD Clock Line (output).

SD_CMD: Command/Response bidirectional line.

SDIO_DAT[0÷3]: SD Card data bus. SDIO_DAT0 signal is used for all communication modes. SDIO_DAT[1÷3] signals are required for 4-bit communication mode.

3.3.13 Front Panel Header

Switch / LED Header Interface - CN34			
Pin	**Signal**	**Pin**	**Signal**
1	HD_LED_P	2	FP PWR_P/SLP_N
3	HD_LED_N	4	FP PWR_N/SLP_P
5	RST_SW_N	6	PWR_SW_P
7	RST_SW_P	8	PWR_SW_N
9	+5V_RUN		

To allow the integration of a COM Express™ module based system inside a box PC-like, there is a connector on the carrier board that allows to remote signals for the Power Button (to be used to put the system in a Soft Off State, or awake from it), for the Reset Button, and the signal for optional LED signalling activity on SATA Channel and Power On states.

The pinout of this connector complies with Intel® Front Panel I/O connectivity Design Guide, Switch/LED Front Panel section, chapter 2.2.

Connector CN34 is an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E10 or equivalent.

Signals Description:

HD_LED_P: Hard Disk Activity LED signal's pull-up to +5V_RUN voltage (510Ω pull-up).

HD_LED_N: Hard Disk Activity LED output signal.

RST_SW_N: Reset Switch GND.

RST_SW_P: Reset switch input signal SYS_RESET#. This signal can be connected to an external momentary pushbutton (contacts normally open). When the pushbutton is pressed, the pulse of Reset signal will cause the reset of the board.

PWR_SW_P: Power switch input signal PWRBTN#. This signal can be connected to an external momentary pushbutton (contacts normally open). Upon the pressure of this pushbutton, the pulse of this signal will let the switched voltage rails turn on or off.

PWR_SW_N: Power Switch GND.

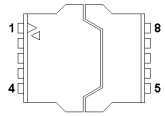
FP PWR_P/SLP_N: Power/Sleep messaging LED terminal 1 with 510Ω pull-up resistor to +5V_ALW voltage. Connect it to an extremity of a dual-colour power LED for power ON/OF, sleep and message waiting signalling. Please refer to Intel® Front Panel I/O connectivity Design Guide, chapter 2.2.4, for LED functionalities and signal meaning.

FP PWR_N/SLP_P: Power/Sleep messaging LED terminal 2 with 510Ω pull-up resistor to +5V_ALW voltage. Connect it to the other extremity of the dual-colour power LED above mentioned.

Please be aware that the power switch input signal and the reset switch input signal are also managed directly on the carrier board by the two pushbuttons M2 and M1 (respectively), so it is not mandatory to connect them externally using CN34.

3.3.14 External EEPROM I2C Flash socket

External EEPROM I2C Flash socket – CN62			
Pin	Signal	Pin	Signal
1	4.7kΩ pull-up +3.3V_ALW	5	I2C_DAT
2	4.7kΩ pull-up +3.3V_ALW	6	I2C_CK
3	4.7kΩ pull-up +3.3V_ALW	7	I2C_Write Protect (GND)
4	GND	8	+3.3V_ALW



The I2C bus coming from COM Express™ module is carried directly to Feature pin Header (see par.3.3.8).

It is also used to manage an SO8 EEPROM Socket CN62, type LOTES p/n ASPI0001-P001A, for plugging I2C Flash in SO-8 format.

The I2C_Write Protect function is disabled for this board (signal tied to GND).

I2C_DAT: General purpose I2C port data I/O line

I2C_CK: General purpose I2C port clock output

3.3.15 POST Code Display

For debugging purposes, it is available a display made by 4x 7-segment LED display, type Kingbright KCSC02-105 or equivalent.

The management of this display is done using a Lattice LC4064V-75TN44I CPLD, driven through the COM Express™ LPC Bus

3.3.16 JTAG Connector

JTAG Connector – CN16			
Pin	Signal	Pin	Signal
1	+3.3V_RUN	5	POST_TDO
2	GND	6	POST_TDI
3	POST_TCK	7	POST_TMS
4	N.C.		

For the programming of CPLD used to manage POST Code Display, it is available a JTAG connector CN16, which is a single row, 7 pin, P2.54mm standard pin header, type ADIMPEX p/n NPE08007-R.

POST_TCK: JTAG Test Clock Signal, 4k7Ω pull down resistor to GND

POST_TDO: JTAG Test Data Out Signal

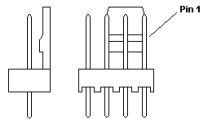
POST_TDI: JTAG Test Data In, +3.3V_RUN with 4k7Ω pull up resistor

POST_TMS: JTAG Test Mode Select, +3.3V_RUN with 4k7Ω pull up resistor

3.3.17 FAN Connector

FAN Connector – CN32	
Pin	**Signal**
1	GND
2	FAN_PWR
3	FAN_TACHO_IN
4	FAN_PWM

Onboard it is available a 4-pin connector, type MOLEX p/n 47053-3000 or equivalent, for the connection of tachometric FANs. Please be aware that the use of an external fan depends strongly on customer's application/installation. Fan Speed control must be supported by COM Express™ module through signals FAN_TACHIN and FAN_PWMOUT. Please refer to chapter 4.1 for considerations about thermal dissipation.



FAN_PWR: +12V_RUN derived power rail for FAN, managed by PWM signal FAN_PWMOUT coming from COM Express™ connector. FAN_PWR is fixed +12V_RUN in 4-wires Fan, while is pulse width modulated via FAN_PWMOUT for 3-wires Fan

FAN_TACHO_IN: tachometric input from the fan to the COM Express™ module

FAN_PWM: PWM output to the fan, +5V_RUN electrical level with 10kΩ pull up resistor. Only used in 4-wires Fan.

JP9 position	FAN driver mode selector
1-2	4-Wires Fan
2-3	3-Wires Fan

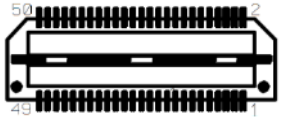
As stated above, by using a dedicate jumper JP9, it is possible to select if FAN_PWR is fixed to +12V_RUN, in order to support 4-wire tachometric fans, or must be controlled by the signal FAN_PWMOUT, coming directly from COM Express™ module, in order to support 3-wire tachometric fans.

3.3.18 BMC Connector

BMC connector – CN58			
Pin	Signal	Pin	Signal
1	+5V_ALW	2	+3.3V_ALW
3	+5V_ALW	4	+3.3V_ALW
5	+5V_ALW	6	+3.3V_ALW
7	---	8	GND
9	GND	10	LPC_CLK (N.C.)
11	SMB_CK	12	LPC_RST# (N.C.)
13	SMB_DAT	14	LPC_SERIRQ# (N.C.)
15	GND	16	LPC_AD0 (N.C.)
17	I2C_CK	18	LPC_AD1 (N.C.)
19	I2C_DAT	20	LPC_AD2 (N.C.)
21	GND	22	LPC_AD3 (N.C.)
23	USB3+	24	LPC_FRAME# (N.C.)
25	USB3-	26	GND
27	GND	28	PCIE_BMC_CLK-
29	NCSI_CLK_IN	30	PCIE_BMC_CLK+
31	NCSI_RXD0	32	GND
33	NCSI_RXD1	34	BMC_CLK_REQ#
35	NCSI_CRS_DV	36	PCIE_BMC_RST#
37	NCSI_TXD0	38	GND
39	NCSI_TXD1	40	PCIE_BMC_RX3+
41	NCSI_ARB_OUT	42	PCIE_BMC_RX3-
43	NCSI_ARB_IN	44	GND
45	NCSI_TX_EN	46	PCIE_BMC_TX3+
47	NCSI_RX_ER	48	PCIE_BMC_TX3-
49	GND	50	GND

COM Express™ MC79 Carrier Board expands its functionalities by means of connector CN58, to be used for plugging Baseboard Management Controller (BMC) modules.

This connector does include multiple interfaces, SM Bus, I2C, LPC Bus, 1x USB 2.0, 1x PCI-e x1, NCSI signals. CN58, type SAMTEC QStrip® p/n QTS-025-01-L-D-A with the pinout on left table.



I2C bus coming from COM Express™ module is carried directly to Feature header (see par.3.3.8) and to the BMC Connector. It is also used to manage an SO8 EEPROM Socket CN63, for plugging I2C Flash in SO-8 format.

Also LPC bus and SM bus are carried to BCM Connector.

PCI-e lane #3 is shared between PCI-e slot #1 CN12 and BCM connector.

A dedicated 2 way jumper JP6 is used to redirect the PCI-e lane #3.

PCI-e reference clock for BMC is provided by the on Carrier board PCI-e Clock buffer.

Another interface shared with BCM connector is USB 2.0 port #3. This interface is switched using a jumper JP5 to the BMC Connector.

JP5 position	BMC/USB selector
1-2	BMC
2-3	USB Port#3 (CN19)

JP6 position	BMC/PCI-e slot selector
1-2	BMC
2-3	PCI-e Slot (CN12)

Signals Description:

SMB_CK: SM Bus control clock line for System Management, bidirectional signal

SMB_DAT: SM Bus control data line for System Management, bidirectional signal

I2C_CK: General purpose I2C port clock output

I2C_DAT: General purpose I2C port data I/O line

USB3+/USB3-: USB 2.0 Port #3 differential pair

NCSI_CLK_IN: NC-SI 50MHz reference Clock input for Rx, Tx and control interfaces

NCSI_RXD0: NC-SI Receive Data #0 Output, from Network Controller placed on Type 7 modules to external BMC

NCSI_RXD1: NC-SI Receive Data #1 Output, from Network Controller placed on Type 7 modules to

external BMC

NCSI_TXD0: NC-SI Transmit Data #0 Input, from external BMC to Network Controller placed on Type 7 modules

NCSI_TXD1: NC-SI Transmit Data #1 Input, from external BMC to Network Controller placed on Type 7 modules

NCSI_CRS_DV: NC-SI Carrier Sense/Receive Data Valid Output, from Network Controller placed on Type 7 modules to external BMC

NCSI_TX_EN: NC-SI Transmit Enable Input, from external BMC to Network Controller placed on Type 7 modules

NCSI_RX_ER: NC-SI Receive Error Output, managed by Network Controller placed on Type 7 modules

NCSI_ARB_IN: NC-SI Hardware arbitration Input from external BMC to Network Controller placed on Type 7 modules

NCSI_ARB_OUT: NC-SI Hardware arbitration Output from Network Controller placed on Type 7 modules to external BMC

LPC_CLK: LPC Clock Output 33MHz

LPC_RST#: when jumper JP3 is inserted, this signal is derived by CB_RESET# signal or simply by biasing it using a Ultra High Speed CMOS buffer. When jumper JP3 is not inserted, this signal is derived by an eSPI to LPC bridge placed on carrier board. Active low Output signal

LPC_AD[0:3]: LPC address, command and data bus, bidirectional signal

LPC_FRAME#: LPC Frame indicator, active low output line. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition

LPC_DRQ0#: LPC serial DMA request input signal

LPC_SERIRQ#: LPC Serialised IRQ request, bidirectional signal

PCIE_BMC_CLK+/PCIE_BMC_CLK-: PCI Express Reference Clock, Differential Pair. This signal is obtained by a zero-delay clock buffer placed on Carrier Board.

BMC_CLK_REQ#: PCI Express Clock Request Input. This signal shall be driven correctly by any module inserted in the BMC connector, in order to ensure that the PCI-e clock buffer available on the carrier board makes available the reference clock for the external BMC module. +3.3V_RUN electrical level with 10kΩ pull up resistor

PCIE_BMC_RST#: Reset Input Signal for external BMC module, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor

PCIE_BMC_RX3+ / PCIE_BMC_RX3-: PCI Express lane #3, Receiving Input Differential pair

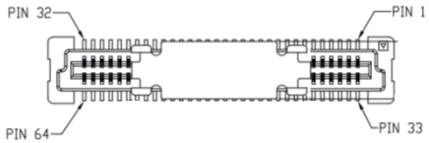
PCIE_BMC_TX3+ / PCIE_BMC_TX3- : PCI Express lane #3, Transmitting Output Differential pair

3.3.19 Networking

10Gbase-KR OCP Type-C Connector – CN59			
Pin	Signal	Pin	Signal
1	OCP_SMB_CK	26	10G_SFP_SCL1
2	OCP_SMB_DAT	27	10G_SFP_SDA1
3	EXT_MDIO_I2C_SEL	28	GND
4	GND	29	10G_SFP_SCL3
5	10G_KR_TX2+	30	10G_SFP_SDA3
6	10G_KR_TX2-	31	10G_INT2
7	GND	32	10G_INT3
8	10G_LED1_2#	33	+VIN_OCP
9	10G_LED1_0#	34	+VIN_OCP
10	GND	35	+VIN_OCP
11	10G_KR_TX3+	36	RST
12	10G_KR_TX3-	37	10G_INT0
13	GND	38	10G_INT1
14	10G_LED2_2#	39	GND
15	10G_LED2_0#	40	10G_KR_TX0+
16	GND	41	10G_KR_TX0-
17	10G_KR_RX2+	42	GND
18	10G_KR_RX2-	43	10G_LED0_2#
19	GND	44	10G_LED0_0#
20	10G_SFP_SCL0	45	GND
21	10G_SFP_SDA0	46	10G_KR_TX1+
22	GND	47	10G_KR_TX1-
23	10G_KR_RX3+	48	GND
24	10G_KR_RX3-	49	10G_PHY_MDC_OCP_SCL
25	GND	50	10G_PHY_MDC_OCP_SDA

First introduced with COM Express™ Specifications Revision 3.0, COM Express Type 7 modules can offer up to four 10GBase-KR interfaces, where the MAC is located on the module and the PHY is located on the carrier.

To make MC79 Carrier board more flexible, the PHYs are not directly implemented in the carrier board. The signals necessary for their management, instead, are carried to an OCP Type-C connector CN59, i.e. a board-to-board connector type AMPHENOL P/N 10135583-641402LF.



The MC79 Carrier Board is equipped with two jumpers JP12 and JP13, which indicate if the PHY for 10G lanes can be driven only via MDIO or if I2C/MDIO is supported.

JP12 refers to configurability for 10G lanes #2 #3 and is used to drive input signal 10G_PHY_CAP_23 for the module.

JP13 refers to configurability for 10G lanes #0 #1 and is used to drive input signal 10G_PHY_CAP_01 for the module.

JP12 position	Set for 10G_PHY_CAP_23
1-2	MDIO-only
2-3	MDIO/I2C

JP13 position	Set for 10G_PHY_CAP_01
1-2	MDIO-only
2-3	MDIO/I2C

Instead, one of the MDIO/I2C interfaces #0 and #2 can also be selected for OCP connector's pins #49 and #50. Switching is controlled via Jumper JP11.

JP11 position	Controlled by signals:
1-2	10G_PHY_MDIO_SDA0 / 10G_PHY_MDC_SCL0
2-3	10G_PHY_MDIO_SDA2 / 10G_PHY_MDC_SCL2

51	GND	58	10G_KR_RX1+
52	10G_KR_RX0+	59	10G_KR_RX1-
53	10G_KR_RX0-	60	GND
54	GND	61	10G_SFP_SCL2
55	10G_LED3_2#	62	10G_SFP_SDA2
56	10G_LED3_0#	63	GND
57	GND	64	N.C.

Signals Description:

10G_KR_TX0+/10G_KR_TX0-: 10GBASE-KR port #0 Transmit output differential pair

10G_KR_RX0+/10G_KR_RX0-: 10GBASE-KR port #0 Receive Input differential pair

10G_KR_TX1+/10G_KR_TX1-: 10GBASE-KR port #1 Transmit output differential pair

10G_KR_RX1+/10G_KR_RX1-: 10GBASE-KR port #1 Receive Input differential pair

10G_KR_TX2+/10G_KR_TX2-: 10GBASE-KR port #2 Transmit output differential pair

10G_KR_RX2+/10G_KR_RX2-: 10GBASE-KR port #2 Receive Input differential pair

10G_KR_TX3+/10G_KR_TX3-: 10GBASE-KR port#3 Transmit output differential pair

10G_KR_RX3+/10G_KR_RX3-: 10GBASE-KR port#3 Receive Input differential pair

10G_LED0_0#: Status /Activity Indicator for LED signalling of PHY #0 controller. Active low Output Signal, +3.3V_ALW electrical level

10G_LED0_2#: Link speed Indicator for LED signalling of PHY #0 controller. Active low Output Signal, +3.3V_ALW electrical level

10G_LED1_0#: Status /Activity Indicator for LED signalling of PHY #1 controller. Active low Output Signal, +3.3V_ALW electrical level

10G_LED1_2#: Link speed Indicator for LED signalling of PHY #1 controller. Active low Output Signal, +3.3V_ALW electrical level

10G_LED2_0#: Status /Activity Indicator for LED signalling of PHY #2 controller. Active low Output Signal, +3.3V_ALW electrical level

10G_LED2_2#: Link speed Indicator for LED signalling of PHY #2 controller. Active low Output Signal, +3.3V_ALW electrical level

10G_LED3_0#: Status /Activity Indicator for LED signalling of PHY #2 controller. Active low Output Signal, +3.3V_ALW electrical level

10G_LED3_2#: Link speed Indicator for LED signalling of PHY #2 controller. Active low Output Signal, +3.3V_ALW electrical level

EXT_MDIO_I2C_SEL: Output selection signal for the PHY indicating if the transfer is made by I2C mode (signal tied to GND) or by MDIO mode (signal tied to +3.3V_ALW)

10G_SFP_SCL[0:3]: I2C clock signal of the 2-wire management interface used by the10GbE controller to access the management registers of an external Optical SFP Module

10G_SFP_SDA[0:3]: I2C data signal of the 2-wire management interface used by the10GbE controller to access the management registers of an external Optical SFP Module

10G_INT[0:3]: Interrupt input signal from copper PHY or optical SFP Module to the 10GbE controller

OCP_SMB_CK: SM Bus control clock line for OCP System Management. Bidirectional signal, +3.3V_RUN electrical level with 10kΩ pull up resistor

OCP_SMB_DAT: SM Bus control data line for OCP System Management. Bidirectional signal, +3.3V_RUN electrical level with 10kΩ pull up resistor

10G_PHY_MDC_OCP_SCL: Management Data I/O Interface mode (MDIO mode) or I2C (I2C mode) clock signal for serial data transfers between the MAC and an external PHY. Its routing to OCP connector is controlled by JP11 to select which I2C/MDIO lane is selected, and its capability mode (MDIO-only or MDIO/I2C) is regulated by JP12 (PHI lane#2 and#3) and JP13 (PHI lane#0 and#1)

10G_PHY_MDC_OCP_SDA: Management Data I/O Interface mode (MDIO mode) or I2C (I2C mode) data signal for serial data transfers between the MAC and an external PHY. Its routing to OCP connector is controlled by JP11 to select which I2C/MDIO lane is selected, and its operating mode (MDIO-only or MDIO/I2C) is regulated by JP12 (PHI lane#2 and#3) and JP13 (PHI lane#0 and#1)

+VIN_OCP: Power for external OCP module. It will be +5V_ALW when the module is turned off, while +12V_RUN when is turned on

MDIO / I2C Connector - CN60			
Pin	**Signal**	**Pin**	**Signal**
1	10G_PHY_MDC_SCL2	2	10G_PHY_MDC_SCL0
3	10G_PHY_MDIO_SDA2	4	10G_PHY_MDIO_SDA0
5	10G_PHY_MDC_SCL3	6	10G_PHY_MDC_SCL1
7	10G_PHY_MDIO_SDA3	8	10G_PHY_MDIO_SDA1
9	GND	10	GND

In addition, the MDIO/I2C signals from COM Express™ module are available on a dual row 10 pin, P2.54mm standard pin header 10-pin header, type ADIMPEX p/n LE008210-R or equivalent.

One of the MDIO I2C interfaces #0 and #2 can also be switched to OCP connector's pins #49 and #50. Switching is controlled via Jumper JP11.

Four on-board yellow LEDs D53-D56 notify that maximum link speed of the corresponding 10Gb Ethernet ports has been reached (D53 for PHI #0 and so on).

Signals Description:

10G_PHY_MDIO_SDA[0:3]: Management Data I/O Interface mode (MDIO mode) or I2C (I2C mode) data signal for serial data transfers between the MAC and an external PHY

10G_PHY_MDC_SCL[0:3]: Management Data I/O Interface mode (MDIO mode) or I2C (I2C mode) clock signal for serial data transfers between the MAC and an external PHY

The MC79 carrier board offers four Software Definable Pin (SDP) interfaces, supporting both input and output operation, according to COM Express Rel. 3.0 specifications. The SDP can be used to provide a timing communication path between the Module and Carrier.

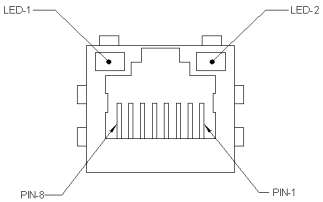
A board level signal that communicates time is a key element that facilitates clock synchronization between elements of a platform.

These interfaces are available on as many SMA RF connectors CN53 (10G_SDP0), CN54 (10G_SDP2), CN55 (10G_SDP1), CN56 (10G_SDP3) , type Amphenol p/n 132134.

RJ45 Gigabit Ethernet Connector- CN23			
Pin	Signal	Pin	Signal
1	GBE0_MDI0+	5	GBE0_MDI2-
2	GBE0_MDI0-	6	GBE0_MDI1-
3	GBE0_MDI1+	7	GBE0_MDI3+
4	GBE0_MDI2+	8	GBE0_MDI3-

COM Express Type 7 modules offer a Gigabit Ethernet interface, including GbE MAC and PHY. Only the isolation magnetic (with a 1:1 turn ratio) is required.

On the carrier board, therefore, there is a GbE RJ-45 connector CN23 with integrated magnetic, also including Activity and Link LEDs, type TRXCOM P/N TRJG16414A4NL or equivalent.



On this connector there are also two bicolour Green/Yellow LEDs: LED1 (Left LED) shows 10/100 or 1000 connection: green means 100Mbps connection, yellow means 1000Mpbs connection, when the LED is Off then 10Mpbs or no connection is available. LED2 (Right LED) shows ACTIVITY presence.

This interface is compatible both with Gigabit Ethernet (1000Mbps) and with Fast Ethernet (10/100Mbps) Networks. It will configure automatically to work with the existing network.

Please be aware that it will work in Gigabit mode only in case that it is connected to Gigabit Ethernet switches/hubs/routers. For the connection, cables category Cat5e or better are required. Cables category Cat6 are recommended for noise reduction and EMC compatibility issues, especially when the length of the cable is significant.

Signals Description:

GBE0_MDI0+/GBE0_MDI0-: Ethernet Controller #0 Media Dependent Interface (MDI) I/O differential pair #0. It is the first differential pair in Gigabit Ethernet mode, and the Transmit differential pair in 10/100 Mbps modes.

GBE0_MDI1+/GBE0_MDI1-: Ethernet Controller #0 Media Dependent Interface (MDI) I/O differential pair #1. It is the second differential pair in Gigabit Ethernet mode, and the Receive differential pair in 10/100 Mbps modes.

GBE0_MDI2+/GBE0_MDI2-: Ethernet Controller #0 Media Dependent Interface (MDI) I/O differential pair #2. It is the third differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

GBE0_MDI3+/GBE0_MDI3-: Ethernet Controller #0 Media Dependent Interface (MDI) I/O differential pair #3. It is the fourth differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

3.3.20 Buttons

On the carrier board, there are four momentary pushbuttons (with contacts normally open) for the direct handling of COM Express™ power management signals.

The first pushbutton, M1, is placed on SYS_RESET# signal. Upon the pressure of this pushbutton, the COM Express™ module will perform a reset.

The second pushbutton, M2, is placed on POWER_BTN# signal. Upon the pressure of this pushbutton, the COM Express™ module will perform a power up / power down sequence.

The third pushbutton, M3, is placed on LID # signal. Such a signal can be used by the COM Express™ module to detect the opening / the closure of an external lid switch, like those used to detect opening / closure of the notebooks. Upon changes in LID # state, the OS could trigger the transition of the module from Working to Sleep status, or vice versa.

The fourth pushbutton, M4, is placed on SLEEP# signal. Upon the pressure of this pushbutton, the COM Express™ module will enter in a sleep state (if such states are supported by the module).

Chapter 4.
Appendices

- Thermal Design
- Accessories

4.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like COM Express™ modules, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

COM Express™ specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the COM Express™ module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsinks in some situation can represent a cooling solution. Until the modules are used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with fan could be sufficient for modules' cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat.

Indeed, when using CCOMe-C79 carrier board with any COM Express™ module, it is necessary to consider carefully the global heat generated by the system, and the scenario of utilisation.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide COM Express™ modules' specific heatspreaders and heatsinks (active and passive), but please remember that their use must be evaluated accurately inside the final system (electronics + mechanics), and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions, which also keeps the surface temperature of all carrier board's components in the temperature range specified for the specific carrier board configuration (commercial grade).

4.2 Accessories

The CCOMe-C79 Carrier Board will not be sold alone, but as a part of a more comprehensive Development kit, like those already available for Qseven Carrier boards and also for COM Express M965 Carrier board.

The full development kit is coded as COM EXP T7 DEV KIT and does contain:

- Carrier board for COM Express® Type 7 compliant modules CCOMe-C79
- 1 x DB-9 Serial cable adapter
- Front Panel Board with connecting cable (CV-837/30 and CV-836/30)
- SATA 7p Data cable

A more detailed description can be found at related product page in Seco S.p.A website: COM EXP T7 DEV KIT (seco.com)