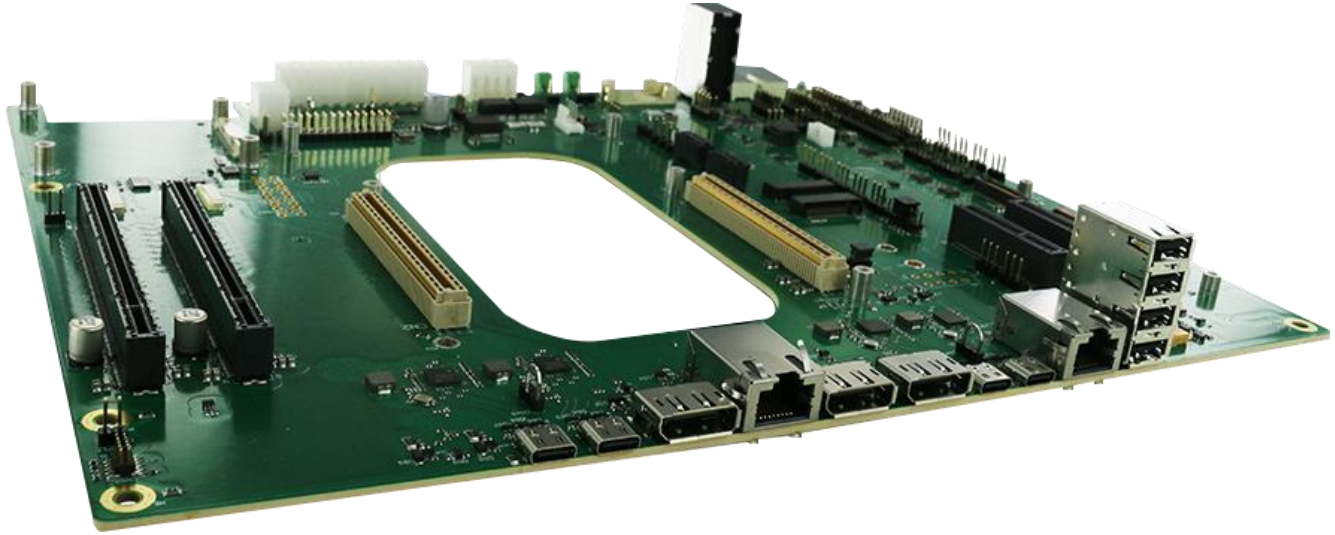
COM-HPC®

User Manual

PICMG COM-HPC™

CCHPC-C78-C



Carrier Board for COM-HPC™ compliant client modules

SECO

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	6th February 2023	First Official Release	SO
1.1	2nd March 2023	Included Engineering Samples Policy	SO

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

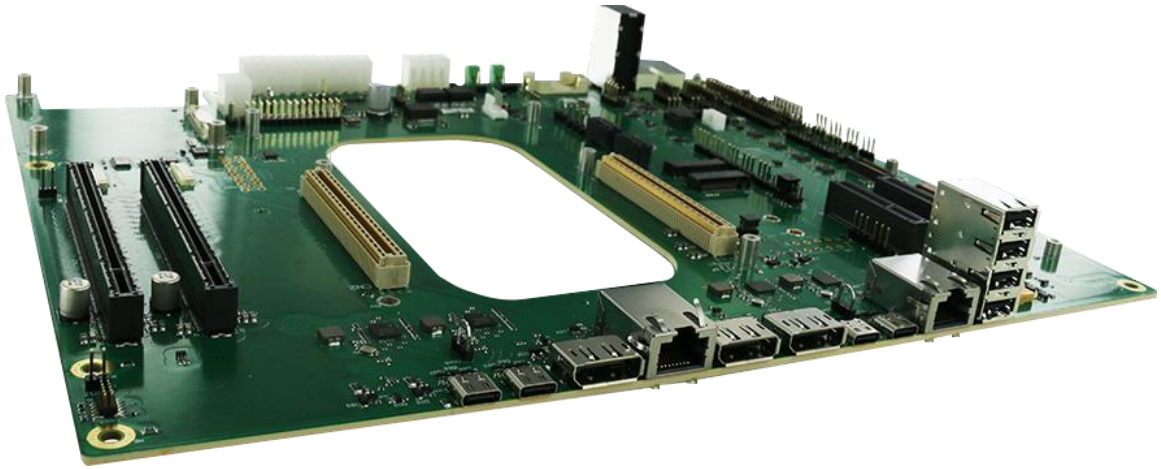
For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at www.seco.com (registration required).

Our team is ready to assist.

INDEX

Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Safety Policy
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific ticketing procedure https://support.seco.com/ (web RMA). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

SECO offers Engineering Samples for early evaluation and development. Engineering Samples are sold "as-is" with no warranty of any kind, neither explicit nor implied.

Here https://www.seco.com/it/EngineeringSamplesPolicy is defined the framework of SECO and customer responsibilities regarding Engineering Samples.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipments and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210
- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The board uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The board, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

Whenever handling this product, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The board is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Policy

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, this product shall be:

- installed inside a fire enclosure made of non-combustible material or V-1 material;
- installed inside an enclosure compliant with all applicable IEC 62368-1 requirements;
- Use an ATX standard power supply unit compliant with the reference safety standard for the product;

The manufacturer which includes this product in his end-user product shall respect the previous and following points:

- Install the board inside an enclosure provided with the symbol IEC 60417-5041 (element 1a according to clause 9.5.2 of the IEC 62368-1) on the external part and that must be placed also on end-user product's User Manual;
- Verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition;
- Prescribe temperature and humidity range for operating, transport and storage conditions;
- Prescribe to perform maintenance on the board only when it is off and has already cooled down;
- Prescribe the use of the board with a power source classified ES1 according to the requirements of IEC EN 62368-1;
- The board in its enclosure must be evaluated for temperature and airflow considerations;
- Install in a way that prevents the access to the board from children;
- Use along with CPU heatspreader/heatsinks designed according to the thermal and mechanical characteristics;

1.8 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
GbE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
JTAG	Joint Test Action Group, common name of IEEE1149.1 standard for testing printed circuit boards and integrated circuits through the Debug port
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
N.A.	Not Applicable
N.C.	Not Connected
OS	Operating System
PCI-e	Peripheral Component Interface Express
PWM	Pulse Width Modulation
PWR	Power
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows use the use of the same SD interface to drive different Input/Output

	devices, like cameras, GPS, Tuners and so on
SIM	Subscriber Identity Module, a card which stores all data of the owner necessary to allow him accessing to mobile communication networks
SM Bus	System Management Bus, a subset of the I2C bus protocol dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UIM	User Identity Module, an extension of SIM modules.
USB	Universal Serial Bus
V_REF	Voltage reference Pin

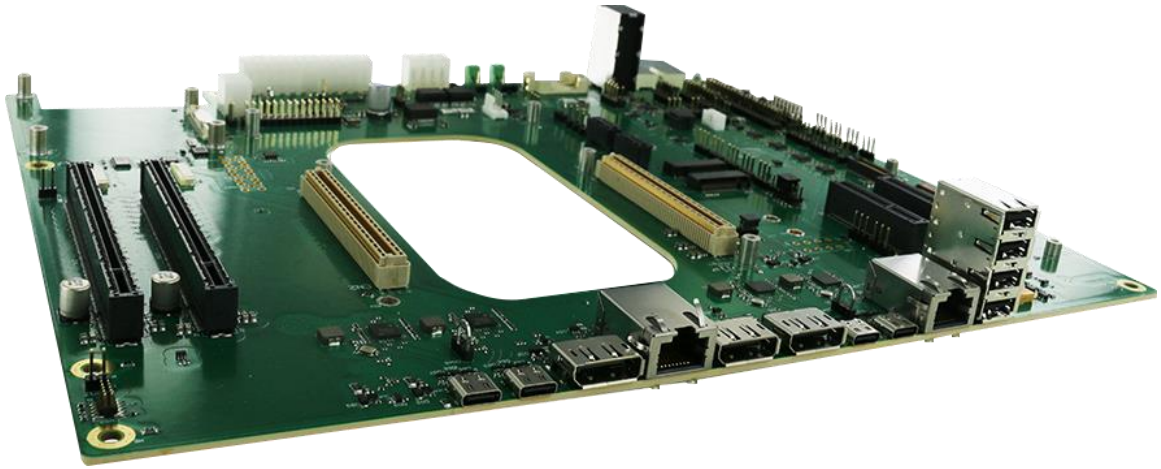
1.9 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
Com HPC	https://www.picmg.org/openstandards/com-hpc/
Com HPC Carrier Design Guide	PICMG® COM-HPC® Carrier Design Guide
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	https://cache.nxp.com/documents/user_manual/UM10204.pdf?fsrch=1&sr=2&pageNum=1
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SM Bus	http://www.smbus.org/specs
UEFI	http://www.uefi.org
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip
xHCI	http://www.intel.com/content/www/us/en/io/universal-serial-bus/extensible-host-controler-interface-usb-xhci.html?wapkw=xhci

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram



2.1 Introduction

CCHPC-C78-C (abbreviated HC78) is a carrier board, designed in ATX form factor, intended for the use with COM-HPC™ Client modules.

COM-HPC™ is an open industry standard defined specifically for COMs (computer on modules). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today.

COM HPC™ CPU modules integrate all the core components of a typical PC-like architecture, and make all interface available through two standardized connectors, so that COM HPC™ modules become scalable. This means that once an application has been created, there is the ability to diversify the product range through the use of different performance class or form factor size modules.

Baseboard designers can use just the I/O interfaces that really need, providing, on the carrier board, the routing to the adequate interface connectors.

This versatility allows the designer to create a dense and optimised package, which results in a more reliable product while simplifying system integration.

HC78 board can be used both as an evaluation module, to test the functionality of your COM-HPC™ module and design an application specific carrier board for it, or as a complete carrier board, already suited for standard purposes, with a small space consumption.

In any case, the solutions so realised is fully scalable, and allows to the user to keep his own-designed system continuously up-to-date, since the system can be updated simply replacing the COM-HPC™ module with a newer one, just unplugging the module and replacing it, without the need of redesigning it.

The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

2.2 Technical Specifications

Supported Modules
- COM HPC™ Client compliant modules

Mass Storage interfaces
- 2x SATA 7p M connectors
- 2x M.2 Socket 3 Key M 2088 NVME PCIe x4 slots

Networking
- 2x RJ-45 connector NBASET
- 2x 10Gbase-KR interfaces on OCP connector

USB
- 4 x USB 2.0 Host ports on Type-A sockets
- 4 x USB 3.2 Host ports on Type-C sockets

PCI-e
- 2x PCI-e x4 Slots
- 1x PCI-e x16 Slot, PCIe graphics (PEG) capable
- 1x PCI-socke x16 Slot
- 2x M.2 Socket 3 Key M 2088 NVME PCIe x4 slots

Serial Ports
- 2 x RS-232 ports on dedicated pin header (from module)

Other Interfaces
- BMC connector with SM Bus, I2C, LPC, 1x USB 2.0, 1x PCI-e x1, NCSI signals
- 4 x GPI + 4 x GPO pin header (interface multiplexed with µSD slot)
- SPI Flash Socket
- Button / LEDs front panel header
- 4-pin tachometric FAN connector
- I2C + SM Bus on feature Pin header
- I2C Flash Socket
- SM Bus Smart Battery Connector
- 4 x 7-segment LCD displays for POST codes
- eSPI internal header
- USB Overcurrent header
- JTAG connector
- FuSa header
- SPI Flash header
- Buzzer

Power supply: ATX 24 poles connector for carrier board working only
Auxiliary 12V connector for carrier board working only
12 V_{DC} power in connector for COM Express™ module's working
Coin-cell holder for RTC

Operating temperature: 0°C ÷ +60°C * (Commercial version)

Dimensions: 305x244mm (ATXform factor, 12" x 9.6")

! ** Temperature ranges indicated mean that all components available onboard are certified for working with a Tcase included in these temperature ranges. This means that it is customer's responsibility to ensure that all components' Tcases remain in the range above indicated. Please also check paragraph 4.1.*

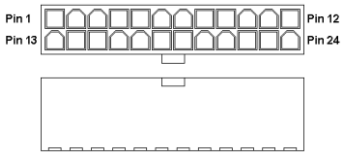
2.3 Electrical Specifications

The board needs to be supplied using a standard ATX Power Supply, which can, however, also be configured to work in AT mode.

ATX/ AT Power Connector – CN10

Pin	Signal	Pin	Signal
1	+3.3V_RUN	13	+3.3V_RUN
2	+3.3V_RUN	14	---
3	GND	15	GND
4	+5V_RUN	16	PS_ON# (*)
5	GND	17	GND
6	+5V_RUN	18	GND
7	GND	19	GND
8	PWR_OK_ATX	20	---
9	+5V_SB	21	+5V_RUN
10	+12V_RUN	22	+5V_RUN
11	+12V_RUN	23	+5V_RUN
12	+3.3V_RUN	24	GND

Power Connector CN10 is type Molex Mini-Fit Jr. connector, p/n 39-28-1243, or equivalent, with the pin-out indicated in the table here on the left (it is the standard 24-pin ATX pin-out).



Mating Connector, MOLEX p/n 39-01-2240 or equivalent, with female crimp terminal MOLEX series 5566.

PS_ON#: this signal is present only if the board is configured, via JP33 and JP34, to work in ATX mode. If working in AT mode, this pin is connected directly to Ground.

Power connector can be set to work in ATX mode or AT mode by using dedicated jumpers JP33 and JP34, which are a standard pin headers, P2.54mm, 1x3 pin.

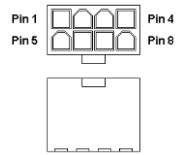
JP33 position	JP34 position	Power mode
2-3	Don't Care	AT mode
1-2	1-2	ATX mode
1-2	2-3	ATX – No Suspend status

EPS CPU Power Connector – CN8

Pin	Signal	Pin	Signal
1	GND	5	+12V_RUN
2	GND	6	+12V_RUN
3	GND	7	+12V_RUN
4	GND	8	+12V_RUN

The board has a CPU Power Connector CN8 providing +12V_RUN for the installed module only.

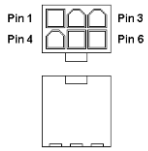
CN8 is a Molex Mini-Fit jr. 8 poles connector, p/n 39-28-1083 or equivalent.



Mating Connector, MOLEX p/n 39-01-2080 or equivalent, with female crimp terminal MOLEX series 5566.

12V PCI-e 6-pin Power Connector – CN7			
Pin	Signal	Pin	Signal
1	+12V_RUN	5	GND
2	+12V_RUN	6	GND
3	+12V_RUN	7	GND

The board has an Auxiliary Power connector CN7 providing +12V_RUN for the carrier board section only, useful when multiple PCI-e modules are connected.



CN7 is 6-poles connector, type MOLEX mini-Fit Jr. p/n 39-28-1063 or equivalent.

Mating Connector, MOLEX p/n 39-01-2060 or equivalent, with female crimp terminal MOLEX series 5566.

The use of wires with section 18 AWG is recommended, in order to ensure the proper amperage of the power section.

JP31 position	+5V_ALW enabled by
Not inserted	COM HPC Client module presence
Inserted	Always enabled

+5V_ALW power rail is generated starting from +5V_SB coming from ATX power connector. In normal condition, it is automatically generated when a COM HPC Client module is plugged in COM HPC connectors CN1 and CN2. However, it is possible to force its generation independently by the presence of a client module. For this purpose. On-board it is available the 2 way jumper JP31

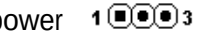
JP2 position	+5V_SB Current monitor selector
Not inserted	Current measurement enabled
Inserted	Current measurement disabled

The power consumption on +5V_SB can be monitored by removing 2 way jumper JP2 and inserting a tester set as ammeter.

Alternatively, the consumption on +5V_SB can be monitored by inserting a tester set as ammeter between pin 1 and 2 of +5V_SB Sense Connector CN4.

JP32 position	Power Ok management
1-2	PSU PWR_OK enabled
2-3	PWR_OK always high

The COM HPC® card edge connector has a PWR_OK signal from main power supplied by Carrier Board to the module, indicating that all the power supplies to the Module are stable within specified ranges. The Module will typically not power up until the PWR_OK signal goes active.

JP32 is a standard pin header, P2.54mm, 1x3 pin, dedicated to manage this power 

status signal for the Module. For normal operation, set the jumper in 1-2 position, otherwise set in 2-3 position to fix its level high and have it always activated.

Diode LED D17 is present on Carrier Board to notify the system has been correctly powered-up.

Another diode LED D16, complementary to D17, is used to notify the Reset Output from Module to Carrier Board.

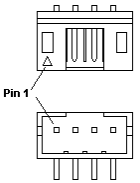
JP35 position	Module power type
1-2	Client Module - Wide Range 8V to 20V input
2-3	Client Module – Fixed 12V Input
Not inserted	Carrier board 12V Fixed

A dedicated 3-way jumper, JP35, has to be configured according to the allowed Voltage range of the COM HPC Client module-

2.3.1 Smart Battery SM Bus Connector

Smart Battery SM Bus Connector – CN29			
Pin	**Signal**	**Pin**	**Signal**
1	SMB_CLK	3	SMB_ALERT#
2	SMB_DAT	4	GND

The SM bus coming from the installed module is carried directly both to the Feature header (see par.Errore. L'origine riferimento non è stata trovata.) and to a JST 4-pin connector CN29, p/n B4B-PH-K-S(LF)(SN), or equivalent, which can be used for the connection of external Smart battery controllers. Pinout as indicated in the left table.



SB_SMB_CLK: Smart Battery System Management bus bidirectional clock line, +3.3V_ALW electrical level with 10kΩ pull up resistor derived by SMB_CK signal

SB_SMB_DAT: Smart Battery System Management bus bidirectional data line, +3.3V_ALW electrical level with 10kΩ pull up resistor derived by SMB_DAT signal

SMB_ALERT#: System Management Bus Alert, active low input to the module that can be used to generate an Interrupt or to wake the system

2.3.2 Coin cell battery holder

For the occurrences when the System (Carrier board + installed module) is not powered with an external power supply, on board there is a RTC Coin Cell Battery holder CN9, for the use of standard coin battery type CR2032 with a nominal capacity of 220mAh, to supply, with a 3V voltage, the Real Time Clock and CMOS memory mounted on the COM Express™ module.

The batteries should only be replaced with devices of the same type. Always check the orientation before inserting and make sure that they are aligned correctly and are not damaged or leaking.

! CAUTION: handling batteries incorrectly or replacing with not-approved devices may present a risk of fire or explosion.

Never allow the batteries to become short-circuited during handling. Batteries supplied with this product are compliant to requirements of European Directive 2006/66/EC regarding batteries and accumulators. When putting out of order this product, remove the batteries from the board in order to collect and dispose them according to the requirement of the same European Directive above mentioned. Even when replacing the batteries, the disposal has to be made according to these requirements.

JP36 position	RTC Battery enable
1-2	Battery disconnected
2-3	Battery connected
NO jumper	Current measurement

RTC battery can be enabled/disabled using dedicated jumper on JP36, which is a standard pin header, P2.54mm, 1x3 pin.

It is possible to monitor the consumption on VCC_RTC battery by removing the jumper from JP36 connector and connecting an Ampere meter to the pins 2-3.

Alternatively, the consumption on VCC_RTC can be monitored by connecting an Ampere meter between pin 1 and 2 of RTC Battery Sense Connector CN5.

CN5 is a dedicated 2 position Wire to Board Terminal Block, type Wurth p/n 691210910002

JP15 position	Battery Low Indicator enable
Not inserted	Indicator disabled
Inserted	Indicator enabled

The RTC battery voltage level is monitored through a comparator inside the board. Battery low status signal (BATLOW#) is carried to COM-HPC™ module to be managed.

JP15 is a 2-way jumper to enable/disable this indicator.

2.3.3 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

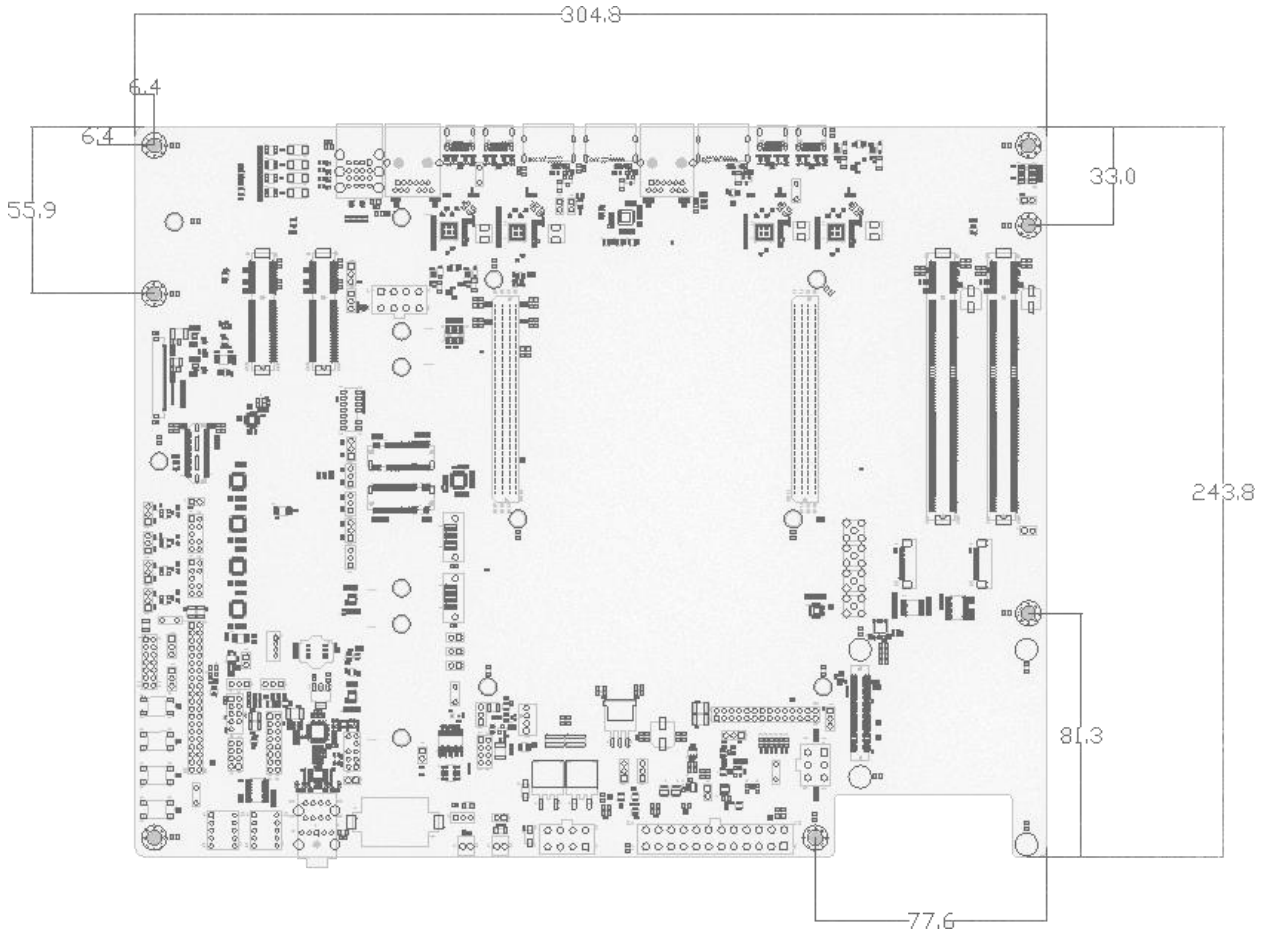
_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

2.4 Mechanical Specifications

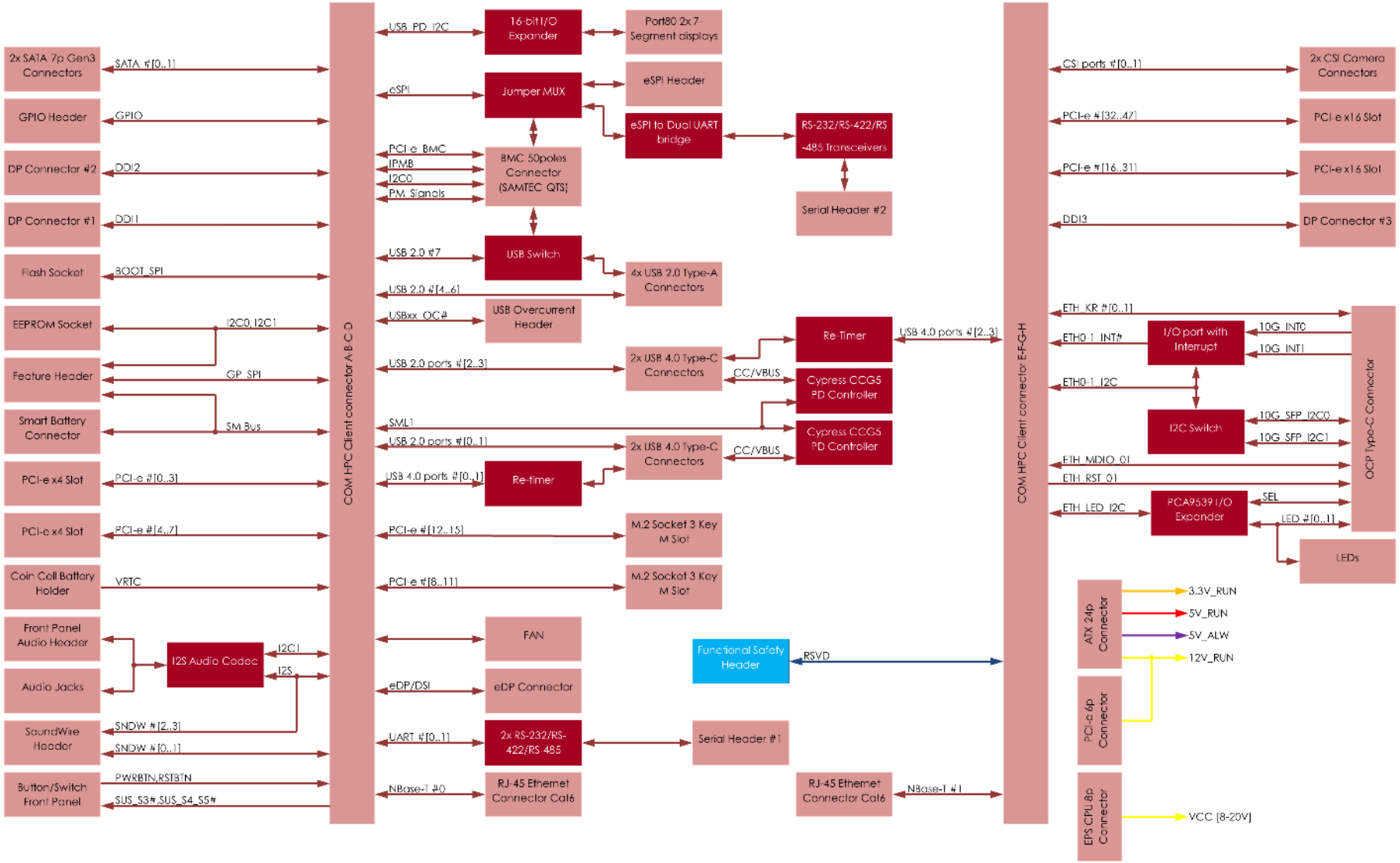
According to ATX form factor, board dimensions are nominal 305 x 244 mm (12” x 9.6”).

The printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

In order to fix the COM HPC™ module to the carrier board, on HC78 have been soldered four metallic spacers, height 8mm, 2.5mm diameter.

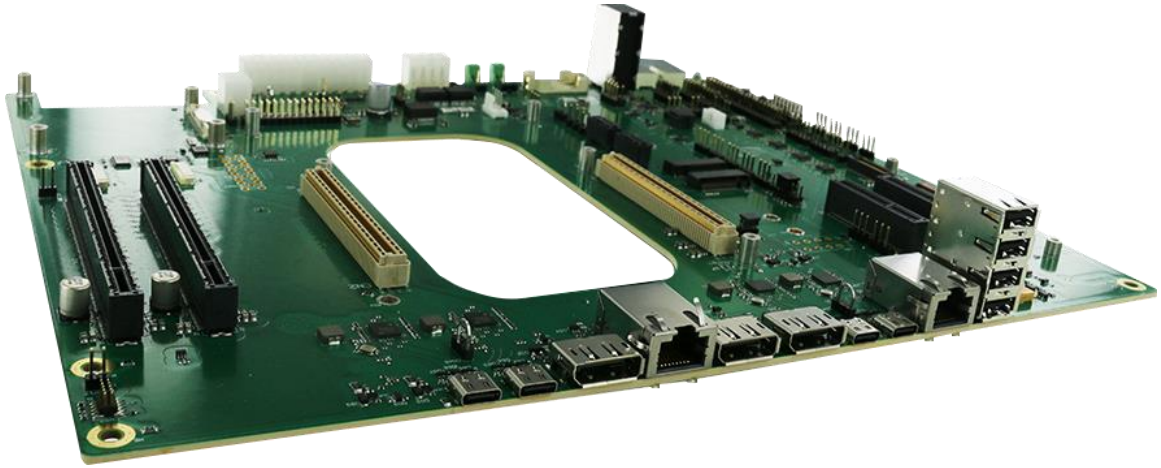


2.5 Block Diagram



Chapter 3.
CONNECTORS

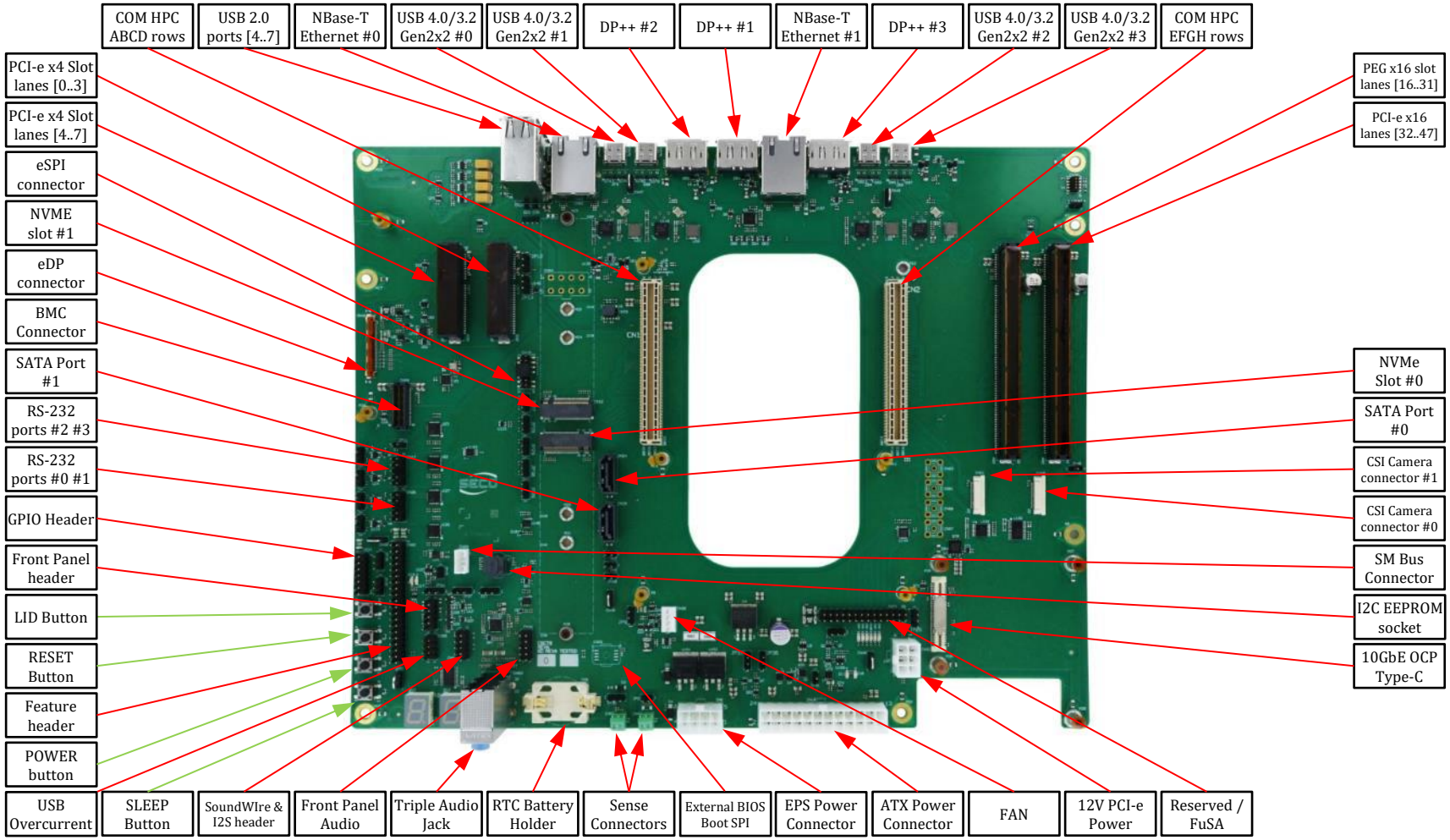
- Connectors placement
- Connectors overview
- Connectors description



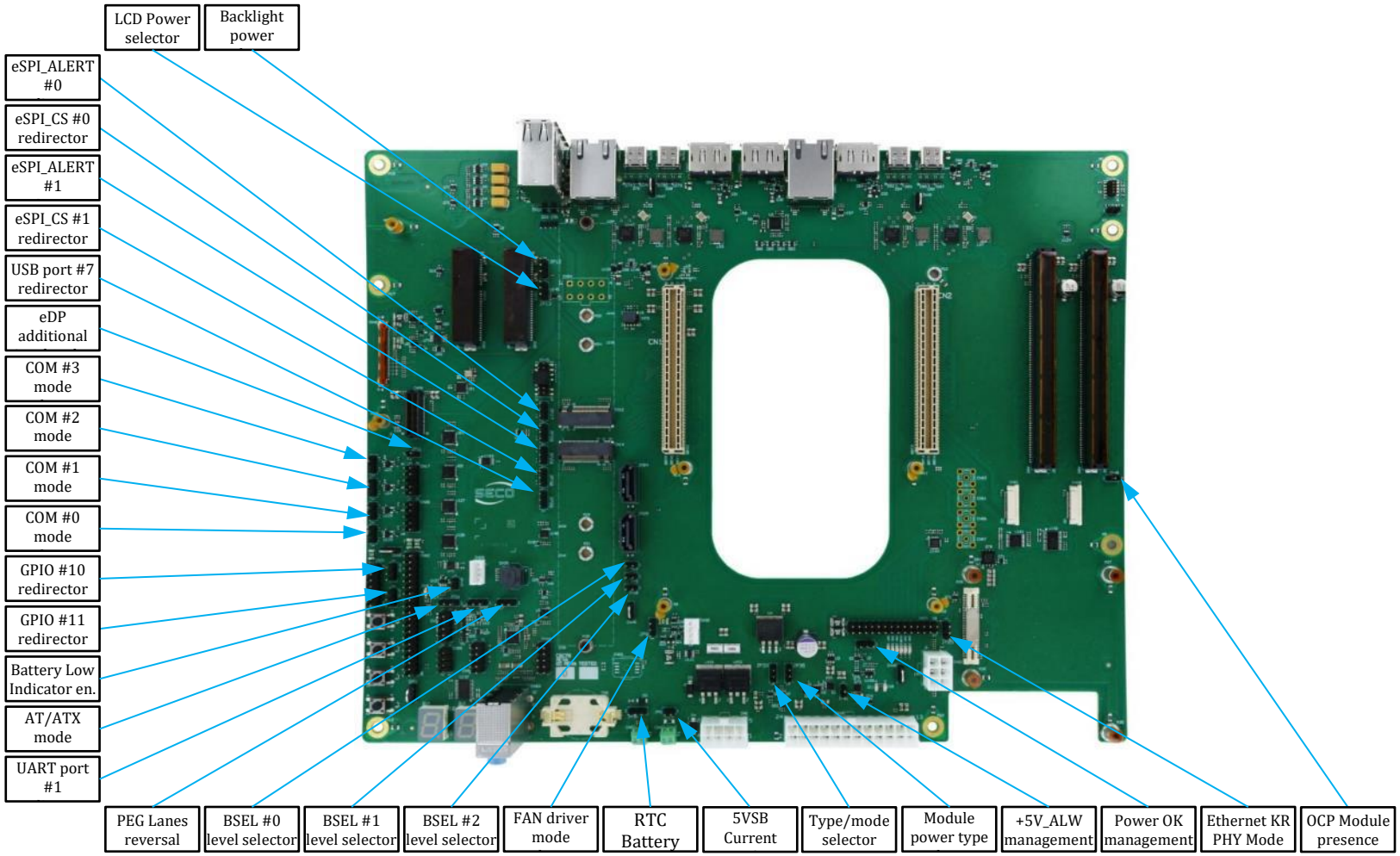
3.1 Connectors placement

On this product, there are several connectors. Some of them are standard connectors, like Gigabit Ethernet, USB ports, and are placed on the same side of the board, so that they can be placed on a panel of a possible enclosure.

In the following picture it is possible to see the position of each connector.



JUMPER POSITION



3.2 Connectors overview

3.2.1 Connectors list

Name	Description	Name	Description
CN1	Com HPC, A-B-C-D rows connector	CN42	eDP connector
CN2	Com HPC, E-F-G-H rows connector	CN52	DP++ Connector #1
CN4	+5V_SB Sense Connector	CN53	DP++ Connector #2
CN5	RTC Battery Sense connector	CN54	DP++ Connector #3
CN7	12V PCI-e 6-pin Power Connector	CN55	USB Overcurrent header
CN8	EPS CPU Power Connector	CN58	BMC Connector
CN9	Coin Cell RTC Battery Holder	CN60	CSI CAMERA CONNECTOR #0
CN10	Power ATX connector	CN61	CSI CAMERA CONNECTOR #1
CN12	M.2 Socket 3 Key M NVMe slot #1 (lanes #[8..11])	CN62	Feature pin Header
CN13	PCI-e Graphics (PEG) x16 slot (lanes #[16..31])	CN63	triple audio jack
CN14	M.2 Socket 3 Key M NVMe slot #2 (lanes #[12..15])	CN64	SoundWire and I2S header
CN15	eSPI Connector	CN65	RJ45 NBase-T Ethernet #1 Connector
CN17	RS-232 ports #2 #3 Internal pin Header	CN68	RJ45 NBase-T Ethernet #0 Connector
CN20	USB 2.0 ports #4 #5 #6 #7 Quad Type-A socket	CN71	Reserved / FuSa Header
CN24	SATA M 7-p #0 Connector	CN72	PCI-e x16 slot (lanes #[32..47])
CN25	SATA M 7-p #1 Connector	CN73	PCI-e x4 slot (lanes #[0..3])
CN26	RS-232 ports #0 #1 Internal pin Header	CN74	PCI-e x4 slot (lanes #[4..7])
CN28	External BIOS Boot SPI Header	CN75	USB 4,0 / 3.2 Gen2x2 port #0 Type-C socket
CN29	Smart Battery SM Bus Connector	CN76	USB 4.0 / 3.2 Gen2x2 port #1 Type-C socket
CN31	GPIO pin header	CN77	USB 4,0 / 3.2 Gen2x2 port #2 Type-C socket
CN32	FAN Connector	CN78	USB 4.0 / 3.2 Gen2x2 port #3 Type-C socket
CN34	Front Panel Header	CN79	USB ports #0 #1 PD Controller programming (reserved)
CN35	I2C EEPROM socket	CN80	USB ports #2 #3 PD Controller programming (reserved)
CN38	Front Panel Audio Header	CN82	10GbE OCP Type-C Connector

3.2.2 Jumpers and switch list

Name	Description	Name	Description
JP2	+5V_SB Current monitor selector	JP26	USB port #7 redirector
JP5	COM #2 mode selector	JP27	eSPI_ALERT #0 redirector
JP6	COM #3 mode selector	JP28	eSPI_CS #0 redirector
JP7	BSEL #0 level selector	JP29	eSPI_ALERT #1 redirector
JP8	BSEL #1 level selector	JP30	eSPI_CS #1 redirector
JP9	FAN driver mode selector	JP31	+5V_ALW management
JP11	eDP additional signals selector	JP32	Power OK management
JP12	Backlight power selector	JP33	Type/mode selector
JP13	LCD Power selector	JP34	AT/ATX mode selector
JP15	Battery Low Indicator enable	JP35	Module power type selector
JP17	PEG_LANE reversal	JP36	RTC Battery enable
JP18	COM #0 mode selector	JP37	UART port #1 redirector
JP19	COM #1 mode selector	JP38	GPIO #10 redirector
JP20	BSEL #2 level selector	JP39	GPIO #11 redirector
JP25	Ethernet KR PHY Mode	JP40	OCP Module presence

3.3 Connectors description

3.3.1 COM Express™ module connectors

For the connection of COM HPC® Client CPU modules, on board there are two double connectors, type SAMTEC ASP-209948-01 (400 pin, ultra thin, 0.635mm pitch, h=10mm), as requested by COM HPC® specifications.

In the following table, signals related to DDI Port #2 are factory alternative to USB 3.2 Gen2 2x2 Port#2, and signals related to DDI Port #1 are factory alternative to USB 3.2 Gen2 2x2 Port#3.

COM HPC® Connector CN1 – Rows A & B					
Row A			Row B		
Description	Pin name	Pin	Pin	Pin name	Description
VIN Power supply	VCC	A1	B1	VCC	VIN Power supply
VIN Power supply	VCC	A2	B2	PWRBTN#	Power Button Input
VIN Power supply	VCC	A3	B3	VCC	VIN Power supply
VIN Power supply	VCC	A4	B4	THERMTRIP#	Thermal Trip Output
VIN Power supply	VCC	A5	B5	VCC	VIN Power supply
VIN Power supply	VCC	A6	B6	TAMPER#	Intruder Detect Input
VIN Power supply	VCC	A7	B7	VCC	VIN Power supply
VIN Power supply	VCC	A8	B8	SUS_S3#	Suspend to RAM (S3) indicator output
VIN Power supply	VCC	A9	B9	VCC	VIN Power supply
Power Ground	GND	A10	B10	WD_STROBE#	Watchdog Strobe Input
Battery Low Input	BATLOW#	A11	B11	WD_OUT	Watchdog Event indicator Output
Platform Reset Output	PLTRST#	A12	B12	GND	Power Ground
Power Ground	GND	A13	B13	USB5-	USB 2.0 Data Port #5-
USB 2.0 Data Port #7-	USB7-	A14	B14	USB5+	USB 2.0 Data Port #5+
USB 2.0 Data Port #7+	USB7+	A15	B15	GND	Power Ground
Power Ground	GND	A16	B16	USB4-	USB 2.0 Data Port #4-
USB 2.0 Data Port #6-	USB6-	A17	B17	USB4+	USB 2.0 Data Port #4+
USB 2.0 Data Port #6+	USB6+	A18	B18	GND	Power Ground
Power Ground	GND	A19	B19	I2S_LRCLK	I2S L/R Clock
DDI Port #1 TMDS I2C Data or DP Aux-	DDI1_SDA_AUX-	A20	B20	I2S_DOUT	I2S Data Out
DDI Port #1 TMDS I2C Clock or DP Aux+	DDI1_SCL_AUX+	A21	B21	I2S_MCLK	I2S Master Clock
Power Ground	GND	A22	B22	I2S_DIN	I2S Data In
DDI Port #1 Differential pair 0-	DDI1_PAIR0-	A23	B23	I2S_CLK	I/O Data line for General Purpose I2C #0
DDI Port #1 Differential pair 0+	DDI1_PAIR0+	A24	B24	VCC_5V_SBY	Standby Power Input
Power Ground	GND	A25	B25	USB67_OC#	USB Over Current Ports 6/7
DDI Port #1 Differential pair 1-	DDI1_PAIR1-	A26	B26	USB45_OC#	USB Over Current Ports 4/5

DDI Port #1 Differential pair 1+	DDI1_PAIR1+	A27	B27	USB23_OC#	USB Over Current Ports 2/3
Power Ground	GND	A28	B28	USB01_OC#	USB Over Current Ports 0/1
DDI Port #1 Differential pair 2-	DDI1_PAIR2-	A29	B29	SML1_CLK	Carrier board PD Controller I2C Clock
DDI Port #1 Differential pair 2+	DDI1_PAIR2+	A30	B30	SML1_DAT	Carrier board PD Controller I2C Data
Power Ground	GND	A31	B31	PMCALERT#	USB PD Controller Alert Input
DDI Port #1 Differential pair 3-	DDI1_PAIR3-	A32	B32	SML0_CLK	Carrier board USB4 Re-Timer I2C Clock
DDI Port #1 Differential pair 3+	DDI1_PAIR3+	A33	B33	SML0_DAT	Carrier board USB4 Re-Timer I2C Data
Power Ground	GND	A34	B34	USB_PD_ALERT#	Carrier board PD Controller Alert#
eDP Channel Aux-	eDP_AUX-	A35	B35	USB_PD_I2C_CLK	EC Master to USB PD Controller (Slave) Dedicated I2C Clock Line
eDP Channel Aux+	eDP_AUX+	A36	B36	USB_PD_I2C_DAT	EC Master to USB PD Controller (Slave) Dedicated I2C Data Line
Power Ground	GND	A37	B37	USB_RT_ENA	USB Re-Timers Power Enable Output
eDP Channel Data 0-	eDP_TX0-	A38	B38	USB1_LSRX	USB4 Port #1 Alternate Modes Sideband RX interface
eDP Channel Data 0+	eDP_TX0+	A39	B39	USB1_LSTX	USB4 Port #1 Alternate Modes Sideband TX interface
Power Ground	GND	A40	B40	USB0_LSRX	USB4 Port #0 Alternate Modes Sideband RX interface
eDP Channel Data 1-	eDP_TX1-	A41	B41	USB0_LSTX	USB4 Port #0 Alternate Modes Sideband TX interface
eDP Channel Data 1+	eDP_TX1+	A42	B42	GND	Power Ground
Power Ground	GND	A43	B43	USB0_AUX-	DisplayPort Alternate Mode Port #0 Aux-
eDP Channel Data 2-	eDP_TX2-	A44	B44	USB0_AUX+	DisplayPort Alternate Mode Port #0 Aux+
eDP Channel Data 2+	eDP_TX2+	A45	B45	LID#	LID Switch Input
Power Ground	GND	A46	B46	SLEEP#	Sleep Button Input
eDP Channel Data 3-	eDP_TX3-	A47	B47	VCC_BOOT_SPI	+3.3V_Always Power Supply for Carrier board SPI
eDP Channel Data 3+	eDP_TX3+	A48	B48	BOOT_SPI_CS#	Chip select for Carrier Board SPI
Power Ground	GND	A49	B49	BSEL0	Boot Select Input Pin #0
eSPI Master Data Input / Output #0	eSPI_IO0	A50	B50	BSEL1	Boot Select Input Pin #1
eSPI Master Data Input / Output #1	eSPI_IO1	A51	B51	BSEL2	Boot Select Input Pin #2
eSPI Master Data Input / Output #2	eSPI_IO2	A52	B52	eSPI_ALERT0#	eSPI service request from the Slave #0
eSPI Master Data Input / Output #3	eSPI_IO3	A53	B53	eSPI_ALERT1#	eSPI service request from the Slave #1
eSPI Master Clock Output	eSPI_CLK	A54	B54	eSPI_CS0#	eSPI Chip Select Slave #0
Power Ground	GND	A55	B55	eSPI_CS1#	eSPI Chip Select Slave #1
PCI-e Clock request #1	PCIe_CLKREQ0_LO#	A56	B56	eSPI_RST#	eSPI Reset Output
PCI-e Clock request #0	PCIe_CLKREQ0_HI#	A57	B57	GND	Power Ground
Power Ground	GND	A58	B58	PCIe_BMC_RX-	Board Management Controller PCIe
Board Management Controller PCIe	PCIe_BMC_TX-	A59	B59	PCIe_BMC_RX+	Board Management Controller PCIe
Board Management Controller PCIe	PCIe_BMC_TX+	A60	B60	GND	Power Ground
Power Ground	GND	A61	B61	PCIe08_RX-	PCI-e x4 Gen4 Lane 8 Receive -
PCI-e x4 Gen4 Lane 8 Transmit -	PCIe08_TX-	A62	B62	PCIe08_RX+	PCI-e x4 Gen4 Lane 8 Receive +
PCI-e x4 Gen4 Lane 8 Transmit +	PCIe08_TX+	A63	B63	GND	Power Ground
Power Ground	GND	A64	B64	PCIe09_RX-	PCI-e x4 Gen4 Lane 9 Receive -
PCI-e x4 Gen4 Lane 9 Transmit -	PCIe09_TX-	A65	B65	PCIe09_RX+	PCI-e x4 Gen4 Lane 9 Receive +

PCI-e x4 Gen4 Lane 9 Transmit +	PCIe09_TX+	A66	B66	GND	Power Ground
Power Ground	GND	A67	B67	PCIe10_RX-	PCI-e x4 Gen4 Lane 10 Receive -
PCI-e x4 Gen4 Lane 10 Transmit -	PCIe10_TX-	A68	B68	PCIe10_RX+	PCI-e x4 Gen4 Lane 10 Receive +
PCI-e x4 Gen4 Lane 10 Transmit +	PCIe10_TX+	A69	B69	GND	Power Ground
Power Ground	GND	A70	B70	PCIe11_RX-	PCI-e x4 Gen4 Lane 11 Receive -
PCI-e x4 Gen4 Lane 11 Transmit -	PCIe11_TX-	A71	B71	PCIe11_RX+	PCI-e x4 Gen4 Lane 11 Receive +
PCI-e x4 Gen4 Lane 11 Transmit +	PCIe11_TX+	A72	B72	GND	Power Ground
Power Ground	GND	A73	B73	PCIe12_RX-	PCI-e x4 Gen4 Lane 12 Receive -
PCI-e x4 Gen4 Lane 12 Transmit -	PCIe12_TX-	A74	B74	PCIe12_RX+	PCI-e x4 Gen4 Lane 12 Receive +
PCI-e x4 Gen4 Lane 12 Transmit +	PCIe12_TX+	A75	B75	GND	Power Ground
Power Ground	GND	A76	B76	PCIe13_RX-	PCI-e x4 Gen4 Lane 11 Receive -
PCI-e x4 Gen4 Lane 13 Transmit -	PCIe13_TX-	A77	B77	PCIe13_RX+	PCI-e x4 Gen4 Lane 11 Receive +
PCI-e x4 Gen4 Lane 13 Transmit +	PCIe13_TX+	A78	B78	GND	Power Ground
Power Ground	GND	A79	B79	PCIe14_RX-	PCI-e x4 Gen4 Lane 11 Receive -
PCI-e x4 Gen4 Lane 14 Transmit -	PCIe14_TX-	A80	B80	PCIe14_RX+	PCI-e x4 Gen4 Lane 11 Receive +
PCI-e x4 Gen4 Lane 14 Transmit +	PCIe14_TX+	A81	B81	GND	Power Ground
Power Ground	GND	A82	B82	PCIe15_RX-	PCI-e x4 Gen4 Lane 11 Receive -
PCI-e x4 Gen4 Lane 15 Transmit -	PCIe15_TX-	A83	B83	PCIe15_RX+	PCI-e x4 Gen4 Lane 11 Receive +
PCI-e x4 Gen4 Lane 15 Transmit +	PCIe15_TX+	A84	B84	GND	Power Ground
Power Ground	GND	A85	B85	TEST#	
RTC Power Supply	VCC_RTC	A86	B86	RSMRST_OUT#	Resume From Reset Signal
32.768kHz Clock Out for Low Power States	SUS_CLK	A87	B87	UART1_TX	Serial Port #1 Transmit
General Purpose Input/Output #00	GPIO_00	A88	B88	UART1_RX	Serial Port #1 Receive
General Purpose Input/Output #01	GPIO_01	A89	B89	UART1_RTS#	Serial Port #1 Request to Send
General Purpose Input/Output #02	GPIO_02	A90	B90	UART1_CTS#	Serial Port #1 Clear to Send
General Purpose Input/Output #03	GPIO_03	A91	B91	IPMB_CLK	Intelligent Platform Management Bus I/O Clock line
General Purpose Input/Output #04	GPIO_04	A92	B92	IPMB_DAT	Intelligent Platform Management Bus I/O Data line
General Purpose Input/Output #05	GPIO_05	A93	B93	GP_SPI_MOSI	General Purpose SPI Master Out Slave In
General Purpose Input/Output #06	GPIO_06	A94	B94	GP_SPI_MISO	General Purpose SPI Master In Slave Out
General Purpose Input/Output #07	GPIO_07	A95	B95	GP_SPI_CS0#	General Purpose SPI Chip Select Slave #0
General Purpose Input/Output #08	GPIO_08	A96	B96	GP_SPI_CS1#	General Purpose SPI Chip Select Slave #1
General Purpose Input/Output #09	GPIO_09	A97	B97	GP_SPI_CS2#	General Purpose SPI Chip Select Slave #2
General Purpose Input/Output #10	GPIO_10	A98	B98	GP_SPI_CS3#	General Purpose SPI Chip Select Slave #3
General Purpose Input/Output #11	GPIO_11	A99	B99	GP_SPI_CLK	General Purpose SPI clock output
Module Type Definition Pin #0	TYPE0	A100	B100	GP_SPI_ALERT#	General Purpose SPI Alert Input

COM HPC® Connector CN1 – Rows C & D					
Row C			Row D		
Description	Pin name	Pin	Pin	Pin name	Description
VIN Power supply	VCC	C1	D1	VCC	VIN Power supply
Reset Button Input	RSTBTN#	C2	D2	VCC	VIN Power supply
VIN Power supply	VCC	C3	D3	VCC	VIN Power supply
Carrier Over-Temperature Indication	CARRIER_HOT#	C4	D4	VCC	VIN Power supply
VIN Power supply	VCC	C5	D5	VCC	VIN Power supply
Power OK Input from Main Power Supply	VIN_PWROK	C6	D6	VCC	VIN Power supply
VIN Power supply	VCC	C7	D7	VCC	VIN Power supply
Suspend to Disk (S4) / Soft Off (S5) indicator output	SUS_S4_S5#	C8	D8	VCC	VIN Power supply
VIN Power supply	VCC	C9	D9	VCC	VIN Power supply
Power Ground	GND	C10	D10	WAKE0#	PCI Express wake up signal.
PWM output for FAN speed	FAN_PWMOUT	C11	D11	WAKE1#	General purpose wake-up signal.
FAN tachometric input	FAN_TACHIN	C12	D12	GND	Power Ground
Power Ground	GND	C13	D13	USB1-	USB 2.0 Data Port #1-
USB 2.0 Data Port #3-	USB3-	C14	D14	USB1+	USB 2.0 Data Port #1+
USB 2.0 Data Port #3+	USB3+	C15	D15	GND	Power Ground
Power Ground	GND	C16	D16	USB0-	USB 2.0 Data Port #0-
USB 2.0 Data Port #2-	USB2-	C17	D17	USB0+	USB 2.0 Data Port #0+
USB 2.0 Data Port #2+	USB2+	C18	D18	GND	Power Ground
Power Ground	GND	C19	D19	DDI0_SDA_AUX-	DDI Port #0 TMDS I2C Data or DP Aux -
Soundwire #1 clock output	SNDW_DMIC_CLK1	C20	D20	DDI0_SCL_AUX+	DDI Port #0 TMDS I2C Clock or DP Aux+
Soundwire #1 bidirectional data lane	SNDW_DMIC_DAT1	C21	D21	GND	Power Ground
Power Ground	GND	C22	D22	DDI0_PAIR0-	DDI Port #0 Differential pair 0-
Soundwire #0 clock output	SNDW_DMIC_CLK0	C23	D23	DDI0_PAIR0+	DDI Port #0 Differential pair 0+
Soundwire #0 bidirectional data lane	SNDW_DMIC_DAT0	C24	D24	GND	Power Ground
Power Ground	GND	C25	D25	DDI0_PAIR1-	DDI Port #0 Differential pair 1-
DDI Port #0 TMDS / DP mode selection	DDI0_DDC_AUX_SEL	C26	D26	DDI0_PAIR1+	DDI Port #0 Differential pair 1+
DDI Port #1 TMDS / DP mode selection	DDI1_DDC_AUX_SEL	C27	D27	GND	Power Ground
DDI Port #0 Hot Plug Detect	DDI0_HPD	C28	D28	DDI0_PAIR2-	DDI Port #0 Differential pair 2-
DDI Port #1 Hot Plug Detect	DDI1_HPD	C29	D29	DDI0_PAIR2+	DDI Port #0 Differential pair 2+
eDP Panel Hot Plug Detect	eDP_HPD	C30	D30	GND	Power Ground
eDP Panel Power Enable	eDP_VDD_EN	C31	D31	DDI0_PAIR3-	DDI Port #0 Differential pair 3-
eDP Panel Backlight Enable	eDP_BKLT_EN	C32	D32	DDI0_PAIR3+	DDI Port #0 Differential pair 3+
eDP Panel PWM Control	eDP_BKLTCTL	C33	D33	GND	Power Ground
Power Ground	GND	C34	D34	AC_PRESENT	System Power Present (no battery mode)
DisplayPort Alternate Mode Port #1 Aux Channel-	USB1_AUX-	C35	D35	N.C.	

DisplayPort Alternate Mode Port #1 Aux Channel+	USB1_AUX+	C36	D36	GND	Power Ground
Power Ground	GND	C37	D37	USB1_SSTX0-	USB 3.2 Gen2 2x2 port #1 Tx pair 0-
USB 3.2 Gen2 2x2 port #1 Rx pair 0-	USB1_SSRX0-	C38	D38	USB1_SSTX0+	USB 3.2 Gen2 2x2 port #1 Tx pair 0+
USB 3.2 Gen2 2x2 port #1 Rx pair 0+	USB1_SSRX0+	C39	D39	GND	Power Ground
Power Ground	GND	C40	D40	USB1_SSTX1-	USB 3.2 Gen2 2x2 port #1 Tx pair 1-
USB 3.2 Gen2 2x2 port #1 Rx pair 1-	USB1_SSRX1-	C41	D41	USB1_SSTX1+	USB 3.2 Gen2 2x2 port #1 Tx pair 1+
USB 3.2 Gen2 2x2 port #1 Rx pair 1+	USB1_SSRX1+	C42	D42	GND	Power Ground
Power Ground	GND	C43	D43	USB0_SSTX0-	USB 3.2 Gen2 2x2 port #0 Tx pair 0-
USB 3.2 Gen2 2x2 port #0 Rx pair 0-	USB0_SSRX0-	C44	D44	USB0_SSTX0+	USB 3.2 Gen2 2x2 port #0 Tx pair 0+
USB 3.2 Gen2 2x2 port #0 Rx pair 0+	USB0_SSRX0+	C45	D45	GND	Power Ground
Power Ground	GND	C46	D46	USB0_SSTX1-	USB 3.2 Gen2 2x2 port #0 Tx pair 1-
USB 3.2 Gen2 2x2 port #0 Rx pair 1-	USB0_SSRX1-	C47	D47	USB0_SSTX1+	USB 3.2 Gen2 2x2 port #0 Tx pair 1+
USB 3.2 Gen2 2x2 port #0 Rx pair 1+	USB0_SSRX1+	C48	D48	GND	Power Ground
Power Ground	GND	C49	D49	SATA0_RX-	SATA Port #0 Rx Data -
Carrier Board Boot SPI I/O data #0	BOOT_SPI_IO0	C50	D50	SATA0_RX+	SATA Port #0 Rx Data +
Carrier Board Boot SPI I/O data #1	BOOT_SPI_IO1	C51	D51	GND	Power Ground
Carrier Board Boot SPI I/O data #2	BOOT_SPI_IO2	C52	D52	SATA0_TX-	SATA Port #0 Tx Data -
Carrier Board Boot SPI I/O data #3	BOOT_SPI_IO3	C53	D53	SATA0_TX+	SATA Port #0 Tx Data +
Carrier Board Boot SPI Clock Out	BOOT_SPI_CLK	C54	D54	GND	Power Ground
Power Ground	GND	C55	D55	SATA1_RX-	SATA Port #1 Receive Data -
PCI-e Ref. Clock #0 Differential pair -	PCIe_REFCLK0_HI-	C56	D56	SATA1_RX+	SATA Port #1 Receive Data +
PCI-e Ref. Clock #0 Differential pair +	PCIe_REFCLK0_HI+	C57	D57	GND	Power Ground
Power Ground	GND	C58	D58	SATA1_TX-	SATA Port #1 Transmit Data -
PCI-e Ref. Clock #1 Differential pair -	PCIe_REFCLK0_LO-	C59	D59	SATA1_TX+	SATA Port #1 Transmit Data +
PCI-e Ref. Clock #1 Differential pair +	PCIe_REFCLK0_LO+	C60	D60	GND	Power Ground
Power Ground	GND	C61	D61	PCIe00_TX-	PCI-e Gen3 Lane 0 Transmit -
PCI-e Gen3 Lane 0 receive -	PCIe00_RX-	C62	D62	PCIe00_TX+	PCI-e Gen3 Lane 0 Transmit +
PCI-e Gen3 Lane 0 receive +	PCIe00_RX+	C63	D63	GND	Power Ground
Power Ground	GND	C64	D64	PCIe01_TX-	PCI-e Gen3 Lane 1 Transmit -
PCI-e Gen3 Lane 1 receive -	PCIe01_RX-	C65	D65	PCIe01_TX+	PCI-e Gen3 Lane 1 Transmit +
PCI-e Gen3 Lane 1 receive +	PCIe01_RX+	C66	D66	GND	Power Ground
Power Ground	GND	C67	D67	PCIe02_TX-	PCI-e Gen3 Lane 2 Transmit -
PCI-e Gen3 Lane 2 receive -	PCIe02_RX-	C68	D68	PCIe02_TX+	PCI-e Gen3 Lane 2 Transmit +
PCI-e Gen3 Lane 2 receive +	PCIe02_RX+	C69	D69	GND	Power Ground
Power Ground	GND	C70	D70	PCIe03_TX-	PCI-e Gen3 Lane 3 Transmit -
PCI-e Gen3 Lane 3 receive -	PCIe03_RX-	C71	D71	PCIe03_TX+	PCI-e Gen3 Lane 3 Transmit +
PCI-e Gen3 Lane 3 receive +	PCIe03_RX+	C72	D72	GND	Power Ground
Power Ground	GND	C73	D73	PCIe04_TX-	PCI-e Gen3 Lane 4 Transmit -
PCI-e Gen3 Lane 4 receive -	PCIe04_RX-	C74	D74	PCIe04_TX+	PCI-e Gen3 Lane 4 Transmit +

PCI-e Gen3 Lane 4 receive +	PCIe04_RX+	C75	D75	GND	Power Ground
Power Ground	GND	C76	D76	PCIe05_TX-	PCI-e Gen3 Lane 5 Transmit -
PCI-e Gen3 Lane 5 receive -	PCIe05_RX-	C77	D77	PCIe05_TX+	PCI-e Gen3 Lane 5 Transmit +
PCI-e Gen3 Lane 5 receive +	PCIe05_RX+	C78	D78	GND	Power Ground
Power Ground	GND	C79	D79	PCIe06_TX-	PCI-e Gen3 Lane 6 Transmit -
PCI-e Gen3 Lane 6 receive -	PCIe06_RX-	C80	D80	PCIe06_TX+	PCI-e Gen3 Lane 6 Transmit +
PCI-e Gen3 Lane 6 receive +	PCIe06_RX+	C81	D81	GND	Power Ground
Power Ground	GND	C82	D82	PCIe07_TX-	PCI-e Gen3 Lane 7 Transmit -
PCI-e Gen3 Lane 7 receive -	PCIe07_RX-	C83	D83	PCIe07_TX+	PCI-e Gen3 Lane 7 Transmit +
PCI-e Gen3 Lane 7 receive +	PCIe07_RX+	C84	D84	GND	Power Ground
Power Ground	GND	C85	D85	NBASET0_MDI0-	2.5GbE #0 Differential pair 0-
System Management Bus Clock line	SMB_CLK	C86	D86	NBASET0_MDI0+	2.5GbE #0 Differential pair 0+
System Management Bus Data line	SMB_DAT	C87	D87	GND	Power Ground
System Management Bus Alert Input	SMB_ALERT#	C88	D88	NBASET0_MDI1-	2.5GbE #0 Differential pair 1-
Serial Port #0 Transmit	UART0_TX	C89	D89	NBASET0_MDI1+	2.5GbE #0 Differential pair 1+
Serial Port #0 Receive	UART0_RX	C90	D90	GND	Power Ground
Serial Port #0 Request to Send	UART0_RTS#	C91	D91	NBASET0_MDI2-	2.5GbE #0 Differential pair 2-
Serial Port #0 Clear to Send	UART0_CTS#	C92	D92	NBASET0_MDI2+	2.5GbE #0 Differential pair 2+
General Purpose I2C #0 I/O Clock Line	I2C0_CLK	C93	D93	GND	Power Ground
General Purpose I2C #0 I/O Data Line	I2C0_DAT	C94	D94	NBASET0_MDI3-	2.5GbE #0 Differential pair 3-
Alert Input for I2C #0 interface	I2C0_ALERT#	C95	D95	NBASET0_MDI3+	2.5GbE #0 Differential pair 3+
General Purpose I2C #1 I/O Clock Line	I2C1_CLK	C96	D96	GND	Power Ground
General Purpose I2C #1 I/O Data Line	I2C1_DAT	C97	D97	NBASET0_LINK_MAX#	2.5GbE #0 Max Speed indicator
2.5GbE #0 Software Definable Pin	NBASET0_SDP	C98	D98	NBASET0_LINK_MID#	2.5GbE #0 Mid Speed indicator
2.5GbE #0 Reference Voltage	NBASET0_CTREF	C99	D99	NBASET0_LINK_ACT#	2.5GbE #0 activity indicator
Module Type Definition Pin #1	TYPE1	C100	D100	TYPE2	Module Type Definition Pin #2

COM HPC® Connector CN2 – Rows E & F					
Row E			Row F		
Description	Pin name	Pin	Pin	Pin name	Description
	N.C.	E1	F1	RSVD: FUSA_F1	Raw FuSa interface
Power Ground	GND	E2	F2	RSVD: FUSA_F2	Raw FuSa interface
DDI Port #2 TMDS I2C Data or DP Aux -	DDI2_SDA_AUX-	E3	F3	RSVD: FUSA_F3	Raw FuSa interface
DDI Port #2 TMDS I2C Clock or DP Aux+	DDI2_SCL_AUX+	E4	F4	RSVD: FUSA_F4#	Raw FuSa interface
Power Ground	GND	E5	F5	RSVD: FUSA_F5	Raw FuSa interface
DDI Port #2 Differential pair 0-	DDI2_PAIR0-	E6	F6	RSVD: FUSA_F6	Raw FuSa interface
DDI Port #2 Differential pair 0+	DDI2_PAIR0+	E7	F7	RSVD: FUSA_F7	Raw FuSa interface
Power Ground	GND	E8	F8	RSVD: FUSA_F8	Raw FuSa interface
DDI Port #2 Differential pair 1-	DDI2_PAIR1-	E9	F9	RSVD: FUSA_F9	Raw FuSa interface
DDI Port #2 Differential pair 1+	DDI2_PAIR1+	E10	F10	RSVD: FUSA_F10	Raw FuSa interface
Power Ground	GND	E11	F11	RSVD: FUSA_F11	Raw FuSa interface
DDI Port #2 Differential pair 2-	DDI2_PAIR2-	E12	F12	RSVD: FUSA_F12	Raw FuSa interface
DDI Port #2 Differential pair 2+	DDI2_PAIR2+	E13	F13	RSVD: FUSA_F13	Raw FuSa interface
Power Ground	GND	E14	F14	RSVD: FUSA_F14	Raw FuSa interface
DDI Port #2 Differential pair 3-	DDI2_PAIR3-	E15	F15	RSVD: FUSA_F15	Raw FuSa interface
DDI Port #2 Differential pair 3+	DDI2_PAIR3+	E16	F16	RSVD: FUSA_F16	Raw FuSa interface
Power Ground	GND	E17	F17	RSVD: FUSA_F17	Raw FuSa interface
DDI Port #2 TMDS / DP mode selection	DDI2_DDC_AUX_SEL	E18	F18	RSVD: FUSA_F18	Raw FuSa interface
DDI Port #2 Hot Plug Detect	DDI2_HPD	E19	F19	GND	Power Ground
Power Ground	GND	E20	F20	PCIe32_RX-	PCI-e Gen3 Lane 32 Receive -
PCI-e Gen3 Lane 32 Transmit -	PCIe32_TX-	E21	F21	PCIe32_RX+	PCI-e Gen3 Lane 32 Receive +
PCI-e Gen3 Lane 32 Transmit +	PCIe32_TX+	E22	F22	GND	Power Ground
Power Ground	GND	E23	F23	PCIe33_RX-	PCI-e Gen3 Lane 33 Receive -
PCI-e Gen3 Lane 33 Transmit -	PCIe33_TX-	E24	F24	PCIe33_RX+	PCI-e Gen3 Lane 33 Receive +
PCI-e Gen3 Lane 33 Transmit +	PCIe33_TX+	E25	F25	GND	Power Ground
Power Ground	GND	E26	F26	PCIe34_RX-	PCI-e Gen3 Lane 34 Receive -
PCI-e Gen3 Lane 34 Transmit -	PCIe34_TX-	E27	F27	PCIe34_RX+	PCI-e Gen3 Lane 34 Receive +
PCI-e Gen3 Lane 34 Transmit +	PCIe34_TX+	E28	F28	GND	Power Ground
Power Ground	GND	E29	F29	PCIe35_RX-	PCI-e Gen3 Lane 35 Receive -
PCI-e Gen3 Lane 35 Transmit -	PCIe35_TX-	E30	F30	PCIe35_RX+	PCI-e Gen3 Lane 35 Receive +
PCI-e Gen3 Lane 35 Transmit +	PCIe35_TX+	E31	F31	GND	Power Ground
Power Ground	GND	E32	F32	PCIe36_RX-	PCI-e Gen3 Lane 36 Receive -
PCI-e Gen3 Lane 36 Transmit -	PCIe36_TX-	E33	F33	PCIe36_RX+	PCI-e Gen3 Lane 36 Receive +
PCI-e Gen3 Lane 36 Transmit +	PCIe36_TX+	E34	F34	GND	Power Ground
Power Ground	GND	E35	F35	PCIe37_RX-	PCI-e Gen3 Lane 37 Receive -

PCI-e Gen3 Lane 37 Transmit -	PCIe37_TX-	E36	F36	PCIe37_RX+	PCI-e Gen3 Lane 37 Receive +
PCI-e Gen3 Lane 37 Transmit +	PCIe37_TX+	E37	F37	GND	Power Ground
Power Ground	GND	E38	F38	PCIe38_RX-	PCI-e Gen3 Lane 38 Receive -
PCI-e Gen3 Lane 38 Transmit -	PCIe38_TX-	E39	F39	PCIe38_RX+	PCI-e Gen3 Lane 38 Receive +
PCI-e Gen3 Lane 38 Transmit +	PCIe38_TX+	E40	F40	GND	Power Ground
Power Ground	GND	E41	F41	PCIe16_RX-	PCI-e Gen3 Lane 16 Receive -
PCI-e Gen3 Lane 39 Transmit -	PCIe39_TX-	E42	F42	PCIe16_RX+	PCI-e Gen3 Lane 16 Receive +
PCI-e Gen3 Lane 39 Transmit +	PCIe39_TX+	E43	F43	GND	Power Ground
Power Ground	GND	E44	F44	PCIe17_RX-	PCI-e Gen3 Lane 17 Receive -
PCI-e Gen3 Lane 16 Transmit -	PCIe16_TX-	E45	F45	PCIe17_RX+	PCI-e Gen3 Lane 17 Receive +
PCI-e Gen3 Lane 16 Transmit +	PCIe16_TX+	E46	F46	GND	Power Ground
Power Ground	GND	E47	F47	PCIe18_RX-	PCI-e Gen3 Lane 18 Receive -
PCI-e Gen3 Lane 17 Transmit -	PCIe17_TX-	E48	F48	PCIe18_RX+	PCI-e Gen3 Lane 18 Receive +
PCI-e Gen3 Lane 17 Transmit +	PCIe17_TX+	E49	F49	GND	Power Ground
Power Ground	GND	E50	F50	PCIe19_RX-	PCI-e Gen3 Lane 19 Receive -
PCI-e Gen3 Lane 18 Transmit -	PCIe18_TX-	E51	F51	PCIe19_RX+	PCI-e Gen3 Lane 19 Receive +
PCI-e Gen3 Lane 18 Transmit +	PCIe18_TX+	E52	F52	GND	Power Ground
Power Ground	GND	E53	F53	PCIe20_RX-	PCI-e Gen3 Lane 20 Receive -
PCI-e Gen3 Lane 19 Transmit -	PCIe19_TX-	E54	F54	PCIe20_RX+	PCI-e Gen3 Lane 20 Receive +
PCI-e Gen3 Lane 19 Transmit +	PCIe19_TX+	E55	F55	GND	Power Ground
Power Ground	GND	E56	F56	PCIe21_RX-	PCI-e Gen3 Lane 21 Receive -
PCI-e Gen3 Lane 20 Transmit -	PCIe20_TX-	E57	F57	PCIe21_RX+	PCI-e Gen3 Lane 21 Receive +
PCI-e Gen3 Lane 20 Transmit +	PCIe20_TX+	E58	F58	GND	Power Ground
Power Ground	GND	E59	F59	PCIe22_RX-	PCI-e Gen3 Lane 22 Receive -
PCI-e Gen3 Lane 21 Transmit -	PCIe21_TX-	E60	F60	PCIe22_RX+	PCI-e Gen3 Lane 22 Receive +
PCI-e Gen3 Lane 21 Transmit +	PCIe21_TX+	E61	F61	GND	Power Ground
Power Ground	GND	E62	F62	PCIe23_RX-	PCI-e Gen3 Lane 23 Receive -
PCI-e Gen3 Lane 22 Transmit -	PCIe22_TX-	E63	F63	PCIe23_RX+	PCI-e Gen3 Lane 23 Receive +
PCI-e Gen3 Lane 22 Transmit +	PCIe22_TX+	E64	F64	GND	Power Ground
Power Ground	GND	E65	F65	N.C.	
PCI-e Gen3 Lane 23 Transmit -	PCIe23_TX-	E66	F66	N.C.	
PCI-e Gen3 Lane 23 Transmit +	PCIe23_TX+	E67	F67	GND	Power Ground
Power Ground	GND	E68	F68	N.C.	
	N.C.	E69	F69	N.C.	
	N.C.	E70	F70	GND	Power Ground
	N.C.	E71	F71	NBASET1_MDI0-	2.5GbE #1 Differential pair 0-
	N.C.	E72	F72	NBASET1_MDI0+	2.5GbE #1 Differential pair 0+
	N.C.	E73	F73	GND	Power Ground
	N.C.	E74	F74	NBASET1_MDI1-	2.5GbE #1 Differential pair 1-

	N.C.	E75	F75	NBASET1_MDI1+	2.5GbE #1 Differential pair 1+
	N.C.	E76	F76	GND	Power Ground
	N.C.	E77	F77	NBASET1_MDI2-	2.5GbE #1 Differential pair 2-
2.5GbE #0 Reference Voltage	NBASET1_CTREF	E78	F78	NBASET1_MDI2+	2.5GbE #1 Differential pair 2+
2.5GbE #1 Software Definable Pin	NBASET1_SDP	E79	F79	GND	Power Ground
2.5GbE #1 Mid Speed indicator	NBASET1_LINK_MID#	E80	F80	NBASET1_MDI3-	2.5GbE #1 Differential pair 3-
2.5GbE #1 activity indicator	NBASET1_LINK_ACT#	E81	F81	NBASET1_MDI3+	2.5GbE #1 Differential pair 3+
2.5GbE #1 Max Speed indicator	NBASET1_LINK_MAX#	E82	F82	GND	Power Ground
Power Ground	GND	E83	F83	RSVD: FUSA_83	Raw FuSa interface
	N.C.	E84	F84	RSVD: FUSA_F84	Raw FuSa interface
	N.C.	E85	F85	GND	Power Ground
Power Ground	GND	E86	F86	ETH0_TX-	KR Ethernet #0 Transmit -
KR Ethernet #0 Receive -	ETH0_RX-	E87	F87	ETH0_TX+	KR Ethernet #0 Transmit +
KR Ethernet #0 Receive +	ETH0_RX+	E88	F88	GND	Power Ground
Power Ground	GND	E89	F89	ETH1_TX-	KR Ethernet #1 Transmit -
KR Ethernet #1 Receive -	ETH1_RX-	E90	F90	ETH1_TX+	KR Ethernet #1 Transmit +
KR Ethernet #1 Receive +	ETH1_RX+	E91	F91	GND	Power Ground
Power Ground	GND	E92	F92	PCIe_REFCLK2-	PCI-e Ref. Clock #3 Differential pair -
PCI-e Ref. Clock #2 Differential pair -	PCIe_REFCLK1-	E93	F93	PCIe_REFCLK2+	PCI-e Ref. Clock #3 Differential pair +
PCI-e Ref. Clock #2 Differential pair +	PCIe_REFCLK1+	E94	F94	GND	Power Ground
Power Ground	GND	E95	F95	RSVD: FUSA_F95	Raw FuSa interface
PCI-e Clock request #2	PCIe_CLKREQ1#	E96	F96	ETH0-1_PRSNT#	KR Ethernet #0-1 PHY presence:
PCI-e Clock request #3	PCIe_CLKREQ2#	E97	F97	ETH0-1_PHY_RST#	KR Ethernet #0-1 Reset
	N.C.	E98	F98	ETH0_SDP	KR Ethernet #0 Software Definable Pin
	N.C.	E99	F99	ETH1_SDP	KR Ethernet #1 Software Definable Pin
	N.C.	E100	F100	N.C.	

COM HPC® Connector CN2 – Rows G & H					
Row G			Row H		
Description	Pin name	Pin	Pin	Pin name	Description
Standby power input: +5.0V	VCC_5V_SBY	G1	H1	GND	Power Ground
Power Ground	GND	G2	H2	USB2_SSTX0-	USB 3.2 Gen2 2x2 port #2 Tx pair 0-
USB 3.2 Gen2 2x2 port #2 Rx pair 0-	USB2_SSRX0-	G3	H3	USB2_SSTX0+	USB 3.2 Gen2 2x2 port #2 Tx pair 0+
USB 3.2 Gen2 2x2 port #2 Rx pair 0+	USB2_SSRX0+	G4	H4	GND	Power Ground
Power Ground	GND	G5	H5	USB2_SSTX1-	USB 3.2 Gen2 2x2 port #2 Tx pair 1-
USB 3.2 Gen2 2x2 port #2 Rx pair 1-	USB2_SSRX1-	G6	H6	USB2_SSTX1+	USB 3.2 Gen2 2x2 port #2 Tx pair 1+
USB 3.2 Gen2 2x2 port #2 Rx pair 1+	USB2_SSRX1+	G7	H7	GND	Power Ground
Power Ground	GND	G8	H8	USB3_SSTX0-	USB 3.2 Gen2 2x2 port #3 Tx pair 0-
USB 3.2 Gen2 2x2 port #3 Rx pair 0-	USB3_SSRX0-	G9	H9	USB3_SSTX0+	USB 3.2 Gen2 2x2 port #3 Tx pair 0+
USB 3.2 Gen2 2x2 port #3 Rx pair 0+	USB3_SSRX0+	G10	H10	GND	Power Ground
Power Ground	GND	G11	H11	USB3_SSTX1-	USB 3.2 Gen2 2x2 port #3 Tx pair 1-
USB 3.2 Gen2 2x2 port #3 Rx pair 1-	USB3_SSRX1-	G12	H12	USB3_SSTX1+	USB 3.2 Gen2 2x2 port #3 Tx pair 1+
USB 3.2 Gen2 2x2 port #3 Rx pair 1+	USB3_SSRX1+	G13	H13	GND	Power Ground
Power Ground	GND	G14	H14	USB2_AUX-	DisplayPort Alternate Mode Port #2 Aux -
USB4 Port #3 Alt Modes Sideband RX	USB3_LSRX	G15	H15	USB2_AUX+	DisplayPort Alternate Mode Port #2 Aux+
USB4 Port #3 Alt Modes Sideband TX	USB3_LSTX	G16	H16	GND	Power Ground
USB4 Port #2 Alt Modes Sideband RX	USB2_LSRX	G17	H17	USB3_AUX-	DisplayPort Alternate Mode Port #3 Aux -
USB4 Port #2 Alt Modes Sideband TX	USB2_LSTX	G18	H18	USB3_AUX+	DisplayPort Alternate Mode Port #3 Aux+
PCI-e Graphics lane reversal input	PEG_LANE_REV#	G19	H19	GND	Power Ground
Power Ground	GND	G20	H20	PCIe40_TX-	PCI-e Gen3 Lane 40 Transmit -
PCI-e Gen3 Lane 40 Receive -	PCIe40_RX-	G21	H21	PCIe40_TX+	PCI-e Gen3 Lane 40 Transmit +
PCI-e Gen3 Lane 40 Receive +	PCIe40_RX+	G22	H22	GND	Power Ground
Power Ground	GND	G23	H23	PCIe41_TX-	PCI-e Gen3 Lane 41 Transmit -
PCI-e Gen3 Lane 41 Receive -	PCIe41_RX-	G24	H24	PCIe41_TX+	PCI-e Gen3 Lane 41 Transmit +
PCI-e Gen3 Lane 41 Receive +	PCIe41_RX+	G25	H25	GND	Power Ground
Power Ground	GND	G26	H26	PCIe42_TX-	PCI-e Gen3 Lane 42 Transmit -
PCI-e Gen3 Lane 42 Receive -	PCIe42_RX-	G27	H27	PCIe42_TX+	PCI-e Gen3 Lane 42 Transmit +
PCI-e Gen3 Lane 42 Receive +	PCIe42_RX+	G28	H28	GND	Power Ground
Power Ground	GND	G29	H29	PCIe43_TX-	PCI-e Gen3 Lane 43 Transmit -
PCI-e Gen3 Lane 43 Receive -	PCIe43_RX-	G30	H30	PCIe43_TX+	PCI-e Gen3 Lane 43 Transmit +
PCI-e Gen3 Lane 43 Receive +	PCIe43_RX+	G31	H31	GND	Power Ground
Power Ground	GND	G32	H32	PCIe44_TX-	PCI-e Gen3 Lane 44 Transmit -
PCI-e Gen3 Lane 44 Receive -	PCIe44_RX-	G33	H33	PCIe44_TX+	PCI-e Gen3 Lane 44 Transmit +
PCI-e Gen3 Lane 44 Receive +	PCIe44_RX+	G34	H34	GND	Power Ground
Power Ground	GND	G35	H35	PCIe45_TX-	PCI-e Gen3 Lane 45 Transmit -

PCI-e Gen3 Lane 45 Receive -	PCIe45_RX-	G36	H36	PCIe45_TX+	PCI-e Gen3 Lane 45 Transmit +
PCI-e Gen3 Lane 45 Receive +	PCIe45_RX+	G37	H37	GND	Power Ground
Power Ground	GND	G38	H38	PCIe46_TX-	PCI-e Gen3 Lane 46 Transmit -
PCI-e Gen3 Lane 46 Receive -	PCIe46_RX-	G39	H39	PCIe46_TX+	PCI-e Gen3 Lane 46 Transmit +
PCI-e Gen3 Lane 46 Receive +	PCIe46_RX+	G40	H40	GND	Power Ground
Power Ground	GND	G41	H41	PCIe47_TX-	PCI-e Gen3 Lane 47 Transmit -
PCI-e Gen3 Lane 47 Receive -	PCIe47_RX-	G42	H42	PCIe47_TX+	PCI-e Gen3 Lane 47 Transmit +
PCI-e Gen3 Lane 47 Receive +	PCIe47_RX+	G43	H43	GND	Power Ground
Power Ground	GND	G44	H44	PCIe24_TX-	PCI-e Gen3 Lane 24 Transmit -
PCI-e Gen3 Lane 24 Receive -	PCIe24_RX-	G45	H45	PCIe24_TX+	PCI-e Gen3 Lane 24 Transmit +
PCI-e Gen3 Lane 24 Receive +	PCIe24_RX+	G46	H46	GND	Power Ground
Power Ground	GND	G47	H47	PCIe25_TX-	PCI-e Gen3 Lane 25 Transmit -
PCI-e Gen3 Lane 25 Receive -	PCIe25_RX-	G48	H48	PCIe25_TX+	PCI-e Gen3 Lane 25 Transmit +
PCI-e Gen3 Lane 25 Receive +	PCIe25_RX+	G49	H49	GND	Power Ground
Power Ground	GND	G50	H50	PCIe26_TX-	PCI-e Gen3 Lane 26 Transmit -
PCI-e Gen3 Lane 26 Receive -	PCIe26_RX-	G51	H51	PCIe26_TX+	PCI-e Gen3 Lane 26 Transmit +
PCI-e Gen3 Lane 26 Receive +	PCIe26_RX+	G52	H52	GND	Power Ground
Power Ground	GND	G53	H53	PCIe27_TX-	PCI-e Gen3 Lane 27 Transmit -
PCI-e Gen3 Lane 27 Receive -	PCIe27_RX-	G54	H54	PCIe27_TX+	PCI-e Gen3 Lane 27 Transmit +
PCI-e Gen3 Lane 27 Receive +	PCIe27_RX+	G55	H55	GND	Power Ground
Power Ground	GND	G56	H56	PCIe28_TX-	PCI-e Gen3 Lane 28 Transmit -
PCI-e Gen3 Lane 28 Receive -	PCIe28_RX-	G57	H57	PCIe28_TX+	PCI-e Gen3 Lane 28 Transmit +
PCI-e Gen3 Lane 28 Receive +	PCIe28_RX+	G58	H58	GND	Power Ground
Power Ground	GND	G59	H59	PCIe29_TX-	PCI-e Gen3 Lane 29 Transmit -
PCI-e Gen3 Lane 29 Receive -	PCIe29_RX-	G60	H60	PCIe29_TX+	PCI-e Gen3 Lane 29 Transmit +
PCI-e Gen3 Lane 29 Receive +	PCIe29_RX+	G61	H61	GND	Power Ground
Power Ground	GND	G62	H62	PCIe30_TX-	PCI-e Gen3 Lane 30 Transmit -
PCI-e Gen3 Lane 30 Receive -	PCIe30_RX-	G63	H63	PCIe30_TX+	PCI-e Gen3 Lane 30 Transmit +
PCI-e Gen3 Lane 30 Receive +	PCIe30_RX+	G64	H64	GND	Power Ground
Power Ground	GND	G65	H65	PCIe31_TX-	PCI-e Gen3 Lane 31 Transmit -
PCI-e Gen3 Lane 31 Receive -	PCIe31_RX-	G66	H66	PCIe31_TX+	PCI-e Gen3 Lane 31 Transmit +
PCI-e Gen3 Lane 31 Receive +	PCIe31_RX+	G67	H67	GND	Power Ground
Power Ground	GND	G68	H68	N.C.	
	RSVD	G69	H69	N.C.	
	RSVD	G70	H70	GND	Power Ground
Power Ground	GND	G71	H71	CSI1_RX0-	CSI Port #1 Data Input pair 0-
CSI Port #0 Data Input pair 0-	CSI0_RX0-	G72	H72	CSI1_RX0+	CSI Port #1 Data Input pair 0+
CSI Port #0 Data Input pair 0+	CSI0_RX0+	G73	H73	GND	Power Ground
Power Ground	GND	G74	H74	CSI1_RX1-	CSI Port #1 Data Input pair 1-

CSI Port #0 Data Input pair 1-	CSI0_RX1-	G75	H75	CSI1_RX1+	CSI Port #1 Data Input pair 1+
CSI Port #0 Data Input pair 1+	CSI0_RX1+	G76	H76	GND	Power Ground
Power Ground	GND	G77	H77	CSI1_RX2-	CSI Port #1 Data Input pair 2-
CSI Port #0 Data Input pair 2-	CSI0_RX2-	G78	H78	CSI1_RX2+	CSI Port #1 Data Input pair 2-
CSI Port #0 Data Input pair 2-	CSI0_RX2+	G79	H79	GND	Power Ground
Power Ground	GND	G80	H80	CSI1_RX3-	CSI Port #1 Data Input pair 3-
CSI Port #0 Data Input pair 3-	CSI0_RX3-	G81	H81	CSI1_RX3+	CSI Port #1 Data Input pair 3+
CSI Port #0 Data Input pair 3+	CSI0_RX3+	G82	H82	GND	Power Ground
Power Ground	GND	G83	H83	CSI1_CLK-	CSI Port #1 Clock Pair-
CSI Port #0 Clock Pair-	CSI0_CLK-	G84	H84	CSI1_CLK+	CSI Port #1 Clock Pair+
CSI Port #0 Clock Pair+	CSI0_CLK+	G85	H85	GND	Power Ground
Power Ground	GND	G86	H86	CSI1_I2C_CLK	CSI Port #1 I2C Clock Line
CSI Port #0 I2C Clock Line	CSI0_I2C_CLK	G87	H87	CSI1_I2C_DAT	CSI Port #1 I2C Data Line
CSI Port #0 I2C Data Line	CSI0_I2C_DAT	G88	H88	CSI1_MCLK	CSI Port #1 Master Clock Output
CSI Port #0 Master Clock Output	CSI0_MCLK	G89	H89	CSI1_RST#	CSI Port #1 Reset Output
CSI Port #0 Reset Output	CSI0_RST#	G90	H90	CSI1_ENA	CSI Port #1 Enable Output
CSI Port #0 Enable Output	CSI0_ENA	G91	H91	GND	Power Ground
Power Ground	GND	G92	H92	N.C.	
	N.C.	G93	H93	N.C.	
	N.C.	G94	H94	GND	Power Ground
Power Ground	GND	G95	H95	N.C.	
KR Ethernet #0-1 SFP module Clock	ETH0-1_I2C_CLK	G96	H96	N.C.	
KR Ethernet #0-1 SFP module Data	ETH0-1_I2C_DAT	G97	H97	GND	Power Ground
KR Ethernet #0-1 PHY interrupt	ETH0-1_PHY_INT#	G98	H98	ETH0-1_MDIO_CLK	KR Ethernet #0-1 MDIO interface Clock
KR Ethernet #0-1 IO Interrupt	ETH0-1_INT#	G99	H99	ETH0-1_MDIO_DAT	KR Ethernet #0-1 MDIO interface Data
	N.C.	G100	H100	N.C.	

3.3.2 PCI-e Slots

COM HPC specifications foresee up to 48 PCI-e x1 lanes, which can also be grouped (depending on the COM HPC module's chipset/processor), divided in 5 groups of PCI-e lanes. Each group is provided with its own reference clock.

On HC78 carrier board, these lanes are so used:

PCI-e lanes #0..#3 are carried to a single PCI-e x4 slot, CN73.

PCI-e lanes #4..#7 are carried to another single PCI-e x4 slot, CN74.

PCI-e lanes #8..#11 are carried to an M.2 Socket 3 Key M NVME slot, CN12.

PCI-e lanes #12..#15 are carried to a second M.2 Socket 3 Key M NVME slot, CN14.

PCI-e lanes #16..#31 are carried to a single PCI-e x16 slot, CN13. This one can also be used for PCI-e graphics (PEG) Cards

PCI-e lanes #32..#47 are carried to another PCI-e x16 slot, CN72.

All of the previous slots have a dedicated reference clock, which is managed directly by the COM HPC Client module or by a PCI-e clock buffer embedded on the carrier board.

Please be aware that availability of all sixteen PCI express lanes depends on the COM HPC™ module used.

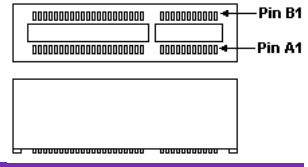
Please check the User Manual of the COM HPC™ module used for details about the availability of these lanes and all possible groupings that can be applied to these lanes.

On HC78 carrier board, the PCI-express compatibility is ensured with devices up to Gen3.

3.3.2.1 PCI-e x4 Slots

The HC78 board offer the possibility for expansion through two standard PCI-e x4 card edge connectors CN73 and CN74

The PCI-e x4 slots are type LOTES p/n APC50015-P006AC or equivalent, with the pinout shown in the following tables.



PCI-e x 4 Slot CN73					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	PRSNT1#	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	Not connected
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	Not connected
Power Ground	GND	B7	A7	JTAG4	Not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	Not connected
Not Connected	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx4_1_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIEx4_1_CLK_P	PCI-e reference clock lane +, derived by PCIE_CK_REF+ using a Clock Buffer
PCI-e Transmitter lane 0+	PCIE_TX0+	B14	A14	PCIEx4_1_CLK_N	PCI-e reference clock lane +, derived by PCIE_CK_REF- using a Clock Buffer
PCI-e Transmitter lane 0-	PCIE_TX0-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX0+	PCI-e Receiver lane 0+

Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX0-	PCI-e Receiver lane 0-
Power Ground	GND	B18	A18	GND	Power Ground
PCI-e Transmitter lane 1+	PCIE_TX1+	B19	A19	RSVD	Not Connected
PCI-e Transmitter lane 1-	PCIE_TX1-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX1+	PCI-e Receiver lane 1+
Power Ground	GND	B22	A22	PCIE_RX1-	PCI-e Receiver lane 1-
PCI-e Transmitter lane 2+	PCIE_TX2+	B23	A23	GND	Power Ground
PCI-e Transmitter lane 2-	PCIE_TX2-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX2+	PCI-e Receiver lane 2+
Power Ground	GND	B26	A26	PCIE_RX2-	PCI-e Receiver lane 2-
PCI-e Transmitter lane 3+. Signal available to this slot by setting jumper JP6 in 2-3 position.	PCIE_TX3+	B27	A27	GND	Power Ground
PCI-e Transmitter lane 3-. Signal available to this slot by setting jumper JP6 in 2-3 position.	PCIE_TX3-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX3+	PCI-e Receiver lane 3+. Signal available to this slot by setting jumper JP6 in 2-3 position.
Not Connected	RSVD	B30	A30	PCIE_RX3-	PCI-e Receiver lane 3-. Signal available to this slot by setting jumper JP6 in 2-3 position.
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not Connected

!

Please be aware that PCI-e management on the carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B81/B48/B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B81 or B48 or B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

PCI-e x 4 Slot CN74					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	PRSNT1#	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	Not connected
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	Not connected
Power Ground	GND	B7	A7	JTAG4	Not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	Not connected
Not Connected	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx4_2_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIEx4_2_CLK_P	PCI-e reference clock lane +, derived by PCIE_CK_REF+ using a Clock Buffer
PCI-e Transmitter lane 4+	PCIE_TX4+	B14	A14	PCIEx4_2_CLK_N	PCI-e reference clock lane +, derived by PCIE_CK_REF- using a Clock Buffer
PCI-e Transmitter lane 4-	PCIE_TX4-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX4+	PCI-e Receiver lane 4+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX4-	PCI-e Receiver lane 4-
Power Ground	GND	B18	A18	GND	Power Ground
PCI-e Transmitter lane 5+	PCIE_TX5+	B19	A19	RSVD	Not Connected

PCI-e Transmitter lane 5-	PCIE_TX5-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX5+	PCI-e Receiver lane 5+
Power Ground	GND	B22	A22	PCIE_RX5-	PCI-e Receiver lane 5-
PCI-e Transmitter lane 6+	PCIE_TX6+	B23	A23	GND	Power Ground
PCI-e Transmitter lane 6-	PCIE_TX6-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX6+	PCI-e Receiver lane 6+
Power Ground	GND	B26	A26	PCIE_RX6-	PCI-e Receiver lane 6-
PCI-e Transmitter lane 7+	PCIE_TX7+	B27	A27	GND	Power Ground
PCI-e Transmitter lane 7-	PCIE_TX7-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX7+	PCI-e Receiver lane 7+
Not Connected	RSVD	B30	A30	PCIE_RX7-	PCI-e Receiver lane 7-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not Connected

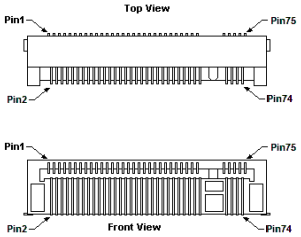
! Please be aware that PCI-e management on the carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

3.3.2.2 M.2 2280 Socket 3 Key M NVMe Slots

M.2 NVMe Slot (Socket 3 Key M type 2280) – CN12			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	+3.3V_RUN
3	GND	4	+3.3V_RUN
5	PCIe_Rx11-	6	---
7	PCIE_Rx11+	8	---
9	GND	10	---
11	PCIE_Tx11-	12	+3.3V_RUN
13	PCIE_Tx11+	14	+3.3V_RUN
15	GND	16	+3.3V_RUN
17	PCIE_Rx10-	18	+3.3V_RUN
19	PCIE_Rx10+	20	---
21	GND	22	---
23	PCIE_Tx10-	24	---
25	PCIE_Tx10+	26	---
27	GND	28	---
29	PCIE_Rx9-	30	---
31	PCIE_Rx9+	32	---
33	GND	34	---
35	PCIE_Tx8-	36	---
37	PCIE_Tx8+	38	---
39	GND	40	M.2_SMB_CLK
41	PCIE_Rx8-	42	M.2_SMB_DAT
43	PCIE_Rx8+	44	---
45	GND	46	---
47	PCIE_Tx8-	48	---
49	PCIE_Tx8+	50	M.2_1_RST#
51	GND	52	M.2_1_CLK_REQ#
53	M.2_1_CLK-	54	---
55	M.2_1_CLK+	56	---
57	GND	58	---
67	---	68	---
69	---	70	+3.3V_RUN
71	GND	72	+3.3V_RUN
73	GND	74	+3.3V_RUN
75	GND		

Mass storage devices can be connected to the M.2 Key M Slot present on the board, which allows the plugging of M.2 High Capacity SSD drives with PCI-e x4 interface, depending on installed module implementation.



The connectors used for the M.2 SSD slot are CN12 and CN14, which are standard 75 pin M.2 Key M connector, type LOTES p/n APCI0359-P003A, H=8.5mm, with the pinout shown in the respective tables.

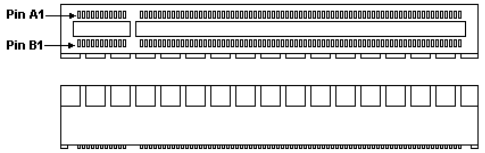
On the board, Threaded Spacers allow the placement of M.2 Socket 3 Key M PCI-e SSD modules in 2280size.

M.2 NVMe Slot (Socket 3 Key M type 2280) – CN14

Pin	Signal	Pin	Signal
1	GND	2	+3.3V_RUN
3	GND	4	+3.3V_RUN
5	PCIe_Rx15-	6	---
7	PCIE_Rx15+	8	---
9	GND	10	---
11	PCIE_Tx15-	12	+3.3V_RUN
13	PCIE_Tx15+	14	+3.3V_RUN
15	GND	16	+3.3V_RUN
17	PCIE_Rx14-	18	+3.3V_RUN
19	PCIE_Rx14+	20	---
21	GND	22	---
23	PCIE_Tx14-	24	---
25	PCIE_Tx14+	26	---
27	GND	28	---
29	PCIE_Rx13-	30	---
31	PCIE_Rx13+	32	---
33	GND	34	---
35	PCIE_Tx13-	36	---
37	PCIE_Tx13+	38	---
39	GND	40	M.2_SMB_CLK
41	PCIE_Rx12-	42	M.2_SMB_DAT
43	PCIE_Rx12+	44	---
45	GND	46	---
47	PCIE_Tx12-	48	---
49	PCIE_Tx12+	50	M.2_2_RST#
51	GND	52	M.2_2_CLK_REQ#
53	M.2_2_CLK-	54	---
55	M.2_2_CLK+	56	---
57	GND	58	---
67	---	68	---
69	---	70	+3.3V_RUN
71	GND	72	+3.3V_RUN
73	GND	74	+3.3V_RUN
75	GND		

3.3.2.3 PCI-e x16 Slots

The HC78 board offer the possibility of additional expansion through two standard PCI-e x16 card edge connectors CN13 and CN72.



PCI-e x16 slots are type LOTES p/n APCI0599-P002C01or equivalent, with the pinout shown in the following tables.

It is also possible to use this connector to increase the graphical capabilities of the board by using PCI-e lanes #16..#31 as PCI Express Graphics x16 bus (PEG) interface.

Associated to PCI-e x16 slot CN13, a dedicated 2-way jumper, JP17, allows to force the Lane reversal order

JP17 position	PEG LANE Order
Not inserted	Normal PEG Lane Order
Inserted	Reversed PEG Lane Order

Please be aware that availability of these PCI express lanes depends on the COM HPC™ module used.

Please check the User Manual of the COM HPC™ module used for details about the availability of these lanes and all possible groupings that can be applied to these lanes.

PCI Express Graphics x16 Slot- CN13					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	GND	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	TCK, tied to GND with 4K7Ω resistor
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	TDI, tied to +3.3V_RUN with 4K7Ω resistor
Power Ground	GND	B7	A7	JTAG4	Test Data Out, not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	TMS, tied to +3.3V_RUN with 4K7Ω resistor
TRST#, tied to GND with 4K7Ω resistor	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail

Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx16_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PEG_CLK_P	PEG reference clock lane + from module pin PCIE_REFCLK1+
PCI Express Transmit Pair 16+	PCIE_TX16+	B14	A14	PEG_CLK_N	PEG reference clock lane - from module pin PCIE_REFCLK1-
PCI Express Transmit Pair 16-	PCIE_TX16-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX16+	PCI Express Receive Pair 16+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX16-	PCI Express Receive Pair 16-
Power Ground	GND	B18	A18	GND	Power Ground
PCI Express Transmit Pair 17+	PCIE_TX17+	B19	A19	RSVD	Not connected
PCI Express Transmit Pair 17-	PCIE_TX17-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX17+	PCI Express Receive Pair 17+
Power Ground	GND	B22	A22	PCIE_RX17-	PCI Express Receive Pair 17-
PCI Express Transmit Pair 18+	PCIE_TX18+	B23	A23	GND	Power Ground
PCI Express Transmit Pair 18-	PCIE_TX18-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX18+	PCI Express Receive Pair 18+
Power Ground	GND	B26	A26	PCIE_RX18-	PCI Express Receive Pair 18-
PCI Express Transmit Pair 19+	PCIE_TX19+	B27	A27	GND	Power Ground
PCI Express Transmit Pair 19-	PCIE_TX19-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX19+	PCI Express Receive Pair 19+
Not Connected	RSVD	B30	A30	PCIE_RX19-	PCI Express Receive Pair 19-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not connected

PCI Express Transmit Pair 20+	PCIE_TX20+	B33	A33	RSVD	Not connected
PCI Express Transmit Pair 20-	PCIE_TX20-	B34	A34	GND	Power Ground
Power Ground	GND	B35	A35	PCIE_RX20+	PCI Express Receive Pair 20+
Power Ground	GND	B36	A36	PCIE_RX20-	PCI Express Receive Pair 20-
PCI Express Transmit Pair 21+	PCIE_TX21+	B37	A37	GND	Power Ground
PCI Express Transmit Pair 21-	PCIE_TX21-	B38	A38	GND	Power Ground
Power Ground	GND	B39	A39	PCIE_RX21+	PCI Express Receive Pair 21+
Power Ground	GND	B40	A40	PCIE_RX21-	PCI Express Receive Pair 21-
PCI Express Transmit Pair 22+	PCIE_TX22+	B41	A41	GND	Power Ground
PCI Express Transmit Pair 22-	PCIE_TX22-	B42	A42	GND	Power Ground
Power Ground	GND	B43	A43	PCIE_RX22+	PCI Express Receive Pair 22+
Power Ground	GND	B44	A44	PCIE_RX22-	PCI Express Receive Pair 22-
PCI Express Transmit Pair 23+	PCIE_TX23+	B45	A45	GND	Power Ground
PCI Express Transmit Pair 23-	PCIE_TX23-	B46	A46	GND	Power Ground
Power Ground	GND	B47	A47	PCIE_RX23+	PCI Express Receive Pair 23+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B48	A48	PCIE_RX23-	PCI Express Receive Pair 23-
Power Ground	GND	B49	A49	GND	Power Ground
PCI Express Transmit Pair 24+	PCIE_TX24+	B50	A50	RSVD	Not connected
PCI Express Transmit Pair 24-	PCIE_TX24-	B51	A51	GND	Power Ground
Power Ground	GND	B52	A52	PCIE_RX24+	PCI Express Receive Pair 24+
Power Ground	GND	B53	A53	PCIE_RX24-	PCI Express Receive Pair 24-
PCI Express Transmit Pair 25+	PCIE_TX25+	B54	A54	GND	Power Ground
PCI Express Transmit Pair 25-	PCIE_TX25-	B55	A55	GND	Power Ground
Power Ground	GND	B56	A56	PCIE_RX25+	PCI Express Receive Pair 25+
Power Ground	GND	B57	A57	PCIE_RX25-	PCI Express Receive Pair 25-
PCI Express Transmit Pair 26+	PCIE_TX26+	B58	A58	GND	Power Ground
PCI Express Transmit Pair 26-	PCIE_TX26-	B59	A59	GND	Power Ground
Power Ground	GND	B60	A60	PCIE_RX26+	PCI Express Receive Pair 26+

Power Ground	GND	B61	A61	PCIE_RX26-	PCI Express Receive Pair 26-
PCI Express Transmit Pair 27+	PCIE_TX27+	B62	A62	GND	Power Ground
PCI Express Transmit Pair 27-	PCIE_TX27-	B63	A63	GND	Power Ground
Power Ground	GND	B64	A64	PCIE_RX27+	PCI Express Receive Pair 27+
Power Ground	GND	B65	A65	PCIE_RX27-	PCI Express Receive Pair 27-
PCI Express Transmit Pair 28+	PCIE_TX28+	B66	A66	GND	Power Ground
PCI Express Transmit Pair 28-	PCIE_TX28-	B67	A67	GND	Power Ground
Power Ground	GND	B68	A68	PCIE_RX28+	PCI Express Receive Pair 28+
Power Ground	GND	B69	A69	PCIE_RX28-	PCI Express Receive Pair 28-
PCI Express Transmit Pair 29+	PCIE_TX29+	B70	A70	GND	Power Ground
PCI Express Transmit Pair 29-	PCIE_TX29-	B71	A71	GND	Power Ground
Power Ground	GND	B72	A72	PCIE_RX29+	PCI Express Receive Pair 29+
Power Ground	GND	B73	A73	PCIE_RX29-	PCI Express Receive Pair 29-
PCI Express Transmit Pair 30+	PCIE_TX30+	B74	A74	GND	Power Ground
PCI Express Transmit Pair 30-	PCIE_TX30-	B75	A75	GND	Power Ground
Power Ground	GND	B76	A76	PCIE_RX30+	PCI Express Receive Pair 30+
Power Ground	GND	B77	A77	PCIE_RX30-	PCI Express Receive Pair 30-
PCI Express Transmit Pair 31+	PCIE_TX31+	B78	A78	GND	Power Ground
PCI Express Transmit Pair 31-	PCIE_TX31-	B79	A79	GND	Power Ground
Power Ground	GND	B80	A80	PCIE_RX31+	PCI Express Receive Pair 31+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B81	A81	PCIE_RX31-	PCI Express Receive Pair 31-
Not Connected	RSVD	B82	A82	GND	Power Ground

! Please be aware that PCI-e management on the carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B81/B48/B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B81 or B48 or B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

PCI Express Graphics x16 Slot- CN72					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	GND	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	TCK, tied to GND with 4K7Ω resistor
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	TDI, tied to +3.3V_RUN with 4K7Ω resistor
Power Ground	GND	B7	A7	JTAG4	Test Data Out, not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	TMS, tied to +3.3V_RUN with 4K7Ω resistor
TRST#, tied to GND with 4K7Ω resistor	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx16_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIEx16_CLK_P	PCI-e reference clock lane + from module pin PCIE_REFCLK2+
PCI Express Transmit Pair 32+	PCIE_TX32+	B14	A14	PCIEx16_CLK_N	PCI-e reference clock lane - from module pin PCIE_REFCLK2-
PCI Express Transmit Pair 32-	PCIE_TX32-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX32+	PCI Express Receive Pair 32+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX32-	PCI Express Receive Pair 32-

Power Ground	GND	B18	A18	GND	Power Ground
PCI Express Transmit Pair 33+	PCIE_TX33+	B19	A19	RSVD	Not connected
PCI Express Transmit Pair 33-	PCIE_TX33-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX33+	PCI Express Receive Pair 33+
Power Ground	GND	B22	A22	PCIE_RX33-	PCI Express Receive Pair 33-
PCI Express Transmit Pair 34+	PCIE_TX34+	B23	A23	GND	Power Ground
PCI Express Transmit Pair 34-	PCIE_TX34-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX34+	PCI Express Receive Pair 34+
Power Ground	GND	B26	A26	PCIE_RX34-	PCI Express Receive Pair 34-
PCI Express Transmit Pair 35+	PCIE_TX35+	B27	A27	GND	Power Ground
PCI Express Transmit Pair 35-	PCIE_TX35-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX35+	PCI Express Receive Pair 35+
Not Connected	RSVD	B30	A30	PCIE_RX35-	PCI Express Receive Pair 35-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not connected
PCI Express Transmit Pair 36+	PCIE_TX36+	B33	A33	RSVD	Not connected
PCI Express Transmit Pair 36-	PCIE_TX36-	B34	A34	GND	Power Ground
Power Ground	GND	B35	A35	PCIE_RX36+	PCI Express Receive Pair 36+
Power Ground	GND	B36	A36	PCIE_RX36-	PCI Express Receive Pair 36-
PCI Express Transmit Pair 37+	PCIE_TX37+	B37	A37	GND	Power Ground
PCI Express Transmit Pair 37-	PCIE_TX37-	B38	A38	GND	Power Ground
Power Ground	GND	B39	A39	PCIE_RX37+	PCI Express Receive Pair 37+
Power Ground	GND	B40	A40	PCIE_RX37-	PCI Express Receive Pair 37-
PCI Express Transmit Pair 38+	PCIE_TX38+	B41	A41	GND	Power Ground
PCI Express Transmit Pair 38-	PCIE_TX38-	B42	A42	GND	Power Ground
Power Ground	GND	B43	A43	PCIE_RX38+	PCI Express Receive Pair 38+
Power Ground	GND	B44	A44	PCIE_RX38-	PCI Express Receive Pair 38-
PCI Express Transmit Pair 39+	PCIE_TX39+	B45	A45	GND	Power Ground

PCI Express Transmit Pair 39-	PCIE_TX39-	B46	A46	GND	Power Ground
Power Ground	GND	B47	A47	PCIE_RX39+	PCI Express Receive Pair 39+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B48	A48	PCIE_RX39-	PCI Express Receive Pair 39-
Power Ground	GND	B49	A49	GND	Power Ground
PCI Express Transmit Pair 40+	PCIE_TX40+	B50	A50	RSVD	Not connected
PCI Express Transmit Pair 40-	PCIE_TX40-	B51	A51	GND	Power Ground
Power Ground	GND	B52	A52	PCIE_RX40+	PCI Express Receive Pair 40+
Power Ground	GND	B53	A53	PCIE_RX40-	PCI Express Receive Pair 40-
PCI Express Transmit Pair 41+	PCIE_TX41+	B54	A54	GND	Power Ground
PCI Express Transmit Pair 41-	PCIE_TX41-	B55	A55	GND	Power Ground
Power Ground	GND	B56	A56	PCIE_RX41+	PCI Express Receive Pair 41+
Power Ground	GND	B57	A57	PCIE_RX41-	PCI Express Receive Pair 41-
PCI Express Transmit Pair 42+	PCIE_TX42+	B58	A58	GND	Power Ground
PCI Express Transmit Pair 42-	PCIE_TX42-	B59	A59	GND	Power Ground
Power Ground	GND	B60	A60	PCIE_RX42+	PCI Express Receive Pair 42+
Power Ground	GND	B61	A61	PCIE_RX42-	PCI Express Receive Pair 42-
PCI Express Transmit Pair 43+	PCIE_TX43+	B62	A62	GND	Power Ground
PCI Express Transmit Pair 43-	PCIE_TX43-	B63	A63	GND	Power Ground
Power Ground	GND	B64	A64	PCIE_RX43+	PCI Express Receive Pair 43+
Power Ground	GND	B65	A65	PCIE_RX43-	PCI Express Receive Pair 43-
PCI Express Transmit Pair 44+	PCIE_TX44+	B66	A66	GND	Power Ground
PCI Express Transmit Pair 44-	PCIE_TX44-	B67	A67	GND	Power Ground
Power Ground	GND	B68	A68	PCIE_RX44+	PCI Express Receive Pair 44+
Power Ground	GND	B69	A69	PCIE_RX44-	PCI Express Receive Pair 44-
PCI Express Transmit Pair 45+	PCIE_TX45+	B70	A70	GND	Power Ground
PCI Express Transmit Pair 45-	PCIE_TX45-	B71	A71	GND	Power Ground
Power Ground	GND	B72	A72	PCIE_RX45+	PCI Express Receive Pair 45+
Power Ground	GND	B73	A73	PCIE_RX45-	PCI Express Receive Pair 45-

PCI Express Transmit Pair 46+	PCIE_TX46+	B74	A74	GND	Power Ground
PCI Express Transmit Pair 46-	PCIE_TX46-	B75	A75	GND	Power Ground
Power Ground	GND	B76	A76	PCIE_RX46+	PCI Express Receive Pair 46+
Power Ground	GND	B77	A77	PCIE_RX46-	PCI Express Receive Pair 46-
PCI Express Transmit Pair 47+	PCIE_TX47+	B78	A78	GND	Power Ground
PCI Express Transmit Pair 47-	PCIE_TX47-	B79	A79	GND	Power Ground
Power Ground	GND	B80	A80	PCIE_RX47+	PCI Express Receive Pair 47+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B81	A81	PCIE_RX47-	PCI Express Receive Pair 47-
Not Connected	RSVD	B82	A82	GND	Power Ground

Please be aware that PCI-e management on the carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B81/B48/B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B81 or B48 or B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

3.3.3 eSPI Debug Connector

eSPI Connector – CN15			
Pin	**Signal**	**Pin**	**Signal**
1	eSPI_CLK	2	eSPI_RESET#
3	eSPI_ALERT1#	4	+1.8V_ALW
5	eSPI_IO_0	6	eSPI_ALERT0#
7	eSPI_IO_1	8	eSPI_CS1#
9	eSPI_IO_2		
11	eSPI_IO_3	12	GND
13	eSPI_CS0#	14	GND

The COM HPC® card edge connector share on the same pins both the LPC and the eSPI interface.

The signals of these pins are first of all carried directly to an internal dual row 6+7 pin header, type NELTRON p/n 2208SM-14G-E10-CR or equivalent, with the pinout shown in the table on the left.

The ALERTx# and CSx# signals, however, are shared with the BMC connector CN58 (see par. 25) and with the eSPI Dual UART controller necessary to implement COM #2 and COM #3 ports (see par. 11).

For this reason, four dedicated 3-way jumpers allow the redirection of the above mentioned signals, according to the tables below.

JP27 position	eSPI_ALERT#0 connected to
1-2	BMC Connector CN58
2-3	eSPI connector CN15

JP28 position	eSPI_CS#0 connected to
1-2	BMC connector CN58
2-3	eSPI connector CN15

JP29 position	eSPI_ALERT#1 connected to
1-2	eSPI Dual UART Controller
2-3	eSPI connector CN15

JP30 position	eSPI_CS#1 connected to
1-2	eSPI Dual UART Controller
2-3	eSPI connector CN15

3.3.4 COM ports #0 #1 internal pin Headers

COM HPC modules foresee a maximum of 2 Serial Ports with only Tx, Rx, RTS# and CTS# signals (UART #0 and UART #1).

COM #0 #1 ports internal pin Header – CN26			
Pin	**RS-232 mode**	**RS-422 mode**	**RS-485 mode**
1	COM0_RxD	COM0_Rx+	
2	COM1_RxD	COM1_Rx+	
3	COM0_TxD	COM0_Tx-	COM0_Rx-/COM0_Tx-
4	COM1_TxD	COM1_Tx-	COM1_Rx-/COM1_Tx-

5		GND	
7	COM0_RTS#	COM0_Tx+	COM0_Rx+/COM0_Tx+
8	COM1_RTS#	COM1_Tx+	COM1_Rx+/COM1_Tx+
9	COM0_CTS#	COM0_Rx-	
10	COM1_CTS#	COM1_Rx-	

These two COM ports are made externally accessible through two multistandard transceivers, which allow using them in RS-232, RS-422 or RS-485 mode. Related outputs are available on an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E06 or equivalent.

Selection of working mode is made using jumpers JP18 and JP19, which are standard pin headers, P2.54mm, 1x3 pin.

JP18 position	COM #0 Working Mode
1-2	RS-422
2-3	RS-232
NO jumper	RS-485

JP19 position	COM #1 Working Mode
1-2	RS-422
2-3	RS-232
NO jumper	RS-485

Please be aware that for proper RS-485 working, the RTS# signals must be used as a handshaking signal, i.e. it is used to control the data flow direction. When RTS# signal is driven low, then the RS-485 port is in receiving mode, when RTS# signal is driven high then the RS-485 port is in transmitting mode.

The UART Port #1, however, is shared (at TTL level) with the BMC connector CN58 (see par. 3.3.19).

For this reason, a dedicated 3-way jumpers allow the redirection of the above mentioned UART port, according to the table below.

JP37 position	UART port #1 connected to
1-2	COM #1 internal header CN26
2-3	BMC Connector CN58

3.3.5 COM ports #2 #3 internal pin Headers

Two other COM ports are realised on HC78 carrier board by using an eSPI Dual UART Controller, Fintek F81214E,

These two additional COM ports are made externally accessible through two multistandard transceivers, which allow using them in RS-232, RS-422 or RS-485 mode. Related outputs are available on an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E06 or equivalent.

COM #2 #3 ports internal pin Header – CN17			
Pin	**RS-232 mode**	**RS-422 mode**	**RS-485 mode**
1	COM2_RxD	COM2_Rx+	
2	COM3_RxD	COM3_Rx+	
3	COM2_TxD	COM2_Tx-	COM2_Rx-/COM2_Tx-
4	COM3_TxD	COM3_Tx-	COM3_Rx-/COM3_Tx-
5		GND	
7	COM2_RTS#	COM2_Tx+	COM2_Rx+/COM2_Tx+
8	COM3_RTS#	COM3_Tx+	COM3_Rx+/COM3_Tx+
9	COM2_CTS#	COM2_Rx-	
10	COM3_CTS#	COM3_Rx-	

Selection of working mode is made using jumpers JP5 and JP6, which are standard pin headers, P2.54mm, 1x3 pin.

According to the working mode selected via jumpers JP5 and JP6, the pinout of the connector is as described in the left table.

Please be aware that for proper RS-485 working, the RTS# signals must be used as a handshaking signal, i.e. it is used to control the data flow direction. When RTS# signal is driven low, then the RS-485 port is in receiving mode, when RTS# signal is driven high then the RS-485 port is in transmitting mode.

JP5 position	COM #2 Working Mode
1-2	RS-422
2-3	RS-232
NO jumper	RS-485

JP6 position	COM #3 Working Mode
1-2	RS-422
2-3	RS-232
NO jumper	RS-485

3.3.6 USB ports

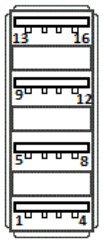
The HC78 Carrier board offers the possibility of using all the possible USB ports that are foreseen for COM HPC Client modules.

USB 2.0 ports #4#5#6#7 Quad Type-A socket - CN20			
Pin	Signal	Pin	Signal
1	$+5V_{USB4}$	5	$+5V_{USB5}$
2	USB4-	6	USB5-
3	USB4+	7	USB5+
4	GND	8	GND
9	$+5V_{USB6}$	13	$+5V_{USB7}$
10	USB6-	14	USB7-
11	USB6+	15	USB7+
12	GND	16	GND

Four USB 2.0 ports (#4, #5, #6 and #7) coming out from COM HPC® module can be used for the connection of external devices.

These four USB 2.0 ports are available on a standard quad Type-A receptacle socket.

The USB Port #7, however, is shared with the BMC connector CN58 (see par. 3.3.19).



For this reason, a dedicated 3-way jumpers allow the redirection of the above mentioned USB port, according to the table below.

JP26 position	USB port #7 connected to
1-2	BMC Connector CN58
2-3	Quad Type-A connector

USB Overcurrent header – CN55			
Pin	Signal	Pin	Signal
1	GND	2	USB_0_1_OC#
3	GND	4	USB_2_3_OC#
5	GND	6	USB_4_5_OC#
7	GND	8	USB_6_7_OC#

For debugging purposes, onboard it is also available an 8-pin connector CN63, type Adimpex p/n LE008208-R or equivalent, for testing of the overcurrent USB_x_y_OC# signals.

Two dedicated headers (CN79 and CN80) allow the programming of the two Power Delivery controllers mounted on the carrier board, each one associated to USB 4.0 / 3.2 Gen2x2 ports 0/1 or 2/3. These headers are not documented since they are reserved for manufacturing purpose.

Other than the USB 4 / 3.2 Gen2x2 ports available through the standard connectors CN75, CN76, CN77 and CN78,

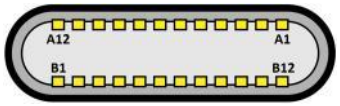
The four USB 4.0 / USB 3.2 Gen2x2 ports are all of them available on standard USB 4.0 Type-C sockets, CN75, CN76, CN77 and CN78, p/n Amphenol GSB4D313302Y1HR, all of them supporting Power Delivery functionality.

USB 4 / 3.2 Gen2x2 port#0 type C socket – CN75

Pin	Signal	Pin	Signal
A1	GND	B12	GND
A2	USBC0_Tx1+	B11	USBC0_Rx1+
A3	USBC0_Tx1-	B10	USBC0_Rx1-
A4	VBUS_C0	B9	VBUS_C0
A5	USBC0_CC1	B8	USBC0_SBU2
A6	USB0_D1+	B7	USB0_D2-
A7	USB0_D1-	B6	USB0_D2+
A8	USBC0_SBU1	B5	USBC0_CC2
A9	VBUS_C0	B4	VBUS_C0
A10	USBC0_Rx2-	B3	USBC0_Tx2-
A11	USBC0_Rx2+	B2	USBC0_Tx2+
A12	GND	B1	GND

USB 4 / 3.2 Gen2x2 port#1 type C socket – CN76

Pin	Signal	Pin	Signal
A1	GND	B12	GND
A2	USBC1_Tx1+	B11	USBC1_Rx1+
A3	USBC1_Tx1-	B10	USBC1_Rx1-
A4	VBUS_C1	B9	VBUS_C1
A5	USBC1_CC1	B8	USBC1_SBU2
A6	USB1_D1+	B7	USB1_D2-
A7	USB1_D1-	B6	USB1_D2+
A8	USBC1_SBU1	B5	USBC1_CC2
A9	VBUS_C1	B4	VBUS_C1
A10	USBC1_Rx2-	B3	USBC1_Tx2-
A11	USBC1_Rx2+	B2	USBC1_Tx2+
A12	GND	B1	GND



USB 4 / 3.2 Gen2x2 port#2 type C socket – CN77

Pin	Signal	Pin	Signal
A1	GND	B12	GND
A2	USBC2_Tx1+	B11	USBC2_Rx1+
A3	USBC2_Tx1-	B10	USBC2_Rx1-
A4	VBUS_C2	B9	VBUS_C2
A5	USBC2_CC1	B8	USBC2_SBU2
A6	USB2_D1+	B7	USB2_D2-
A7	USB2_D1-	B6	USB2_D2+
A8	USBC2_SBU1	B5	USBC2_CC2
A9	VBUS_C2	B4	VBUS_C2
A10	USBC2_Rx2-	B3	USBC2_Tx2-
A11	USBC2_Rx2+	B2	USBC2_Tx2+
A12	GND	B1	GND

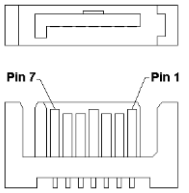
USB 4 / 3.2 Gen2x2 port#3 type C socket – CN78

Pin	Signal	Pin	Signal
A1	GND	B12	GND
A2	USBC3_Tx1+	B11	USBC3_Rx1+
A3	USBC3_Tx1-	B10	USBC3_Rx1-
A4	VBUS_C3	B9	VBUS_C3
A5	USBC3_CC1	B8	USBC3_SBU2
A6	USB3_D1+	B7	USB3_D2-
A7	USB3_D1-	B6	USB3_D2+
A8	USBC3_SBU1	B5	USBC3_CC2
A9	VBUS_C3	B4	VBUS_C3
A10	USBC3_Rx2-	B3	USBC3_Tx2-
A11	USBC3_Rx2+	B2	USBC3_Tx2+
A12	GND	B1	GND

3.3.7 SATA connectors

For the connection of external Mass Storage Devices, there are two standard male 7p SATA connectors, CN24 and CN25, type WINNING p/n WATM-07ABN4B2B8UW or equivalent.

These connectors carry out directly SATA#0 and SATA#1 signals coming from COM Express™ module's connector. Each SATA channel is composed by two differential pairs, SATA_TxX and SATA_RxX.



SATA M 7-p #0 #1 Connectors – CN24 andCN25	
Pin	Signal
1	GND
2	SATA_Tx0+ / SATA_Tx0+
3	SATA_Tx0- / SATA_Tx0-
4	GND
5	SATA_Rx0- / SATA_Rx1-
6	SATA_Rx0+ / SATA_Rx1+
7	GND

3.3.8 Front Panel Header

To allow the integration of a COM HPC® module based system inside a box PC-like, there is a connector on the carrier board that allows to remote signals for the Power Button (to be used to put the system in a Soft Off State, or awake from it), for the Reset Button, and the signal for optional LED signalling activity on SATA Channel and Power On states.

The pinout of this connector complies with Intel® Front Panel I/O connectivity Design Guide, Switch/LED Front Panel section, chapter 2.2.

Connector CN34 is an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E10 or equivalent.

3.3.9 Feature pin Header

Feature internal pin header – CN62			
Pin	Signal	Pin	Signal
1	+3.3V_ALW (with 1.5 resettable fuse)	2	+3.3V_RUN (with 1.5 resettable fuse)
3	SMB_CLK	4	I2C1_CLK
5	SMB_DAT	6	I2C1_DAT
7	SMB_ALERT#	8	I2C0_ALERT#
9	GND	10	I2C0_CLK
11	GP_SPI_MOSI	12	I2C0_DAT
13	GP_SPI_MISO	14	GND
15	GP_SPI_CS0#	16	BATLOW#
17	GP_SPI_CS1#	18	AC_PRESENT
19	GP_SPI_CS2#	20	VIN_PWR_OK
21	GP_SPI_CS3#	22	TEST#
23	GP_SPI_CLK	24	LID#
25	GP_SPI_ALERT#	26	RSTBTN#
27	GND	28	THERMTRIP#
29	BUF_SUS_S4_S5#	30	CARRIER_HOT#
31	BUF_SUS_S3#	32	RSMRST_OUT#
33	PWRBTN#	34	WD_OUT
35	SLEEP#	36	WAKE1#
37	TAMPER#	38	WD_STROBE#
39	GND	40	GND

For further expandability of the system, on board there is an expansion connector CN62, which carries out the signals related to I2C bus, SM Bus, General Purpose SPI, Watchdog and Power Management signals. These signals allow implementing, through external expansion modules, further functionalities that are not already realised by the carrier board.

For this purpose, it is available a dual row, 40 pin, P2.54mm standard pin header, type ADIMPEX p/n LE008240-R or equivalent, with the pinout shown in the table on the left.

All the signals available on this connector come out directly from the COM HPC® connector.

3.3.10 External BIOS SPI Flash header

External BIOS Boot SPI header – CN28			
Pin	Signal	Pin	Signal
1	BOOT_SPI_CS#	8	VCC_BOOT_SPI
2	BOOT_SPI_IO1 (MISO)	7	BOOT_SPI_IO3 (HOLD#)
3	BOOT_SPI_IO2 (WP#)	6	BOOT_SPI_CLK
4	GND	5	BOOT_SPI_IO0 (MOSI)

In case that an external Flash is needed, then on the carrier board it is provided a 8-pin header, p=1.27mm, type TOWNES p/n P1035-2*04MGF-084-D, for the external connection of SPI Flash devices

JP20 position	JP8 position	JP7 position	BIOS Boot Device
Not inserted	Not inserted	Not inserted	SPI Flash on Module
Not inserted	Not inserted	Inserted	Carrier' Boot SPI
Not inserted	Inserted	Not inserted	SPI Flash on Module
Not inserted	Inserted	Inserted	Reserved
Inserted	Not inserted	Not inserted	SPI Flash on Module
Inserted	Not inserted	Inserted	eSPI on BMC Module
Inserted	Inserted	Not inserted	SPI Flash on Module
Inserted	Inserted	Inserted	Reserved

According to COM HPC® Specifications, there are three jumpers on board, JP7 JP8 and JP20, which allow configuring the BSEL[0..2]# signals according to the table below, which is used by the COM HPC Client module to select the BIOS Boot device. More options are possible for boot from SPI Flash on module. Most common usage, however, is the first one, i.e. with JP20, JP7 and JP8 not placed. Please refer to module's User manual to see if different settings on BSEL[0..2] shall be applied.

3.3.11 GPIO pin header

GPIO pin header – CN31			
Pin	Signal	Pin	Signal
1	+3.3V_ALW (with 1.5A resettable fuse)	2	GPIO_00
3	GPIO_01	4	GPIO_02
5	GPIO_03	6	GPIO_04
7	GPIO_05	8	GPIO_06
9	GPIO_07	10	GPIO_08
11	GPIO_09	12	GPIO_10
13	GPIO_11	14	GND

COM HPC® specifications foresee up to 12 GPIOs coming out from the client module.
To deploy them, on HC78 carrier board these signals are carried out to an external dual row 14 pin, P2.54mm standard pin header, with the pinout shown in the table on the left.

GPIO_10 and GPIO_11 signals, however, are shared with the BMC connector CN58 (see par. 3.3.19).

For this reason, two dedicated 3-way jumpers allow the redirection of the above mentioned GPIO signals, according to the tables below.

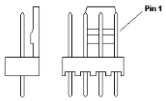
JP38 position	GPIO_10 connected to
1-2	BMC Connector CN58
2-3	GPIO Pin header CN31

JP39 position	GPIO_11 connected to
1-2	BMC Connector CN58
2-3	GPIO Pin header CN31

3.3.12 FAN Connector

FAN Connector – CN32	
Pin	Signal
1	GND
2	FAN_PWR
3	FAN_TACH_IN
4	FAN_PWM

Onboard it is available a 4-pin connector, type MOLEX p/n 47053-3000 or equivalent, for the connection of tachometric FANs.



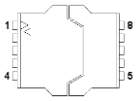
JP9 position	FAN driver mode selector
1-2	4-Wires Fan
2-3	3-Wires Fan

By using a dedicate jumper JP9, it is possible to select if FAN_PWR is fixed to +12V_RUN, in order to support 4-wire tachometric fans, or must be controlled by the signal FAN_PWMOUT, coming directly from COM HPC® module, in order to support 3-wire tachometric fans.

3.3.13 External EEPROM I2C Flash socket

External EEPROM I2C Flash socket – CN35			
Pin	Signal	Pin	Signal
1	4.7kΩ pull-up +3.3V_ALW	5	I2C0_DAT
2	4.7kΩ pull-up +3.3V_ALW	6	I2C0_CLK
3	4.7kΩ pull-up +3.3V_ALW	7	I2C_Write Protect
4	GND	8	+3.3V_ALW

The I2C0 bus coming from COM HPC® module is carried directly to Feature pin Header (see par. 3.3.9) and to the BMC Connector (see par. 3.3.19).
It is also used to manage an SO8 EEPROM Socket CN62, type LOTES p/n ASPI0001-P001A, for plugging I2C Flash in SO-8 format.
The I2C_Write Protect function is disabled for this board.



3.3.14 Audio Section

According to COM HPC® specifications, client modules can offer two dedicated SoundWire audio interface and an I2S audio interface.

Triple Audio Jack – CN63	
Colour	Signal
Light Blue	Line IN (Left + Right)
Light Green	Front_OUT (Left + Right)
Pink	MIC1 IN (Left + Right)

For this reason, interfaced to the I2S Audio Interface, on the carrier board there is an I2S Audio Codec, type Texas Instruments TLV320AIC23B ALC888s, which manages a standard Stereo triple jack connector, type LOTES ABA-JAK-028-K07 (light blue/light green/pink) or equivalent.

Front panel Audio header – CN38			
Pin	Signal	Pin	Signal
1	Mic2_In_L	2	Audio_GND
3	Mic2_In_R	4	---
5	Line_Out_R	6	Mic2_Sense_Return
7	Audio_GND		
9	Line_Out_L	10	Line_Out_Sense_Return

Furthermore, it is also available a dedicated 9-pin 2.54mm pitch Pin header for external connection of a Line Out output and a second Mic In input.

Pinout hereby shown is compliant to "Intel® Front Panel I/O connectivity Design Guide" specifications, par. 2.3.5 Table 7.

Using this dedicated connector, it will be possible to connect any Azalia compliant panel audio jack to remote audio connectors in the preferred position

Alternatively, it is also possible to use SECO's dedicated front panel module, which offers two standard audio jacks, two pushbuttons (for reset and power on) and two LEDs, for SATA activity and Power status signalling (to be used in conjunction to the Front Panel header described at par. 3.3.8).

SoundWire and I2S header – CN64			
Pin	Signal	Pin	Signal
1	+1.8V_RUN	2	I2S_CLK/SNDW_CLK2
3	SNDW_DMIC_CLK1	4	I2S_DIN/SNDW_DAT2
5	SNDW_DMIC_DAT1	6	I2S_LRCLK/SNDW_CLK3
7	SNDW_DMIC_CLK0	8	I2S_DOUT/SNDW_DAT3
9	SNDW_DMIC_DAT0	10	GND

It is also possible to connect external I2S or SoundWire devices by using the dedicated connector CN64, which carries out the 2x SoundWire and the shared I2S/Soundwire interface coming from COM HPC® client module.
CN64 is a dual row 10 pin, P2.54mm standard pin header, with the pinout shown in the table on the left.

3.3.15 eDP Connector

eDP connector – CN42			
Pin	Signal	Pin	Signal
1	PTN_PWR	21	VDD_LCD
2	VDD_BKLT	22	VDD_LCD
3	VDD_BKLT	23	VDD_LCD
4	VDD_BKLT	24	GND
5	VDD_BKLT	25	eDP_AUX-
6	PTN_SMB_CLK	26	eDP_AUX+
7	PTN_SMB_DAT	27	GND
8	LCD_BKLT_CTRL	28	eDP_TX0+
9	LCD_BKLT_EN	29	eDP_TX0-
10	GND	30	GND
11	GND	31	eDP_TX1+
12	GND	32	eDP_TX1-
13	GND	33	GND
14	eDP_HPD	34	eDP_TX2+
15	GND	35	eDP_TX2-
16	GND	36	GND
17	GND	37	eDP_TX3+
18	GND	38	eDP_TX3-
19	N.C.	39	GND
20	VDD_LCD	40	---

The HC78 carrier board offers the possibility of managing external eDP or mipi_DSI Displays.

For the connection of this kind of displays, on-board there is a VESA® certified connectors for embedded Display Port interface, type STARCONN p/n 300E40-0110RA-G3 or equivalent (microcoaxial cable connector, 0.5mm pitch, 40 positions).

On this connector, VDD_BKLT and VDD_LCD are the voltage rails that can be used to supply the LCD and related Backlight Unit.

This connector allows also to connect external eDP-to-LVDS adaptors, by offering a dedicated power rail (PTN_PWR) and SM Bus interface (PTN_SMB_CLK and PTN_SMB_DAT). These signals can be made externally available by using dedicated jumper JP11, according to the table below.

JP11 position	eDP additional signals selector
Inserted	eDP only
Not inserted	eDP additional signal enabled

VDD_LCD: LCD Voltage rail. Its value can be set to +3.3V_RUN or +5V_RUN by using dedicated jumper JP13, which is a standard pin header, P2.54mm, 1x3 pin.

VDD_BKLT: Backlight Voltage rail. Its value can be set to +5V_RUN or +12V_RUN by using dedicated jumper JP12, same of JP13.

JP13 position	LCD Power selector
1-2	+5V_RUN
2-3	+3.3V_RUN

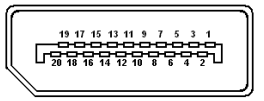
JP12 position	Backlight Power selector
1-2	+12V_RUN
2-3	+5V_RUN

3.3.16 DP++ Connectors

Multimode DP Connectors – CN52, CN53, CN54			
Pin	Signal	Pin	Signal
1	DDI*X*_PAIR0+	2	GND
3	DDI*X*_PAIR0-	4	DDI*X*_PAIR1+
5	GND	6	DDI*X*_PAIR1-
7	DDI*X*_PAIR2+	8	GND
9	DDI*X*_PAIR2-	10	DDI*X*_PAIR3+
11	GND	12	DDI*X*_PAIR3-
13	DDI*X*_DDC_AUX_SEL	14	DDI*X*_CEC
15	DDI*X*_SCL_AUX+	16	GND
17	DDI*X*_SDA_AUX-	18	DDI*X*_HPD
19	GND	20	+3.3V_RUN

According to COM HPC® specifications, client modules pinout defines three Digital Display interfaces (DDI), that can be used to carry out DisplayPort and TMDS (HDMI/DVI) interface.

On HC78 Carrier board, these interfaces (DDI0, DDI1 and DDI2) are carried to as many standard DisplayPort Connectors, CN52,CN53 and CN54, type WINNING p/n WDPE-20F3L1BU3 or equivalent, with the pinout shown in the following table.



All these interfaces support DP++, so it is possible to connect also HDMI and DVI displays by using external adapters.

Please be aware that the CEC signals are connected on the connectors, but they are fixed low through a 5.1MOhm resistor, since this signal is not managed by the COM HPC® client modules.

3.3.17 POST Code Display

For debugging purposes, it is available a display made by 2x 7-segment LED display, type Kingbright KCSC02-105 or equivalent.

The management of this display is done using an NXP PCA9535PW I/O expander, driven through the COM HPC® dedicated USB PD I2C Bus.

3.3.18 Buttons

On the carrier board, there are four momentary pushbuttons (with contacts normally open) for the direct handling of COM HPC® power management signals.

The first pushbutton, M1, is placed on RSTBTN# signal. Upon the pressure of this pushbutton, the COM HPC® Client module will perform a reset.

The second pushbutton, M2, is placed on PWRBTN# signal. Upon the pressure of this pushbutton, the COM HPC® Client module will perform a power up / power down sequence.

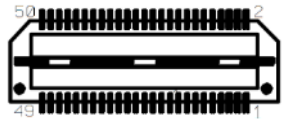
The third pushbutton, M3, is placed on LID# signal. Such a signal can be used by the COM HPC® Client module to detect the opening / the closure of an external lid switch, like those used to detect opening / closure of the notebooks. Upon changes in LID # state, the OS could trigger the transition of the module from Working to Sleep status, or vice versa.

The fourth pushbutton, M4, is placed on SLEEP# signal. Upon the pressure of this pushbutton, the COM HPC® Client module will enter in a sleep state.

3.3.19 BMC Connector

BMC connector – CN58			
Pin	Signal	Pin	Signal
1	+5V_ALW	2	+3.3V_ALW
3	+5V_ALW	4	+3.3V_ALW
5	+5V_ALW	6	+3.3V_ALW
7	---	8	GND
9	GND	10	eSPI_CLK
11	IPMB_CLK	12	eSPI_RST#
13	IPMB_DAT	14	eSPI_ALERT0#
15	GND	16	eSPI_IO_0
17	I2C0_CLK	18	eSPI_IO_1
19	I2C0_DAT	20	eSPI_IO_2
21	GND	22	eSPI_IO_3
23	USB7+	24	eSPI_CS0#
25	USB7-	26	GND
27	GND	28	PCIE_BMC_CLK-
29	PWRBTN#	30	PCIE_BMC_CLK+
31	RSTBTN#	32	GND
33	BUF_SUS_S3#	34	BMC_CLK_REQ#
35	BUF_SUS_S4_S5#	36	PCIE_BMC_RST#
37	VIN_PWR_OK	38	GND
39	WAK0E#	40	PCIE_BMC_RX+
41	UART_TX1	42	PCIE_BMC_RX-
43	UART_RX1	44	GND
45	GPIO_10	46	PCIE_BMC_TX+
47	GPIO_11	48	PCIE_BMC_TX-
49	GND	50	GND

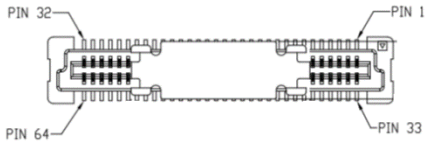
COM HPC HC78 Carrier Board expands its functionalities by means of BMC connector CN58, to be used for plugging Baseboard Management Controller (BMC) modules.
This connector includes multiple interfaces, SM Bus, I2C, LPC, 1x USB 2.0, 1x PCI-e x1, NCSI signals.
CN58, type SAMTEC QStrip® p/n QTS-025-01-L-D-A with the pinout on left table.
Many interfaces available on this connector are also shared with other connectors. In these cases, a dedicated jumper allows the redirection of the specific interface to the BMC connector or to the other one. Please check par. Errore. L'origine riferimento non è stata trovata. (JP27 and JP28), par. 3.3.4 (JP37), par.3.3.6 (JP26) and par. 3.3.11 (JP38 and JP39), These interfaces are highlighted in red in the table on the left.



3.3.20 Networking

10GbE OCP Type-C Connector – CN82			
Pin	Signal	Pin	Signal
1	SMB_CLK	33	+VIN_OCP
2	SMB_DAT	34	+VIN_OCP
3	EXT_MDIO_I2C_SEL	35	+VIN_OCP
4	GND	36	ETH0_1_PHY_RST#
5	N.C:	37	ETH_KR0_INT
6	N.C:	38	ETH_KR1_INT
7	GND	39	GND
8	N.C:	40	ETH0_TX+
9	10G_LED1_0#	41	ETH0_TX-
10	GND	42	GND
11	N.C:	43	N.C:
12	N.C:	44	10G_LED0_0#
13	GND	45	GND
14	N.C:	46	ETH1_TX+
15	N.C:	47	ETH1_TX-
16	GND	48	GND
17	N.C:	49	ETH0-1_MDIO_CLK
18	N.C:	50	ETH0-1_MDIO_DAT
19	GND	51	GND
20	ETH0_I2C_CLK	52	ETH0_RX+
21	ETH0_I2C_DAT	53	ETH0_RX-
22	GND	54	GND
23	N.C:	55	N.C:
24	N.C:	56	N.C:
25	GND	57	GND
26	ETH1_I2C_CLK	58	ETH1_RX+
27	ETH1_I2C_DAT	59	ETH1_RX-
28	GND	60	GND
29	N.C:	61	N.C:
30	N.C:	62	N.C:
31	N.C:	63	GND
32	N.C:	64	N.C:

COM HPC® client modules can manage up to two Ethernet KR interfaces, where the MAC is located on the module and the PHY is located on the carrier.
To make HC78 Carrier board more flexible, the PHYs are not directly implemented in the carrier board. The signals necessary for their management, instead, are carried to an OCP Type-C connector CN82, i.e. a board-to-board connector type AMPHENOL P/N 10135583-641402LF.



JP40 position	OCP Module presence
Inserted	OCP module plugged
Not inserted	OCP module not plugged

On HC78 Carrier bord, the 2-way jumper must be used to signal to the client module (through the signal ETH0-1_PSNT#) when an OCP module is plugged on CN82 connector.

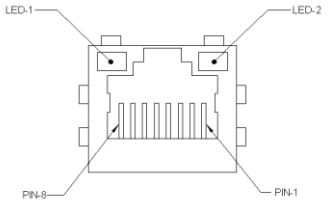
JP25 position	Ethernet KR PHY Mode
1-2	MDIO
2-3	I2C/MDIO

The HC78 Carrier Board is also equipped with a 3-way jumper, JP25, which indicate if the PHY for Ethernet KR lanes can be configured only via MDIO or if I2C/MDIO is supported.
This jumper acts directly on signal EXT_MDIO_I2C_SEL of connector CN82

RJ45 NBase-T Ethernet #0 Connector- CN68			
Pin	Signal	Pin	Signal
1	NBASET0_MDI0+	5	NBASET0_MDI2-
2	NBASET0_MDI0-	6	NBASET0_MDI1-
3	NBASET0_MDI1+	7	NBASET0_MDI3+
4	NBASET0_MDI2+	8	NBASET0_MDI3-

RJ45 NBase-T Ethernet #1 Connector- CN65			
Pin	Signal	Pin	Signal
1	NBASET1_MDI0+	5	NBASET1_MDI2-
2	NBASET1_MDI0-	6	NBASET1_MDI1-
3	NBASET1_MDI1+	7	NBASET1_MDI3+
4	NBASET1_MDI2+	8	NBASET1_MDI3-

COM HPC client modules offer two Nbase-T Ethernet interface, including MAC and PHY. Only the isolation magnetic (with a 1:1 turn ratio) is required.
On the carrier board, therefore, there are two dedicated RJ-45 connectors, CN65 and CN68, with integrated magnetic, also including Activity and Link LEDs, type CTK P/N K3T14-153-01 or equivalent.



Reserved / FuSa Header

Reserved / FuSa Header – CN71			
Pin	Signal	Pin	Signal
1	+5V_ALW (with 1.5A resettable fuse)	2	+12V_RUN (with 1.5A resettable fuse)
3	GND	4	GND
5	RSVD_F1	6	RSVD_F2
7	RSVD_F3	8	RSVD_F4
9	RSVD_F5	10	RSVD_F6
11	RSVD_F7	12	RSVD_F8
13	RSVD_F9	14	RSVD_F10
15	RSVD_F11	16	RSVD_F12
17	RSVD_F13	18	RSVD_F14
19	RSVD_F15	20	RSVD_F16
21	RSVD_F17	22	RSVD_F18
23	RSVD_F84	24	RSVD_F95
25	RSVD_F83	26	RSTBTN#
27	PS_ON#	28	PWRBTN#

According to COM HPC® Specifications, the COM HPC® client module connectors provide additional reserved signals intended to be used for future uses.

On HC78 Carrier Board, these signals are carried out to a dual row, 28 pin, P2.54mm standard pin header, type ADIMPEX p/n LE008228-R, with the pinout shown in the table on the left.

This connector is used to provide functional safety functions for FuSa applications through signals listed in left table.

Please be aware that FuSa functionality can be obtained only in case that it is supported by the COM HPC® module plugged onto the Carrier Board.

Please refer to specific COM HPC® client module for a signal description related to this section.

3.3.21 CSI Camera Connectors

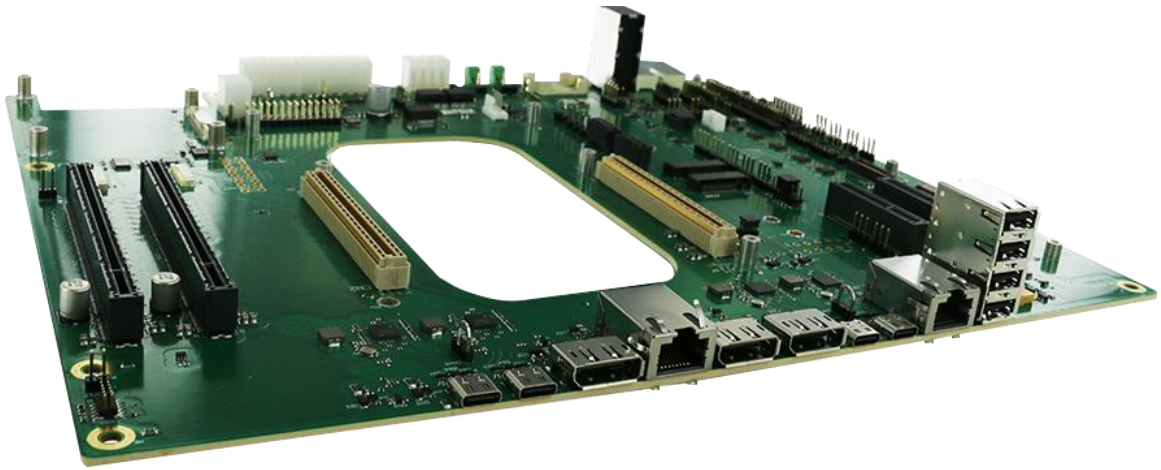
CSI CAMERA CONNECTOR #0 – CN60			
Pin	Signal	Pin	Signal
1	+3.3V_RUN	12	CSI0_RST#
2	+3.3V_RUN	13	CSI0_RX3+
3	GND	14	CSI0_RX3-
4	CSI0_RX0+	15	GND
5	CSI0_RX0-	16	CSI0_CLK+
6	GND	17	CSI0_CLK-
7	CSI0_RX1+	18	GND
8	CSI0_RX1-	19	CSI0_I2C_CLK
9	GND	20	CSI0_I2C_DAT
10	CSI0_RX2+	21	CSI0_ENA
11	CSI0_RX2-	22	CSI0_MCLK

CSI CAMERA CONNECTOR #1 – CN61			
Pin	Signal	Pin	Signal
1	+3.3V_RUN	12	CSI1_RST#
2	+3.3V_RUN	13	CSI1_RX3+
3	GND	14	CSI1_RX3-
4	CSI1_RX0+	15	GND
5	CSI1_RX0-	16	CSI1_CLK+
6	GND	17	CSI1_CLK-
7	CSI1_RX1+	18	GND
8	CSI1_RX1-	19	CSI1_I2C_CLK
9	GND	20	CSI1_I2C_DAT
10	CSI1_RX2+	21	CSI1_ENA
11	CSI1_RX2-	22	CSI1_MCLK

Since SMARC modules can offer up to two CSI camera interfaces, they are made available, without further signal conditioning, on two dedicated 22-pin FPC connectors, type TE p/n 2-1734592-2, with the pinout shown in the table on the left

Chapter 4.
Appendices

- Thermal Design
- Accessories



4.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like COM HPC™ modules, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

COM HPC™ specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the COM HPC™ module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsinks in some situation can represent a cooling solution. Until the modules are used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with fan could be sufficient for modules' cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat.

Indeed, when using CCHPC-C78-C carrier board with any COM HPC™ module, it is necessary to consider carefully the global heat generated by the system, and the scenario of utilisation.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide COM HPC™ modules' specific heatspreaders and heatsinks (active and passive), but please remember that their use must be evaluated accurately inside the final system (electronics + mechanics), and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions, which also keeps the surface temperature of all carrier board's components in the temperature range specified for the specific carrier board configuration (commercial grade).

4.2 Accessories

The CCHPC-C78-C Carrier Board will not be sold alone, but as a part of a more comprehensive Development kit

The full development kit is coded as COM HPC CLIENT DEV KIT and does contain:

- Carrier board for COM HPC® Client compliant modules CCHPC-C78-C
- 1 x DB-9 Serial cable adapter
- Front Panel Board with connecting cable (CV-837/30 and CV-836/30)
- SATA 7p Data cable

A more detailed description can be found at related product page in Seco S.p.A website:

COM-HPC CLIENT DEV KIT - Cross Platform Development Kit compatible with both x86 and ARM COM-HPC Client modules | SECO