SBC

User Manual

ADLER

(formerly codename SBC-C41-pITX)

Single Board Computer
with Intel® Atom™ X Series, Intel® Celeron® J / N Series, Intel® Pentium® N Series (formerly Apollo Lake) Processors on picoITX form factor

HDMI™
HIGH-DEFINITION MULTIMEDIA INTERFACE

www.seco.com

REVISION HISTORY

Revision	Date	Note	Ref
1.0	28th January 2020	First Official Release.	AR / SB
1.1	30th January 2020	Power jack CN2 updated	AR / SB
1.2	2nd December 2021	Declaration of rights updated Trademark Notice (par. 1.7.1) added BIOS documentation updated to Ver. 1.15	SO
1.3	25th March 2022	Minor errors corrected Commercial name updated	SB

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

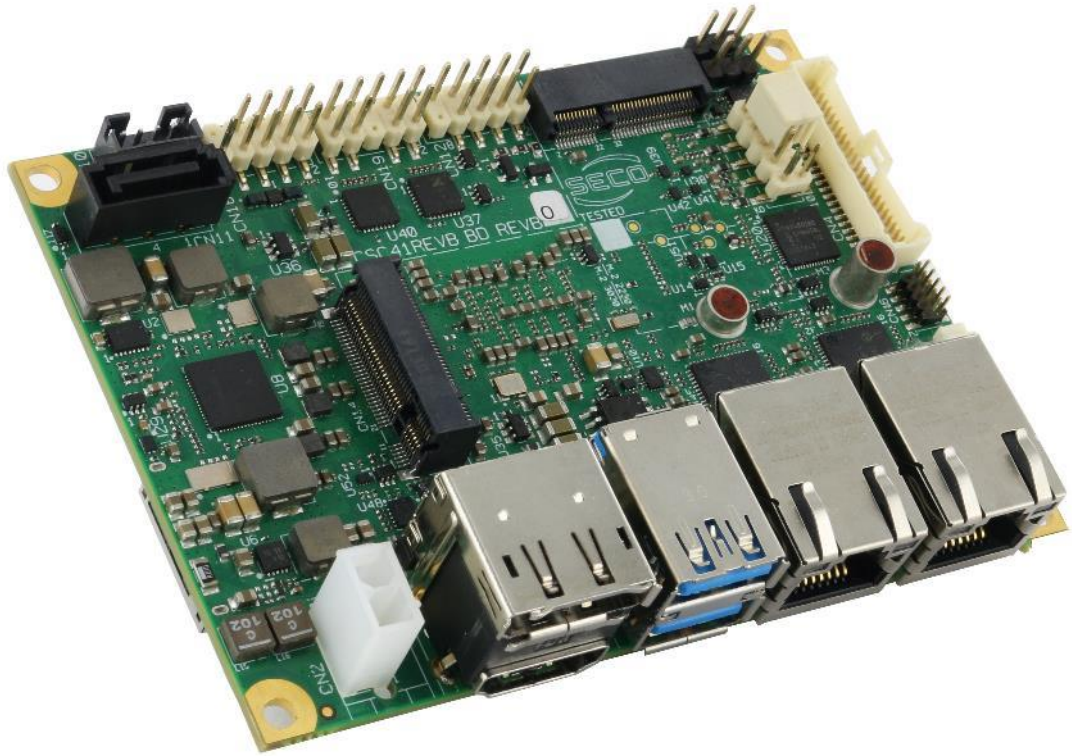
For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

INDEX

Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorized by the supplier.

The authorization is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorization number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above mentioned requirements for the RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionalities and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The ADLER board uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic discharges

The ADLER board, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling a ADLER board, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The ADLER board is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
EHCI	Enhanced Host Controller interface, a high-speed controller for USB ports, able to support USB2.0 standard
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI™	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
LPDDR4	Low Power DDR, 4th generation
LVDS	Low Voltage Differential Signaling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenCL	Open Computing Language, a software library based on C99 programming language, conceived explicitly to realise parallel computing using Graphics Processing Units (GPU)
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics

OS	Operating System
PCI-e	Peripheral Component Interface Express
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
PXE	Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS
SATA	Serial Advance Technology Attachment, a differential full duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDHC	Secure Digital Host Controller
SIM	Subscriber Identity Module, a card which stores all data of the owner necessary to allow him accessing to mobile communication networks
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signaling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
UIM	User Identity Module, an extension of SIM modules.
USB	Universal Serial Bus
V_REF	Voltage reference Pin
xHCI	eXtensible Host Controller Interface, Host controller for USB 3.0 ports, which can also manage USB 2.0 and USB1.1 ports

1.7.1 Trademark Notice

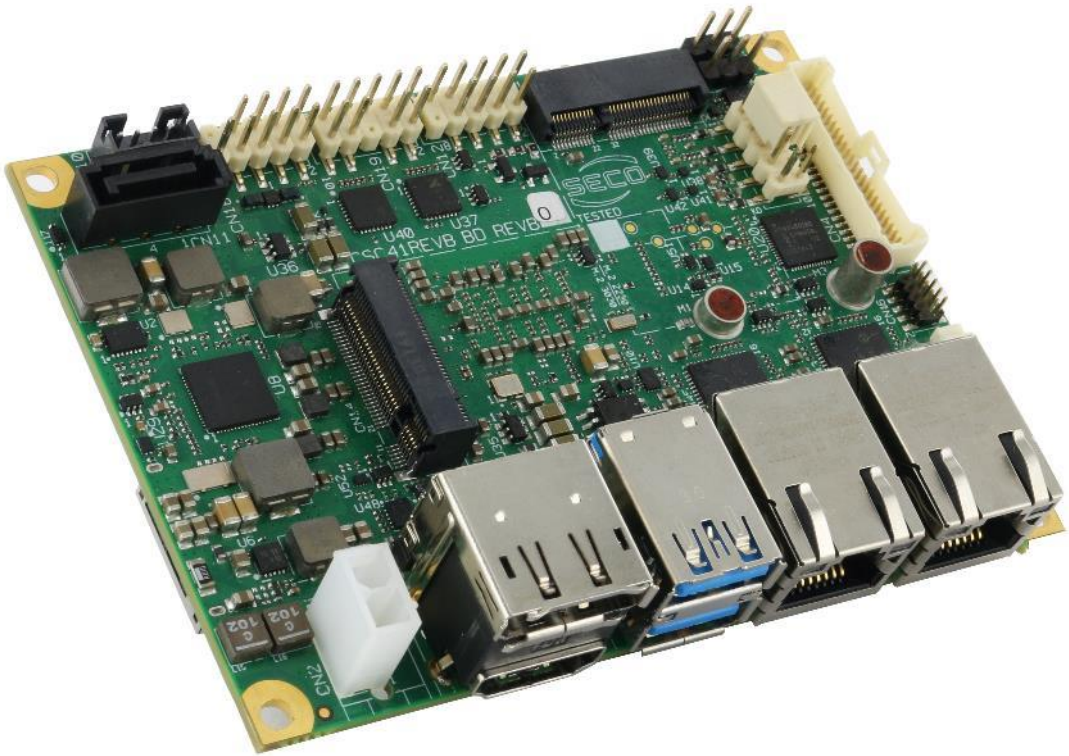
1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	https://uefi.org/specifications
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
DDC	http://www.vesa.org
Gigabit Ethernet	https://standards.ieee.org/standard/802_3-2018.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	https://www.nxp.com/docs/en/user-guide/UM10204.pdf
Intel® Front Panel I/O connectivity DG	Intel Technical Library
LVDS	http://www.ti.com/lit/ug/snla187/snla187.pdf
M.2	http://www.pcisig.com/specifications/pciexpress
MMC/eMMC	https://www.jedec.org/committees/jc-64
OpenCL	http://www.khronos.org/opencl
OpenGL	http://www.opengl.org
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SD Card Association	https://www.sdcard.org
SM Bus	http://www.smbus.org/specs
TMDS	https://www.cablestogo.com/learning/library/digital-signage/intro-to-tmds
UEFI	http://www.uefi.org
USB 2.0 and USB OTG	https://www.usb.org/sites/default/files/usb_20_20190524.zip
USB 3.0	https://usb.org.10-1-108-210.causewaynow.com/sites/default/files/usb_32_20191024.zip
Intel® Atom™ Apollo Lake family	https://ark.intel.com/content/www/us/en/ark/products/codename/80644/apollo-lake.html#@Embedded

Chapter 2.
OVERVIEW

- Introduction
- Technical specifications
- Electrical specifications
- Mechanical specifications
- Block diagram



2.1 Introduction

ADLER is a Single Board Computer in pico-ITX form factor (just 100 x 72mm) based on the Intel® Atom™ X Series, Intel® Celeron® J/N Series and Intel® Pentium® N Series family of System-on-Chips (SOCs) formerly coded as Apollo Lake, a series of Dual / Quad Core SOCs with 64-bit instruction set.

These SOCs embed all the features usually obtained by combination of CPU + platform Controller hubs, all in one single IC, which allows, therefore, the system minimisation and performance optimisation, which is essential for boards with sizes so reduced as for picoITX SBCs, which offers all functionalities of standard PC boards in just 100x72mm.

This single chip solution includes the memory controller, which gives support for up 32-bit Single-/Dual-/Quad-Channel LPDDR4 2400 MT/s Memory.

All SOCs embed an Integrated Intel® HD Graphics 500 series controller with up to 18 Execution Units, which offer high graphical performances, with support for Microsoft® DirectX12, OpenGL 4.3, OpenCL 1.2, OpenGLES 3.0 and HW acceleration for video encoding and decoding of HEVC (H.265), H.264, JPEG/MJPEG. It is also possible the HW video decoding only of VP9, MPEG2, VC-1 and WMV9. This embedded GPU can drive three independent displays, by using HDMI, LVDS and DP++ interfaces. Any combinations of these video interfaces are supported.

Mass Storage capabilities of the board include two external S-ATA Gen3 channels (one available on a standard SATA 7p Male connector, the other on an M.2 Socket 2 Key B Slot, a standard 4-bit SD interface and one optional eMMC Drive soldered on board.

Further features usable on ADLER board are WWAN M.2 Socket 2 Key B Slot connected to a miniSIM slot for modems, four USB ports (two USB 3.0 and two USB 2.0 only), HD Audio, up to 2x Gigabit Ethernet connections, one M.2 Socket 1 Key E Slot for WiFi+BT M.2 modules.

The board is available both in commercial and in industrial temperature range.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

2.2 Technical specifications

SOC

Intel® Atom™ x7-E3950, Quad Core @1.6GHz, 2MB L2 Cache, 12W TDP
Intel® Atom™ x5-E3940, Quad Core @1.6GHz, 2MB L2 Cache, 9.5W TDP
Intel® Atom™ x5-E3930, Dual Core @1.3GHz, 2MB L2Cache, 6.5W TDP
Intel® Pentium® N4200, Quad Core @1.1GHz, 2MB L2 Cache, 6W TDP
Intel® Celeron® N3350, Dual Core @1.1GHz, 2MB L2Cache, 6W TDP
Intel® Celeron® J3455, Quad Core @1.5GHz, 2MB L2Cache, 10W TDP
Intel® Celeron® J3355, Dual Core @2.0GHz, 2MB L2Cache, 10W TDP

Memory

32-bit Single-/Dual-/Quad-Channel LPDDR4 soldered onboard, up to 2400 MT/s
Max memory size 8GB

Graphics

Integrated Intel® HD Graphics 500 series controller with up to 18 Execution Units
Three independent display support
HW decoding of HEVC(H.265), H.264, MVC , VP8, VP9, MPEG2, VC-1, WMV9, JPEG/MJPEG formats
HW encoding of HEVC(H.265), H.264, MVC, VP8, VP9 and JPEG/MPEG formats

Video Interfaces

HDMI connector
Optional DP++ connector (combo with HDMI)
LVDS connector

Video Resolution

HDMI, support 4Kx2K without HDCP @ 30Hz as specified in HDMI 1.4b
LVDS, resolution up to 1920x1200 @ 60Hz
DP++, resolution up to 4096x2160 @ 60Hz

Mass Storage

Optional eMMC 5.0 drive on-board
SATA Gen3 7p M connector
SSD M.2 Socket 2 Key B lot, size 2242 / 3042 (excludes WWAN modules)
microSD Card slot (combo with miniSIM slot)

Networking

2x Gigabit Ethernet connector
WWAN (modem) M.2 Socket 2 Key B 2242 / 3042 slot (excludes SSD interface)
Connectivity M.2 Socket 1 Key E 2230 Slot for WiFi+BTLE modules

USB

USB 3.0 Dual Type-A connector
Internal USB 2.0 Dual pin header

Audio

HD Audio Codec
Line Out + Microphone + S/PDIF Out interfaces on internal pin header

Serial Ports

2 x RS-232/RS-422/RS-485 Serial ports on internal pin header

Other Interfaces

miniSIM slot for M.2 modems (combo with microSD slot)
8 x GPI/Os connector
FAN connector
Switch / LED Front Header connector
I2C + INT# + RST# signals for I2C Touch Screen controller on LVDS connector
Optional TPM 2.0 on-board

Power supply voltage: +12V_{DC} ± 5%
Cabled coin cell battery for RTC

Operating temperature **:

0°C ÷ +60°C (Commercial temperature)
-40° ÷ +85°C (Industrial temperature)

Dimensions: 72 x 100 mm (2.83” x 3.93”).

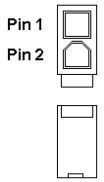
Supported Operating Systems:

Microsoft® Windows® 10 Enterprise (64 bit)
Microsoft® Windows® 10 IoT Core (32- /64-bit)
Linux 64-bit
Yocto (64-bit)

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated. Please also check paragraph 5.1*

2.3 Electrical specifications

ADLER needs to be supplied only with an external $12V_{DC}$ ± 5% power supply. It is possible to supply the module by using two different power connectors (factory alternatives)

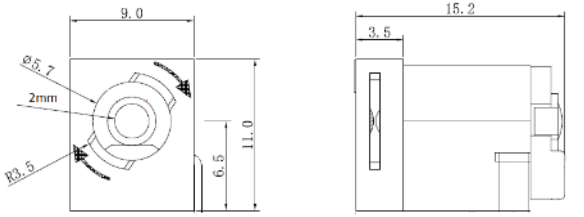


Mini-Fit Power Connector – CN1	
Pin	**Signal**
1	GND
2	V_{IN}

The first possible power connector is type Molex Mini-Fit connector, type MOLEX p/n 39-28-1023 or equivalent.

The pin-out is indicated in the table here on the left, and the mating connector is MOLEX p/n 39-01-2020 or equivalent with crimp terminals series 5556/44476.

As an alternative, the VIN voltage can be supplied through a standard 5.7mm (internal pin, diameter 2.0 mm) Power Jack CN2.



Internal pin is VIN power line.

2.3.1 Power available

When powering ADLER with a PSU with characteristics greater or equal to the one described at beginning of previous paragraph, please consider well what is the typical scenario for using the board (i.e., which peripherals will be connected)

Internal power section is able to supply a maximum of 8A@5V for external devices supplied directly by the module (i.e. USB devices, optionally SSD or SATA disks, display).

Consider that each USB 2.0 port requires 500mA, and USB 3.0 ports need 0.9A each, so if all 5 USB ports are used, then the 5V power section would be able to supply further 4.7A (about 24W) to other peripherals, like SATA Disk and/or LVDS display. Anyway, if all this current is needed by external peripherals, a 40W PSU cannot supply further power for internal circuitry of the board.

Since all the power must be supplied by an external PSU only, please balance well the typical final configuration, considering both the power consumption of the board itself (in paragraph 2.3.2 are detailed current consumption for possible different SOCs) and the power consumption of external devices.

This way it is possible to calculate preliminarily if a 40W PSU can be sufficient for system needing or if most powerful PSUs are required.

2.3.2 Power consumption

Using the following setup, and using all possible SOCs offered for ADLER board, the current consumption has been measured on +12VDC V_{IN} power line.

- O.S. Windows 10
- 32GB eMMC onboard
- USB mouse and keyboard connected
- HDMI + DP++ display connected
- Network connection plugged to Gigabit Ethernet Network.
- TPM 2.0 on-board
- Serial port and HDA
- Bios Release 1.09 Rc01.
- No FAN connected.

Status	SOC			
	E3950 (8GB RAM Quad-Channel LPDDR4)	E3940 (4GB RAM Quad-Channel LPDDR4)	N4200 (4GB RAM Quad-Channel LPDDR4)	N3350 (2GB RAM Double-Channel LPDDR4)
Idle, power saving configuration	228mA	227mA	228mA	197mA
OS Boot, power saving configuration	346mA	322mA	328mA	310mA
Video reproduction@1080p, balanced configuration	464mA	356mA	356mA	354mA
Video reproduction 4K, high performance configuration	711mA	716mA	740mA	602mA
Intel TAT 100% workload CPU and GFX, high performance configuration	1644mA	1220mA	725mA	608mA

Independently by the SOC mounted onboard, the following power consumptions are common to all boards:

Battery Backup power consumption: 3.68µA
Soft-Off State power consumption: 58mA
Suspend State power consumption: 59mA

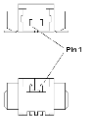
2.3.3 RTC Battery

For the occurrences when the module is not powered with an external power supply, on board there is a cabled coin Lithium Battery to supply, with a 3V voltage, the Real Time Clock embedded inside the SoC.

Battery used is a cabled CR2032-LD Lithium coin-cell battery, with a nominal capacity of 220mAh.

Battery connector - CN3	
Pin	**Signal**
1	V_{RTC}
2	GND

The battery is not rechargeable and can be connected to the board using dedicated connector CN3 which is a 2-pin p1.27 mm type MOLEX p/n 53261-0271 or equivalent, with pinout shown in the table on the left.



Mating connector: MOLEX 51021-0200 receptacle with MOLEX 50079-8000 female crimp terminals.

In case of exhaustion, the battery should only be replaced with devices of the same type. Always check the orientation before inserting and make sure that they are aligned correctly and are not damaged or leaking.

Never allow the batteries to become short-circuited during handling.

! CAUTION: handling batteries incorrectly or replacing with not-approved devices may present a risk of fire or explosion.

Batteries supplied with ADLER board are compliant to requirements of European Directive 2006/66/EC regarding batteries and accumulators. When putting out of order ADLER board, remove the batteries from the board in order to collect and dispose them according to the requirement of the same European Directive above mentioned. Even when replacing the batteries, the disposal has to be made according to these requirements.

2.3.4 Power rails naming convention

In all the tables contained in this manual, Power rails are named with the following meaning:

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

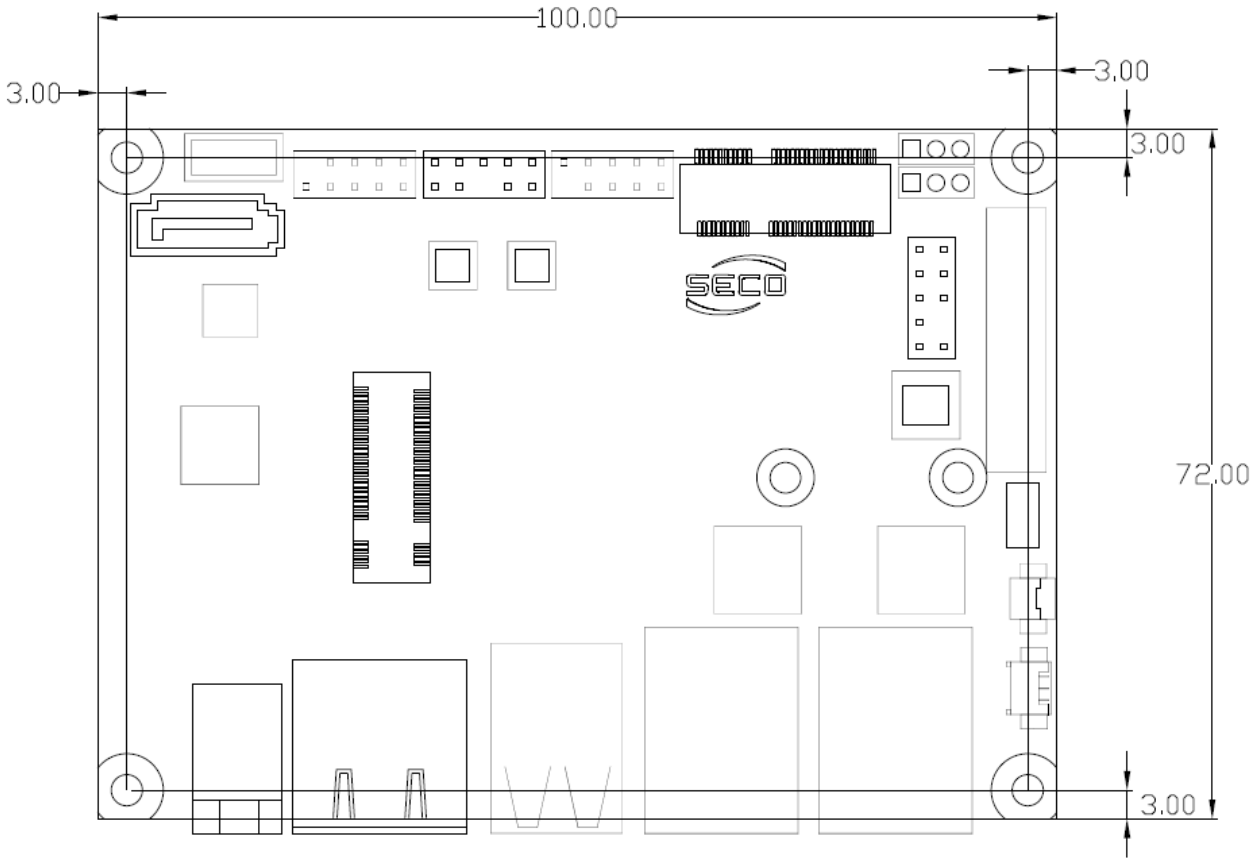
_U: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_U

Other suffixes are used for application specific power rails, which are derived from same voltage value of voltage switched rails, if it is not differently stated (for example, $+5V_{HDMI}$ is derived from +5V_RUN, and so on).

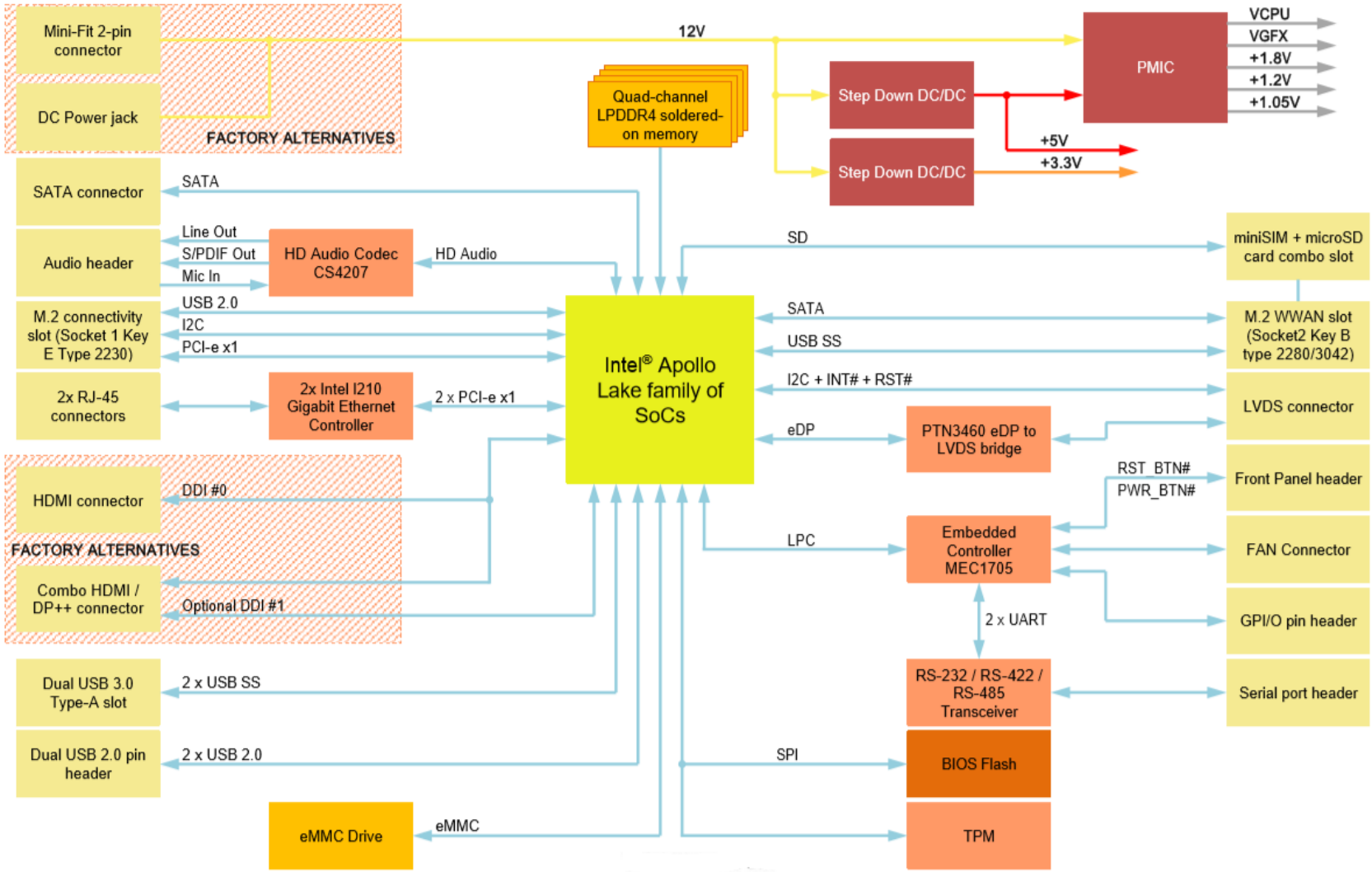
2.4 Mechanical specifications

According to picoITX form factor, board dimensions are: 72 x 100 mm (4.53” x 6.50”).

The printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

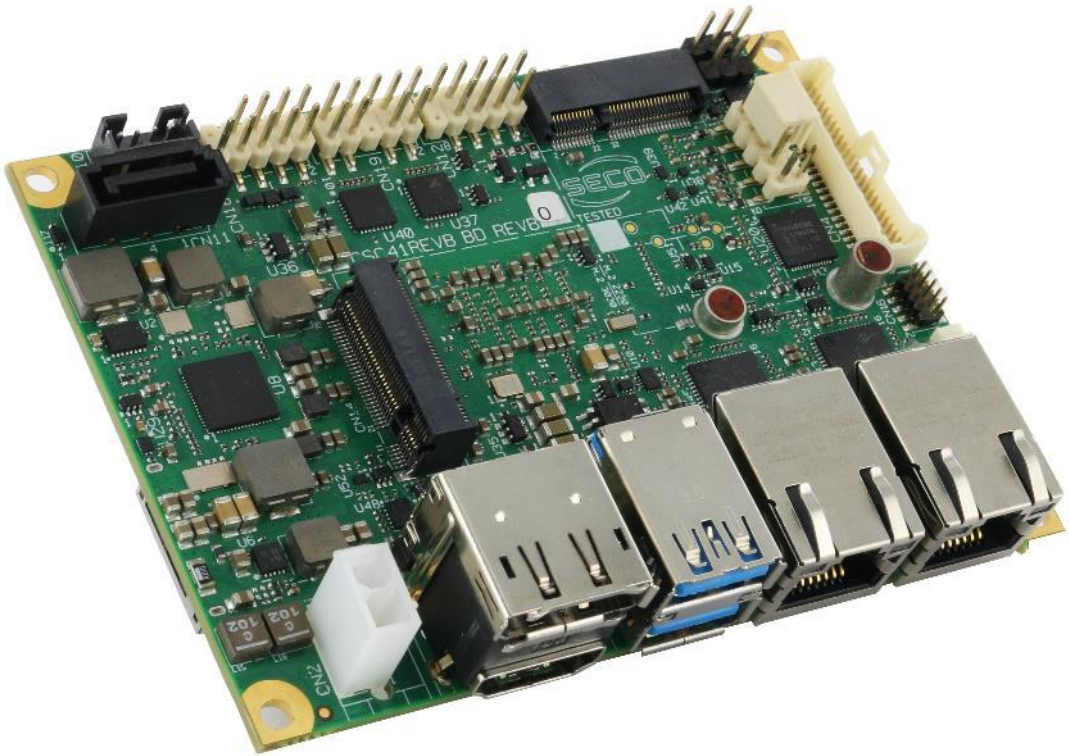


2.5 Block diagram



Chapter 3.
CONNECTORS

- Introduction
- Connectors overview
- Connectors description

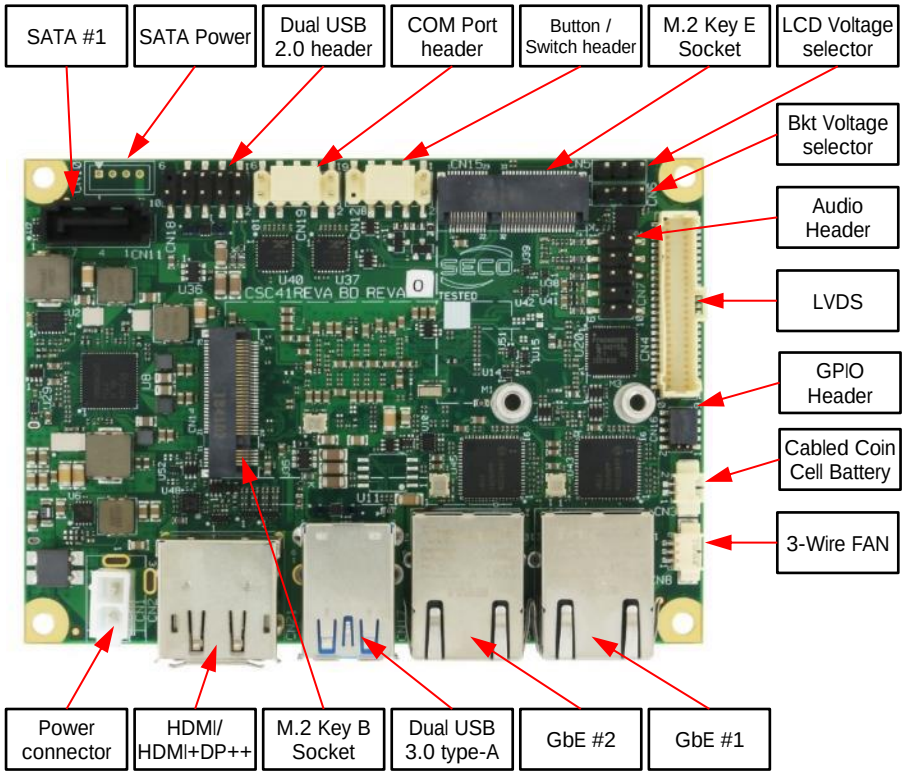


3.1 Introduction

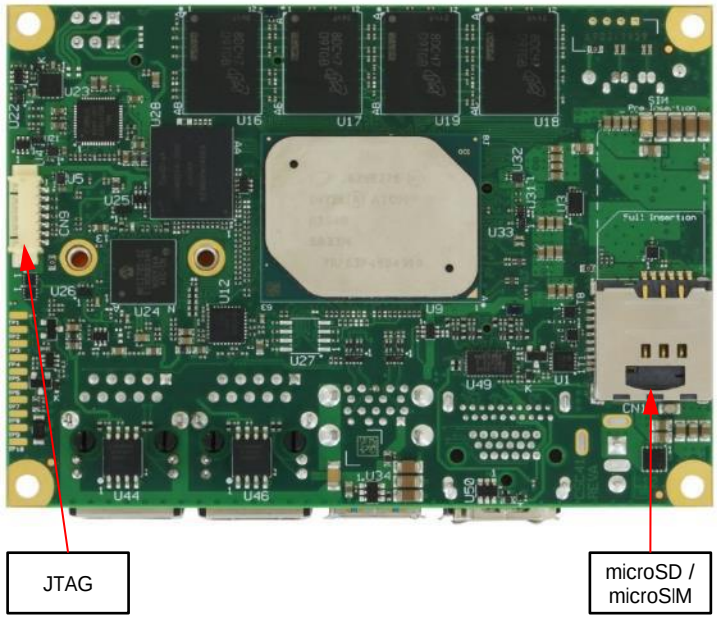
On ADLER board, there are several connectors located on the lower plane. Standard connectors are placed on the same side of PCB, so that it is possible to place them on a panel of an eventual enclosure.

> **!** Please be aware that, depending on the configuration purchased, the appearance of the board could be slightly different from the following pictures.

BOTTOM SIDE



TOP SIDE



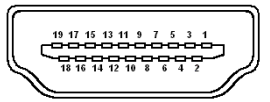
3.2 Connectors overview

Name	Description	Name	Description
CN1	Mini-Fit Power Connector	CN13	Combo microSD / microSIM Slot
CN2	DC Power Jack	CN14	M.2 2260/3042 Socket 2 Key B (SSD/WWAN)
CN3	Cabled Coin Cell Battery	CN15	M.2 2230 Socket 1 Key E (Connectivity Slot)
CN4	LVDS Connector	CN16	GPIO Header
CN5	LCD Voltage selector	CN17	Dual USB 3.0 Type-A connector [0..1]
CN6	Backlight Voltage Selector	CN18	Dual USB 2.0 Internal Header #4 #5
CN7	Audio Header	CN19	COM Port Internal Header
CN8	3-Wire FAN connector	CN20	GbE #1 RJ-45 Connector
CN9	JTAG Connector (reserved for manufacturing purposes)	CN21	Optional combo HDMI + DP++ connector
CN10	SATA Power Connector	CN22	Optional HDMI only connector
CN11	SATA 7p M Connector Port #1	CN23	GbE #2 RJ-45 Connector
CN12	Button/switch Header	SW1	Recovery switch

3.3 Connectors description

3.3.1 HDMI / Multimode Display Port Connectors

HDMI Connector - CN22			
Pin	**Signal**	**Pin**	**Signal**
1	TMDS_LANE2+	2	GND
3	TMDS_LANE2-	4	TMDS_LANE1+
5	GND	6	TMDS_LANE1-
7	TMDS_LANE0+	8	GND
9	TMDS_LANE0-	10	TMDS_CLK+
11	GND	12	TMDS_CLK-
13	CEC	14	---
15	SCL	16	SDA
17	GND	18	+5V$_{HDMI}$
19	HPD		



ADLER board can offer an HDMI technology interface plus an optional DP++ interfaces.

In case that the board purchased in configuration “HDMI only”, then this interface will be available on connector CN22, which is an HDMI approved connector type Freeport p/n 51L019S-30GN-BD.

Signals involved in HDMI management are the following:

TMDS_CLK+/TMDS_CLK-: TMDS differential Clock.

TMDS_LANE0+/TMDS_LANE0-: TMDS differential pair #0

TMDS_LANE1+/TMDS_LANE1-: TMDS differential pair #1

TMDS_LANE2+/TMDS_LANE2-: TMDS differential pair #2

SDA: DDC Data line for HDMI panel. Bidirectional signal, electrical level +5V$_{HDMI}$ with a 1k8Ω pull-up resistor.

SCL: DDC Clock line for HDMI panel. Output signal, electrical level +5V$_{HDMI}$ with a 1k8Ω pull-up resistor.

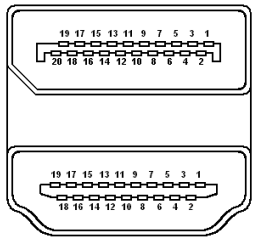
CEC: HDMI Consumer Electronics Control (CEC) Line. Bidirectional signal, electrical level +3.3V_ALW with a 27kΩ pull-up resistor.

HPD: Hot Plug Detect Input signal.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

Always use HDMI-certified cables for the connection between the board and the HDMI display; a Standard HDMI Cable can be used for 720p resolution, while a High-Speed HDMI Cable is recommended for higher resolutions.

HDMI+DP++ Connector - CN21 (factory alternative)			
Pin	Signal	Pin	Signal
A1	TMDS_LANE2+	A2	GND
A3	TMDS_LANE2-	A4	TMDS_LANE1+
A5	GND	A6	TMDS_LANE1-
A7	TMDS_LANE0+	A8	GND
A9	TMDS_LANE0-	A10	TMDS_CLK+
A11	GND	A12	TMDS_CLK-
A13	HDMI_CEC	A14	---
A15	SCL	A16	SDA
A17	GND	A18	+5V$_{HDMI}$
A19	HPD		
B1	DP_LANE0+	B2	GND
B3	DP_LANE0-	B4	DP_LANE1+
B5	GND	B6	DP_LANE1-
B7	DP_LANE2+	B8	GND
B9	DP_LANE2-	B10	DP_LANE3+
B11	GND	B12	DP_LANE3-
B13	CAD	B14	DP_CEC
B15	DP_CLK_AUX+	B16	GND
B17	DP_DAT_AUX-	B18	DP_HPD
B19	GND	B20	DP_PWR



As a factory alternative, it is possible to have two video outputs, i.e. a standard HDMI technology interface and a multimode Display Port Interface.

In this latest case, these interfaces will be available on a combo HDMI + DP++ connector, CN21, type Freeport p/n 62EHDS-30AN0-P1-D. DDI Interface #0 will be available on the HDMI connector, while DDI interface #1 will be available on the DP++ connector (see image on the left).

Signals involved in HDMI and DP++ management are the following:

TMDS_CLK+/TMDS_CLK-: TMDS differential Clock.

TMDS_LANE0+/TMDS_LANE0-: TMDS differential pair #0

TMDS_LANE1+/TMDS_LANE1-: TMDS differential pair #1

TMDS_LANE2+/TMDS_LANE2-: TMDS differential pair #2

SDA: DDC Data line for HDMI panel. Bidirectional signal, electrical level +5V$_{HDMI}$ with a 1k8Ω pull-up resistor.

SCL: DDC Clock line for HDMI panel. Output signal, electrical level +5V$_{HDMI}$ with a 1k8Ω pull-up resistor.

HDMI_CEC: HDMI Consumer Electronics Control (CEC) Line. Bidirectional signal, electrical level +3.3V_ALW with a 27kΩ pull-up resistor.

HPD: HDMI Hot Plug Detect Input signal.

DP_LANE0+/DP_LANE0-: Display Port differential data pair #0

DP_LANE1+/DP_LANE1-: Display Port differential data pair #1

DP_LANE3+/DP_LANE3-: Display Port differential data pair #2

DP_LANE4+/DP_LANE4-: Display Port differential data pair #4

DP_CLK_AUX+/DP_DAT_AUX-: Display Port auxiliary channel differential data pair / DDC Clock and Data Line for HDMI panels. See CAD signal description.

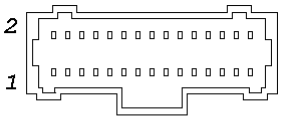
DP_CEC: DP Consumer Electronics Control (CEC) Line. Bidirectional signal, electrical level +3.3V_ALW with a 27kΩ pull-up resistor.

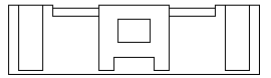
DP_HPD: DP Hot Plug Detect Input signal. +3.3V_RUN electrical level signal with 100kΩ pull-down resistor

CAD: This signal is used to automatically configure DP or HDMI technology interface on DP++ connector. When a DP cable is connected, then the CAD signal remains floating. The internal circuitry will recognize this configuration, making available the Display Port Auxiliary channel signals on pins B15/B17. Instead, when a DP-to-HDMI adapter is connected, it will drive the CAD pin accordingly, making available HDMI_CTRL_CLK and HDMI_CTRL_DAT signals on B15/B17 pins.

3.3.2 LVDS Connector

LVDS connector – CN4			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	GND
3	LVDS_B_TX3+	4	LVDS_A_TX3+
5	LVDS_B_TX3-	6	LVDS_A_TX3-
7	LVDS_B_TX2+	8	LVDS_A_TX2+
9	LVDS_B_TX2-	10	LVDS_A_TX2-
11	LVDS_B_TX1+	12	LVDS_A_TX1+
13	LVDS_B_TX1-	14	LVDS_A_TX1-
15	LVDS_B_TX0+	16	LVDS_A_TX0+
17	LVDS_B_TX0-	18	LVDS_A_TX0-
19	GND	20	GND
21	LVDS_B_CLK+	22	LVDS_A_CLK+
23	LVDS_B_CLK-	24	LVDS_A_CLK-
25	GND	26	GND
27	LVDS_I2C_CLK	28	BKLT_EN
29	LVDS_I2C_DATA	30	BKLT_PWM
31	+3.3V_RUN	32	PVCC_EN
33	LCD_PWR	34	BKLT_PWR
35	LCD_PWR	36	BKLT_PWR
37	LCD_PWR	38	BKLT_PWR
39	GND	40	GND
41	GND	42	GND
43	GND	44	GND
45	TOUCH_RST#	46	TOUCH_SCL
47	TOUCH_INT#	48	TOUCH_SDA
49	+3.3V_RUN	50	GND





ADLER can be interfaced to LCD displays using its LVDS interface, which allows connecting 18 or 24 bit, single or dual channel displays. This interface is implemented using an eDP to LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hx (dual channel mode). Such an interface is derived from Processor's eDP Interface.

For the connection, a connector type HR A1014WA-S-2x25P or equivalent (2 x 25p, male, straight, P1, low profile, polarised) is provided.

Mating connector: HR A1014H-2X25P with HR A1014-T female crimp terminals.

Alternative mating connector, MOLEX 501189-5010 with crimp terminals series 501334.

On the same connectors, are also implemented signals for direct driving of display's backlight: voltages (LCD_PWR and BKLT_PWR) and control signals (LCD enable signal, PVCC_EN, Backlight enable signal, BKLT_EN, and Backlight Brightness Control signal, BKLT_PWM).

There are also the signals necessary for driving I2C touchscreens (I2C signals, reset and interrupt request signals).

When building a cable for connection of LVDS displays, please take care of twist as tight as possible differential pairs' signal wires, in order to reduce EMI interferences. Shielded cables are also recommended.

Here following the signals related to LVDS management:

LVDS_A_TX0+/ LVDS_A_TX0-: LVDS Channel A differential data pair #0.

LVDS_A_TX1+/ LVDS_A_TX1-: LVDS Channel A differential data pair #1.

LVDS_A_TX2+/ LVDS_A_TX2-: LVDS Channel A differential data pair #2.

LVDS_A_TX3+/ LVDS_A_TX3-: LVDS Channel A differential data pair #3.

LVDS_A_CLK+/LVDS_A_CLK-: LVDS Channel A differential Clock.

LVDS_B_TX0+/ LVDS_B_TX0-: LVDS Channel B differential data pair #0.

LVDS_B_TX1+/ LVDS_B_TX1-: LVDS Channel B differential data pair #1.

LVDS_B_TX2+/ LVDS_B_TX2-: LVDS Channel B differential data pair #2.

LVDS_B_TX3+/ LVDS_B_TX3-: LVDS Channel B differential data pair #3.

LVDS_B_CLK+/LVDS_B_CLK-: LVDS Channel B differential Clock.

LVDS_I2C_DAT: DisplayID I2C Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN with a 2k2Ω pull-up resistor.

LVDS_I2C_CLK: DisplayID I2C Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN with a 2k2Ω pull-up resistor.

BKLT_EN: +3.3V_RUN electrical level Output with a 10kΩ pull-down resistor, Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected displays.

PVCC_EN: +3.3V_RUN electrical level Output with a 10kΩ pull-down resistor, Panel Power Enable signal. It can be used to turn On/Off the connected display.

BKLT_PWM: this signal can be used to adjust the backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations (+3.3V_RUN electrical level).

TOUCH_SCL: I2C Bus clock line. Bidirectional signal, electrical level +3.3V_RUN with a 2K2Ω pull-up resistor. It is managed by the processor's I2C controller #4.

TOUCH_SDA: I2C Bus data line. Bidirectional signal, electrical level +3.3V_RUN with a 2K2Ω pull-up resistor. It is managed by the processor's I2C controller #4.

TOUCH_RST#: +3.3V_ALW electrical level output, active low. This signal can be used to drive a reset of an eventual external Touch Screen connected to the dedicated I2C interface.

TOUCH_INT#: +3.3V_RUN electrical level input with a 100kΩ pull-up resistor. This signal can be used to serve the interrupt request of an eventual external Touch Screen connected to the dedicated I2C interface.

CN5 position	LCD_PWR voltage value
1-2	+3.3V_ALW
2-3	+5V_ALW

LCD_PWR: LCD Voltage rail. Its value can be set to +3.3V_ALW or +5V_ALW by using dedicated jumper CN5, which is a standard pin header, P2.54mm, 1x3 pin.

CN6 position	BKLT_PWR voltage value
1-2	+5V_ALW
2-3	+12V_ALW

BKLT_PWR: Backlight Voltage rail. Its value can be set to +5V_ALW or +12V_ALW by using dedicated jumper CN6, which is another standard pin header, P2.54mm, 1x3 pin.

As an alternative, especially for applications where vibrations are a problem, it is possible to set LCD_PWR and BKLT_PWR voltage values by closing the circuit breakers that are located under the pin headers (they are normally not accessible on samples, due to the presence of the pin header, but could be requested for mass productions).

3.3.3 Audio Header

HD Audio Front Panel Header – CN7			
Pin	**Signal**	**Pin**	**Signal**
1	Mic_In_L	2	Audio_GND
3	Mic_In_R	4	S/PDIF_Out
5	Line_Out_R	6	Sense1_Return
7	Audio_GND		
9	Line_Out_L	10	Sense2_Return

ADLER board integrates a High Definition Audio Codec, Cirrus Logic CS4207-CNRZ, for high quality audio implementation.

In order to give the maximum flexibility to ADLER board, it is available a dedicated 9-pin 2.54mm pitch Pin header for external connection of a Line Out output, a Mic In input and also an S/PDIF Output.

Pinout hereby shown is compliant to "Intel® Front Panel I/O connectivity Design Guide" specifications, par. 2.3.5 Table 7.

Using this dedicated connector, it will be possible to connect any Azalia compliant panel audio jack to remote audio connectors in the preferred position.

Signals Description

Mic_In_L: Analog Port 1 - Microphone Left Channel.

Mic_In_R: Analog Port 1 - Microphone Right Channel.

Sense1_Return: Analog Port 1 - Jack detection return signal.

Line_Out_L: Analog Port 2 - Headphone Left Channel.

Line_Out_R: Analog Port 2 - Headphone Right Channel.

Sense2_Return: Analog Port 2 - Jack detection return signal.

S/PDIF_Out: S/PDIF AC-coupled output.

3.3.4 Buttons / LED Header

Buttons / LED Header – CN12			
Pin	**Signal**	**Pin**	**Signal**
1	HD_LED_P	2	FP PWR_P/SLP_N
3	HD_LED_N	4	FP PWR_N/SLP_P
5	RST_SW_N	6	PWR_SW_P
7	RST_SW_P	8	PWR_SW_N
9	---		

To allow the integration of the ADLER board inside a box PC-like, there is a connector on the board that allows to remote signals for the Power Button (to be used to put the system in a Soft Off State, or awake from it), for the Reset Button, and the signal for optional LED signaling activity on SATA Channel and Power On states.

The pinout of this connector complies with Intel® Front Panel I/O connectivity Design Guide, Switch/LED Front Panel section, chapter 2.2. It is shown in the table on the left.

Connector CN12 is an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E10 or equivalent.

Signals Description

HD_LED_P: Hard Disk Activity LED signal's pull-up to +5V_RUN voltage (510Ω pull-up).

HD_LED_N: Hard Disk Activity LED output signal

RST_SW_N: Reset Button GND

RST_SW_P: Reset button input signal. This signal has to be connected to an external momentary pushbutton (contacts normally open). When the pushbutton is pressed, the pulse of Reset signal will cause the reset of the board. +3.3V_ALW electrical level with 10kΩ pull-up.

PWR_SW_P: Power button input signal, +3.3V_ALW electrical level with 10kΩ pull-up. This signal has to be connected to an external momentary pushbutton (contacts normally open). Upon the pressure of this pushbutton, the pulse of this signal will let the switched voltage rails turn on or off.

PWR_SW_N: Power button GND

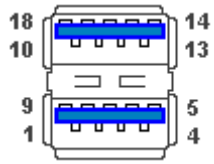
FP PWR_P/SLP_N: Power/Sleep messaging LED terminal 1, +5V_ALW voltage. Connect it to an extremity of a dual-color power LED for power ON/OF, sleep and message waiting signaling. Please refer to Intel® Front Panel I/O connectivity Design Guide, chapter 2.2.4, for LED functionalities and signal meaning.

FP PWR_N/SLP_P: Power/Sleep messaging LED terminal 2, +5V_ALW voltage. Connect it to the other extremity of the dual-color power LED above mentioned.

3.3.5 USB Connectors

USB 3.0 ports Type-A double receptacle - CN17			
Pin	**Signal**	**Pin**	**Signal**
1	$+5V_{USB1}$	10	$+5V_{USB0}$
2	USB_H1-	11	USB_H0-
3	USB_H1+	12	USB_H0+
4	GND	13	GND
5	USB_SSRX1-	14	USB_SSRX0-
6	USB_SSRX1+	15	USB_SSRX0+
7	GND	16	GND
8	USB_SSTX1-	17	USB_SSTX0-
9	USB_SSTX1+	18	USB_SSTX0+

The ADLER board offers the possibility of connecting to many standard USB ports.



USB 3.0 ports are carried to a double type-A USB 3.0 receptacle, CN17, type Winning p/n WDU3R-18F1B4PBUN3 or equivalent.

More specifically, USB 3.0 port #0 is carried to the upper USB receptacle of CN17, while USB 3.0 port #1 is carried to the lower USB receptacle of CN17.

Dual USB 2.0 Internal Header #4 #5 – CN18			
Pin	**Signal**	**Pin**	**Signal**
1	$+5V_{USB4}$	2	$+5V_{USB5}$
3	USB_P4-	4	USB_P5-
5	USB_P4+	6	USB_P5+
7	GND	8	GND
		10	---

There are also two additional USB 2.0 ports (USB #4 and USB #5), which are hosted on a 9-pin p2.54mm pin header, h= 6mm, type NELTRON p/n 2213S-10G-E9 or equivalent, with the pinout shown in the tables on the left (it is a common pinout for USB headers in PC motherboards).

All USB ports' voltages ($+5V_{USBx}$) are derived from +5V_ALW standby voltages. This means that the ports can be powered also when the OS is in Suspend-to-RAM (S3) state in order to support (if enabled) e the "Wake-Up on USB" functionality.

Signal description:

USB_H1+/USB_H1-: USB Port #1 differential pair; it is managed by processor's xHCI controller.

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair; it is managed by processor's xHCI controller.

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair; it is managed by processor's xHCI controller.

USB_H2+/USB_H2-: USB Port #2 differential pair; it is managed by processor's xHCI controller.

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair; it is managed by processor's xHCI controller

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair; it is managed by processor's xHCI controller

USB_P4+/USB_P4-: USB Port #4 differential pair; it is managed by processor's xHCI controller

USB_P5+/USB_P5-: USB Port #5 differential pair, it is managed by processor's xHCI controller

Common mode chokes are placed on all USB differential pairs for EMI compliance.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

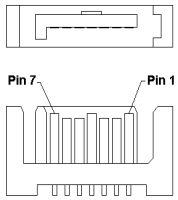
3.3.6 SATA Connector

The Apollo Lake family of SoCs embeds a SATA Controller, which offers two SATA III, 6.0 Gbps interfaces.

S-ATA Connector – CN11

Pin	Signal
1	GND
2	SATA1_Tx+
3	SATA1_Tx-
4	GND
5	SATA1_Rx-
6	SATA1_Rx+
7	GND

Of these interfaces, one SATA channel is carried out to a standard male S-ATA connector, CN11 (the other SATA channel is available on the M.2 Key B socket, CN14, please check par. 3.3.7)
Here following the signals related to SATA interface:



SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair

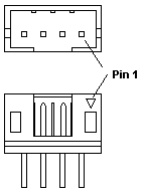
SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

S-ATA Power Connector – CN10

Pin	Signal
1	---
2	GND
3	GND
4	+5V_RUN

A dedicated power connector, CN10, can be used to give supply to external Hard Disks (or Solid State Disks) connected to the SATA male connector.



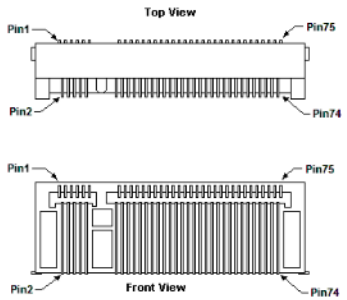
The dedicated power connector is a 4-pin male connector, type HR p/n A2001WV-S-04 or equivalent, with pinout shown in the table on the left.

Mating connector: HR A2001H-04P housing with HR A2001 series crimp terminals.

3.3.7 M.2 3042 Socket 2 Key B SSD/WWAN Slot

M.2 SSD/WWAN Slot (Socket 2 Key B type 2260/3042) – CN14			
Pin	**Signal**	**Pin**	**Signal**
1	CONFIG_3	2	+3.3V_ALW
3	GND	4	+3.3V_ALW
5	GND	6	PWR_OFF#
7	USB_P2+	8	KEYB_W_DISABLE1#
9	USB_P2-	10	---
11	GND	20	---
21	CONFIG_0	22	---
23	WAKE_ON_WWAN#	24	---
25	---	26	KEYB_W_DISABLE2#
27	GND	28	---
29	USB_SSRX2-	30	UIM_RST#
31	USB_SSRX2+	32	UIM_CLK
33	GND	34	UIM_DATA
35	USB_SSTX2-	36	UIM_PWR
37	USB_SSTX2+	38	---
39	GND	40	---
41	SATA_Rx0+	42	---
43	SATA_RX0-	44	---
45	GND	46	---
47	SATA_TX0-	48	---
49	SATA_TX0+	50	PLT_RST#
51	GND	52	---
53	---	54	---
55	---	56	---
57	GND	58	---
59	---	60	---

The mass storage capabilities of the ADLER board are completed by an M.2 SSD Slot, which allow plugging M.2 Socket 2 Key B Solid State Drives.
The same slot can be used alternatively for the connection of Connectivity modules, using USB 3.0 interface.
The connector used for the M.2 SSD slot is CN14, which is a standard 75 pin M.2 Key B connector, type LOTES p/n APCI0087-P001A, H=8.5mm, with the pinout shown in the table on the left.



On the ADLER board there is also a Threaded Spacer which allows the placement of M.2 Socket 2 Key B SSD or WWAN modules in 2260 or 3042 size.

61	---	62	---
63	---	64	---
65	---	66	UIM_DETECT
67	---	68	---
69	CONFIG_1	70	+3.3V_M2
71	GND	72	+3.3V_M2
73	GND	74	+3.3V_M2
75	CONFIG_2		

Signal Description

USB_P2+ / USB_P2-: USB Port #2 differential pair; it is managed by the processor's xHCI controller.

WAKE_ON_WWAN#: Board's Wake Input, 1.8V_ALW active low signal with 100kΩ pull-up resistor. It must be externally driven by the Connectivity module plugged in the slot when it requires waking up the system (functionality not yet supported by the BIOS).

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair; it is managed by xHCI controller

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair; it is managed by xHCI controller

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair

PWR_OFF#: Power Off signal for plugged modules, usually used in battery-powered systems. Fixed 10kΩ pull-up @ 3.3V_ALW

KEYB_W_DISABLE1#: M.2 Key B module disable signal #1, 3.3V_ALW active low output

KEYB_W_DISABLE2#: M.2 Key B module disable signal #2, 3.3V_ALW active low output

UIM_RESET: Reset signal line, sent from M.2 WWAN card to the UIM module.

UIM_DATA: Bidirectional Data line between M.2 WWAN card and UIM module.

UIM_CLK: Clock line, output from M.2 WWAN card to the UIM module.

UIM_PWR: Power line for UIM module.

PLT_RST#: Reset Signal that is sent from the SoC to all devices available on the board (i.e. the GbE controllers and the modules plugged in the CN15 slot). It is a 3.3V active-low signal with 100kΩ pull-down.

CONFIG_[0..3]: Configuration inputs, +3.3V_ALW signals with 10kΩ pull-up. These signals are used to configure properly the Main Host interface according to the Add-In Card plugged in CN14 Slot. These configuration pins are managed according to PCI Express M.2 Specifications Table 5.5. Only SATA SSDs and WWAN USB3.1 modules are supported.

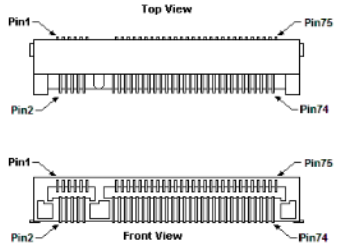
3.3.8 M.2 2230 Socket 1 Key E Connectivity Slot

M.2 Connectivity Slot (Socket 1 Key E type 2230) - CN15			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	+3.3V_ALW
3	USB_P3+	4	+3.3V_ALW
5	USB_P3-	6	---
7	GND	8	---
9	---	10	---
11	---	12	---
13	---	14	---
15	---	16	---
17	---	18	GND
19	---	20	---
21	---	22	---
23	---		
		32	---
33	GND	34	---
35	PCIe0_Tx+	36	---
37	PCIe0_Tx-	38	---
39	GND	40	---
41	PCIe0_Rx+	42	---
43	PCIe0_Rx-	44	---
45	GND	46	---
47	PCIe0_CLK+	48	---
49	PCIe0_CLK-	50	SUS_CLK
51	GND	52	PLT_RST#
53	CLK_REQ0#	54	KEYE_W_DISABLE2#
55	PCIe_WAKE#	56	KEYE_W_DISABLE1#
57	GND	58	---

It is possible to increase the connectivity of the ADLER board by using M.2 Socket 1 Key E connectivity slot.

The connector used for the M.2 Connectivity slot is CN15, which is a standard 75 pin M.2 Key E connector, type LOTES p/n APCI0076-P001A, H=4.2mm, with the pinout shown in the table on the left.

On the ADLER board there is also a Threaded Spacer which allows the placement of M.2 Socket 1 Key E connectivity modules in 2230 size.



59	---	60	---
61	---	62	---
63	GND	64	---
65	---	66	---
67	---	68	---
69	GND	70	---
71	---	72	+3.3V_ALW
73	---	74	+3.3V_ALW
75	GND		

Signal Description

USB_P3+ / USB_P3-: USB Port #3 differential pair; it is managed by the processor's xHCI controller.

PCIe0_Tx+/PCIe0_Tx-: PCI Express lane #0, Transmitting Output Differential pair

PCIe0_Rx+/PCIe0_Rx-: PCI Express lane #0, Receiving Input Differential pair

PCIe0_CLK+/ PCIe0_CLK-: PCI Express Reference Clock for lane #0, Differential Pair

PCIe_WAKE#: Board's Wake Input, it must be externally driven by the module inserted in the slot when it requires waking up the system.

CLK_REQ0#: PCI-e Clock request. Bidirectional signal, electrical level +3.3V_ALW with a 10KΩ pull-up resistor

SUS_CLK: 32.768kHz Clock provided by the ADLER board to the module plugged in the slot CN15. +3.3V_ALW electrical level.

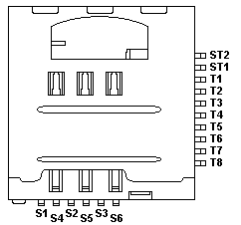
PLT_RST#: Reset Signal that is sent from the SoC to all PCI-e devices available on the board (i.e. the GbE controllers and the modules plugged in the CN14 slot). It is a 3.3V active-low signal with 100kΩ pull-down.

KEYE_W_DISABLE1#: M.2 Key E module disable signal #1, 3.3V_ALW active low output

KEYE_W_DISABLE2#: M.2 Key E module disable signal #2, 3.3V_ALW active low output

3.3.9 microSD + miniSIM Combo Slot

µSD + miniSIM Combo Card Slot – **CN13**			
Pin	**Signal**	**Pin**	**Signal**
S1	UIM_PWR	T3	SDIO_CMD
S2	UIM_RST#	T4	SDIO_VDD
S3	UIM_CLK	T5	SDIO_CLK
S4	GND	T6	GND
S5	---	T7	SDIO_DAT0
S6	UIM_DATA	T8	SDIO_DAT1
T1	SDIO_DAT2	ST1	SDIO_CD#
T2	SDIO_DAT3	ST2	GND



On ADLER board there is also a socket, for the use of standard SD cards, to be used as Mass Storage Device and/or Boot Device.

Moreover, ADLER board can accept also miniSIM cards, for use of M.2 Key B modems.

Both these cards can be inserted in the dedicated slot of connector CN13, which is a combo µSD/MMC + miniSIM connector, push-push type, 2.7 mm global height, type AVX p/n 009162006501150 or equivalent. Pinout here reported is related only to signal routing on specific connector; internally the pin-out is the same of any standard SD/MMC 4.0 and miniSIM card.

For ESD protection, on all signal lines are placed clamping diodes for voltage transient suppression.

Signals related to UIM (SIM) card are described in paragraph 3.3.7 for description. Signals related to SD cards are the following:

SDIO_CD#: Card Detect Input.

SDIO_CLK: SD Clock Line (output).

SDIO_CMD: Command/Response bidirectional line.

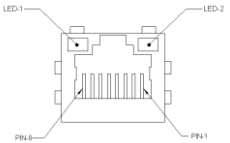
SD_DATA[0÷3]: SD Card data bus. SD_DATA0 signal is used for all communication modes. SD_DATA[1÷3] signals are required for 4-bit communication mode.

SDIO_VDD: +3.3V_ALW SD dedicated Power rail

3.3.10 Gigabit Ethernet connectors

Gigabit Ethernet Port #1 – CN20			
Pin	**Signal**	**Pin**	**Signal**
1	GBE1_MDI0+	5	GBE1_MDI2-
2	GBE1_MDI0-	6	GBE1_MDI1-
3	GBE1_MDI1+	7	GBE1_MDI3+
4	GBE1_MDI2+	8	GBE1_MDI3-

Optional Gigabit Ethernet Port #2 – CN23			
Pin	**Signal**	**Pin**	**Signal**
1	GBE2_MDI0+	5	GBE2_MDI2-
2	GBE2_MDI0-	6	GBE2_MDI1-
3	GBE2_MDI1+	7	GBE2_MDI3+
4	GBE2_MDI2+	8	GBE2_MDI3-



On board, there are two Gigabit Ethernet connector, for the direct connection of the ADLER to two different wired LANs.

The Ethernet connection is realised by using two different Intel® I21x family Gigabit Ethernet controllers.

First connection is available on connector CN20, and is always available, The second connection, available on RJ-45 connector CN23, instead, is available only as a factory option

This interface is compatible both with Gigabit Ethernet (1000Mbps) and with Fast Ethernet (10/100Mbps) Networks. They will configure automatically to work with the existing network.

Please be aware that it will work in Gigabit mode only in case that it is connected to Gigabit Ethernet switches/hubs/routers. For the connection, cables category Cat5e or better are required. Cables category Cat6 are recommended for noise reduction and EMC compatibility issues, especially when the length of the cable is significant.

On the connectors there are also two bicolor (Green /Yellow) LEDs for each port. Left LED shows 10/100 or 1000 connection: green means 100Mbps connection, yellow means 1000Mpbs connection, when the LED is Off then 10Mpbs or no connection is available. The right LED blinks Green to show ACTIVITY presence.

GBEx_MDI0+/GBEx_MDI0-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #0. It is the first differential pair in Gigabit Ethernet mode, and the Transmit differential pair in 10/100 Mbps modes.

GBEx_MDI1+/GBEx_MDI1-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #1. It is the second differential pair in Gigabit Ethernet mode, and the Receive differential pair in 10/100 Mbps modes.

GBEx_MDI2+/GBEx_MDI2-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #2. It is the third differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

GBEx_MDI3+/GBEx_MDI3-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #3. It is the fourth differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes

3.3.11 COM Port Header

Dual RS-232/RS-422/RS-485 pin header- CN19			
Pin	**Signal RS-232 mode**	**Signal RS-422 mode**	**Signal RS-485 mode**
1	COM1_RxD	COM1_Rx+	
2	COM2_RxD	COM2_Rx+	
3	COM1_TxD	COM1_Tx-	COM1_Data-
4	COM2_TxD	COM2_Tx-	COM2_Data-
5	GND	GND	GND
7	COM1_RTS#	COM1_Tx+	COM1_Data+
8	COM2_RTS#	COM2_Tx+	COM2_Data+
9	COM1_CTS#	COM1_Rx-	
10	COM2_CTS#	COM2_Rx-	

The embedded controller of ADLER board manages two 4-wire legacy UARTs, which are carried to as many multistandard RS-23/RS-422/RS-485 transceivers, allowing the implementation of two multistandard serial ports (from now on respectively named COM1 and COM2).

These ports are available on dedicated connector CN19, which is an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h = 6mm, type NELTRON p/n 2213S-10G-E06 or equivalent.

Signals Description

COM1_RxD/COM2_RxD: COM port #1 / #2 RS-232 Receive data

COM1_TxD/COM2_TxD: COM port #1 / #2x RS-232 Transmit data

COM1_RTS#/COM2_RTS#: COM port #1 / #2 RS-232 Request to Send handshaking signal.

COM1_CTS#/COM2_CTS#: COM port #1 / #2x RS-232 Clear To Send handshaking signal

COM1_RX+/COM1_RX-: COM port #1 RS-422 receive differential pair

COM1_TX+/COM1_TX-: COM port #1 RS-422 Transmit differential pair

COM2_RX+/COM2_RX-: COM port #2 Full Duplex RS-485 (RS-422) Receive differential pair

COM2_TX+/COM2_TX-: COM port #2 Full Duplex RS-485 (RS-422) Transmit differential pair

COM1_Data+/COM1_Data-: COM Port #1 Half Duplex RS-485 Differential Pair

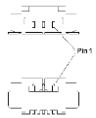
COM2_Data+/COM2_Data-: COM Port #2 Half Duplex RS-485 Differential Pair

The selection of the kind of interface (RS-232, RS-422 or RS-485) can be made via BIOS (please check par. 4.3.14).

Please be aware that for proper RS-485 working, the RTS# signals must be used as a handshaking signal, i.e. it is used to control the data flow direction. When RTS# signal is driven low, then the RS-485 port is in receiving mode, when RTS# signal is driven high then the RS-458 port is in transmitting mode.

3.3.12 FAN Connector

3-Wire FAN Connector – CN8	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN



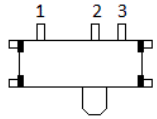
Depending on the usage model of ADLER, for critical applications/environments on ADLER it is available a dedicated connector for an external +12V_{DC} FAN.

The FAN Connector is a 3-pin single line SMT connector, type MOLEX 53261-0371 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

3.3.13 Recovery Switch



In some cases, a wrong configuration of BIOS parameters could lead the module in an unusable state (i.e. no video output, all USB HID devices disabled).

For these cases, on the board it has been placed a 3-way switch which can be used to restore the BIOS to factory default configuration. To do so, it is necessary to place the contact of the switch in 1-2 position, then turn on the module, wait until the board resets itself then turn off the board. The contact MUST be now placed back to 2-3 position.

During normal use, the contact MUST be always placed in 2-3 position.

3.3.14 GPIO Header

GPIO Header – CN16			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V_RUN	2	GND
3	EXT_GPIO0	4	EXT_GPIO7
5	EXT_GPIO1	6	EXT_GPIO6
7	EXT_GPIO2	8	EXT_GPIO5
9	EXT_GPIO3	10	EXT_GPIO4

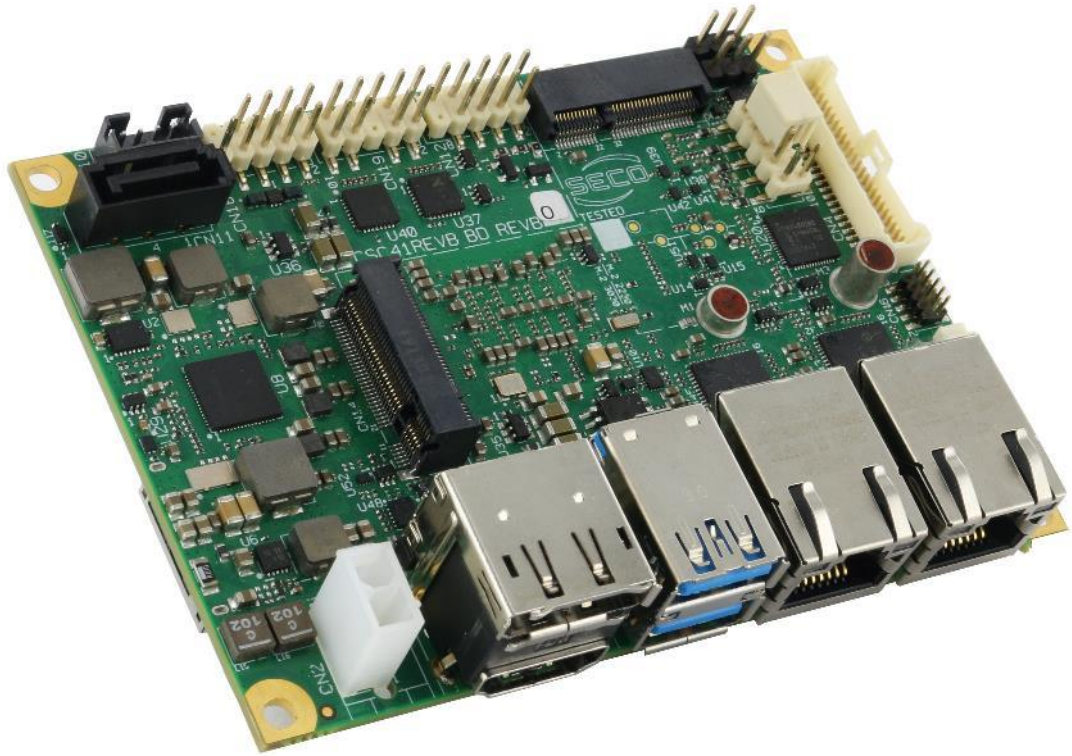
Managed by the Embedded Controller, on ADLER board there are 8 (eight) GPIOs at electrical level 3.3V (5V tolerant).

Access to these General Purpose I/Os comes through a dual-row 10-pin SMT male pin-header, p. 1.27mm, type NELTRON 2199SB-10G-SM-3021-CR or equivalent, with pinout shown in the table on the left.

EXT_GPIO_[0..7]: I/O Expander Input/Output [0..7], voltage reference level: +3.3V_ALW

Chapter 4.
BIOS SETUP

- Aptio setup Utility
- Main setup menu
- Advanced menu
- Chipset menu
- Security menu
- Boot menu
- Save & Exit menu



4.1 Aptio setup Utility

Basic setup of the board can be done using American Megatrends, Inc. “Aptio Setup Utility”, that is stored inside an onboard SPI Serial Flash.

It is possible to access to Aptio Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select “SCU” icon.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
+ / -	+ and - keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows displaying the General Help screen.
<F2>	Previous Values
<F3>	<F3> key allows loading Optimised Defaults for the board. After pressing <F3> BIOS Setup utility will request for a confirmation, before loading such default values. By pressing <ESC> key, this function will be aborted
<F4>	<F4> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows discarding any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow displaying the setup sub-screens.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

4.2.1 System Date / System Time

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Trusted Computing	See submenu	Trusted Computing Settings
ACPI Settings	See submenu	System ACPI parameters
S5 RTC Wake Settings	See submenu	Enable system to wake from S5 using RTC alarm
CPU Configuration	See submenu	CPU Configuration Parameters
AMI Graphic Output Protocol Policy	See submenu	User Selected Monitor Output by Graphic Output protocol
PCI Subsystems Settings	See submenu	PCI Subsystems Settings
Network Stack Configuration	See submenu	Network Stack Settings
CSM Configuration	See submenu	Compatibility Support Module(CSM) Configuration: Enable/Disable, Option ROM execution Settings, etc…
NVMe Configuration	See submenu	NVMe Device Options Settings
SDIO Configuration	See submenu	SDIO Configuration Parameters
USB Configuration	See submenu	USB Configuration Parameters
Platform Trust technology	See submenu	Platform Trust Technology
Main Thermal Configuration	See submenu	Main Thermal Configuration
HSUART Transceiver Configuration	See submenu	HSUART Transceiver Configuration Utility
LVDS Configuration	See submenu	LVDS Configuration
SMBIOS Information	See submenu	SMBIOS Information
Embedded Controller	See submenu	Embedded Controller Parameters
M.2 peripheral management	See submenu	M.2 peripheral management
ACPI Devices Configuration	See submenu	ACPI Devices Configuration

4.3.1 Trusted computing submenu

Menu Item	Options	Description
Security Device Support	Enabled / Disabled	Enables or Disables BIOS support for security device. OS will not show the Security Device. TCG EFI protocol and INT1A interface will not be available. When enabled all the following items will be available.
SHA-1 PCR Bank	Enabled / Disabled	Enables or Disables SHA-1 PCR Bank
SHA256 PCR Bank	Enabled / Disabled	Enables or Disables SHA256 PCR Bank
Pending Operation	None / TPM Clear	Schedule an Operation for the Security Device. NTE: your Computer will reboot during restart in order to change State of Security Device.
Platform Hierarchy	Enabled / Disabled	Enables or Disabled the Platform Hierarchy
Storage Hierarchy	Enabled / Disabled	Enables or Disabled the Storage Hierarchy
Endorsement Hierarchy	Enabled / Disabled	Enables or Disabled the Endorsement Hierarchy
TPM2.0 UEFI Spec Version	TCG_1_2 TCG_2	Select the TCG Spec Version support. TCG_1_2 is the compatible mode for Windows 8 / Windows 10. TCG 2 supports the new TCG2 protocol and event format for Windows 10 or later.
Physical Presence Spec Version	1.2 / 1.3	Select to tell OS to support PPI Spec Version 1.2 or 1.3. Please note that some HCK tests might not support 1.3
Device Select	Auto TPM 1.2 TPM 2.0	TPM 1.2 will restrict the support to TPM 1.2 devices only, TPM 2.0 will restrict the support to TPM 2.0 devices only, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

4.3.2 ACPI Settings submenu

Menu Item	Options	Description
Enable ACPI Auto Configuration	Disabled / Enabled	Enables or Disables BIOS ACPI Auto Configuration. The following menu items will appear only when this menu item is Disabled
Enable Hibernation	Disabled / Enabled	Enables or disables system ability to Hybernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled S3 (Suspend to RAM)	Select the highest ACPI Sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy resources	Disabled / Enabled	Enables or Disables Lock of Legacy resources

4.3.3 S5 RTC Wake Settings submenu

Menu Item	Options	Description
Wake system from S5	Disabled By Every Day By Day of Month	Enables or disables System Wake on Alarm event. The following menu items will appear only when this voice is not set to Disabled
Wake up hour	0..23	Sets the wake up hour in 0..23 format (i.e.,3 means 3am, 15 means 3pm)
Wake up minute	0..59	Sets the wake up minute
Wake up second	0..59	Sets the wake up second
Day of Month	1..31	This item is available only when “Wake system from S5” is set to “By Day of Month”. Sets the day of month for Wake on Alarm event. Valid range s from 1 to 31, error checking will be done against month/day/year combinations that are not valid.

4.3.4 CPU Configuration submenu

Menu Item	Options	Description
Detailed CPU Information		Shows board’s specific SoC information
CPU Power Management	See Submenu	CPU Power Management options
Active Processor Cores	Disabled / Enabled	Number of Cores to enable in each processor package
Core 0 Core 1 Core 2 Core 3	Disabled / Enabled	Core #x Enable / Disable. Only available when “Active Processor Cores” is enabled
Intel Virtualization Technology	Disabled / Enabled	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology
VT-d	Disabled / Enabled	Enables or disables CPU VT-d
Bi-directional PROCHOT	Disabled / Enabled	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor
Thermal Monitor	Disabled / Enabled	Enables or disables the Thermal Monitor
Monitor Mwait	Disabled / Enabled / Auto	Enables or disables Monitor Mwait
P-STATE Coordination	HW_ALL / SW_ALL / SW_ANY	Change P-STATE Coordination type
DTS	Disabled / Enabled	Enables or disables the Digital Thermal Sensor

4.3.4.1 CPU Power Management submenu

Menu Item	Options	Description
EIST	Disabled / Enabled	Enables or disables Intel® SpeedStep
Turbo mode	Disabled / Enabled	Only Available when "EIST" is enabled. Enables or disables the Turbo Mode
Boot Performance mode	Max performance Max battery	Select the performance state that the BIOS will set before OS handoff.
Power Limit 1 Enable	Disabled / Enabled	Enables or disables Power Limit 1. When Enabled, the following menu items will appear
Power Limit 1 Clamp Mode	Disabled / Enabled	When Power Limit 1 is Enabled. Enables or disables the Clamp Mode
Power Limit 1 Power	Auto / 3 / 4 / 5 / 6 / 7 / 8 / 9 / 10	Power Limit 1 in Watts. Auto will program Power Limit 1 based on silicon default support value.
Power Limit 1 Time Windows	Auto / 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8 / 10 / 12 / 14 / 16 / 20 / 24 / 28 / 32 / 40 / 48 / 56 / 64 / 80 / 96 / 112 / 128	Power Limit 1 Time Window Value in Seconds. Auto will program the Power Limit 1 Time Window based on silicon default support value

4.3.5 AMI graphic Output Protocol Policy submenu

Menu Item	Options	Description
Output Select	*List of available / connected module's video interfaces*	User select monitor for graphic console output in the pre-OS phase

4.3.6 PCI Subsystems Settings

Menu Item	Options	Description
Above 4G Decoding	Disabled / Enabled	Globally Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding)
BME DMA Mitigation	Disabled / Enabled	Re-enable Bus Master Attribute, disabled during Pci enumeration for PCI Bridges after SMM Loocked
Hot-Plug support	Disabled / Enabled	Globally Enables or Disables Hot-Plug support for the entire System. If System has Hot-Plug capable Slots and this option set to Enabled, it provides a Setup screen for selecting PCI resource padding for Hot-Plug

4.3.7 Network Stack configuration submenu

Menu Item	Options	Description
Network Stack	Enabled / Disabled	Enables or disables UEFI Network Stack. When enabled, following menu items will appear
Ipv4 PXE Support	Enabled / Disabled	Enables or disables IPV4 PXE Boot Support. If disabled, IPV4 PXE boot option will not be created
Ipv4 HTTP Support	Enabled / Disabled	Enables or disables IPV4 HTTP Boot Support. If disabled, IPV4 HTTP boot option will not be created
Ipv6 PXE Support	Enabled / Disabled	Enables or disables IPV6 PXE Boot Support. If disabled, Ipv6 PXE boot option will not be created
Ipv6 HTTP Support	Enabled / Disabled	Enables or disables IPV6 HTTP Boot Support. If disabled, Ipv6 HTTP boot option will not be created
PXE boot wait time	[0..5]	Wait time to press ESC key to abort the PXE boot
Media detect count	[1..50]	Number of times that the presence of media will be checked

4.3.8 CSM configuration submenu

Menu Item	Options	Description
CSM Support	Enabled / Disabled	Enables or disables the Compatibility Support Module. When enabled, the following menu items will appear
GateA20 Active	Upon Request Always	Upon Request: GateA20 can be disabled using BIOS services, Always: do not allow disabling GateA20; this option is useful when any RT code is executed above 1MB.
INT19 Trap Response	Immediate Postponed	BIOS Reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot
Boot option filter	UEFI and Legacy Legacy only UEFI only	This option controls Legacy / UEFI ROMs priority
Network	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy PXE OpROM
Storage	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Video OpROM

Other PCI devices	Do not launch UEFI Legacy	Determines the OpROM execution policy for devices other than Network, Storage or Video

4.3.9 NVMe configuration submenu

NVMe Device Options Settings, depend on NVMe Devices found in the system.

4.3.10 SDIO configuration submenu

Menu Item	Options	Description
SDIO Access Mode	Auto ADMA SDMA PIO	Auto Option: Access the SD Device in DMA mode if the controller supports it, otherwise in PIO Mode. DMA Option: Access the SD Device in DMA mode ADMA Option: Access the SD Device in Advanced DMA mode PIO Option: Access the SD Device in PIO mode
List of SDIO devices found, if available	Auto Floppy Forced FDD Hard Disk	Mass storage device emulation type. 'Auto' enumerates devices less than 530Mb as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD.

4.3.11 USB configuration submenu

Menu Item	Options	Description
Legacy USB Support	Enabled / Disabled / Auto	Enables Legacy USB Support. AUTO Option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
XHCI hand-off	Enabled/ Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enabled/ Disabled	Enables or disables USB Mass Storage Driver Support
USB Transfer time-out	1 sec / 5 sec / 10 sec / 20 sec	Sets the time-out value for Control, Bulk and Interrupt transfers
Device reset time-out	10 sec / 20 sec / 30 sec / 40 sec	USB mass storage device Start Unit command time-out
Device power-up delay	Auto / Manual	Sets the maximum time that the device will take before it properly reports itself to the Host controller. 'Auto' uses the default vale (for a Root port it is 100ms, for a Hub port the delay is taken from the Hub descriptor).
Device power-up delay in seconds	[1..40]	When "Device power-up delay" is set to manual. Delay range in seconds, in increments of one second.

4.3.12 Platform Trust technology submenu

Menu Item	Options	Description
fTPM	Enabled / Disabled	Enable/Disable fTPM

4.3.13 Main Thermal Configuration submenu

Menu Item	Options	Description
Critical Temperature (°C)	Settable Threshold (°C) [80 .. 110]	Above this threshold, an ACPI aware OS performs a critical shut down. Allowed range is from 80 to 110 included, where 110 means disabled.
Passive Cooling Temperature (°C)	Settable Threshold (°C) [60 .. 105]	Above this threshold, an ACPI aware OS begins to lower the CPU speed. Allowed range is from 60 to 105 included, where values not below Critical Temperature mean disabled.
TC1	[0...16]	Thermal Constant 1: part of the ACPI Passive Cooling Formula
TC2	[0..16]	Thermal Constant 2: part of the ACPI Passive Cooling Formula
TSP (seconds)	[2..32]	Period of temperature sampling when Passive Cooling

4.3.14 HSUART Transceiver Configuration submenu

Menu Item	Options	Description
HSUART #0 Interface	RS-232 RS-422 RS-485	Select among RS232 (default), RS-422 or RS-485 interface. When selecting RS-422 or RS-485, the following menu item will appear
HSUART #0 RX termination	Disabled / Enabled	RX termination can be enabled when RS-422 or RS-485 is selected. Disable (default) or enable 120 Ohm RX Termination.
HSUART #0 TX termination	Disabled / Enabled	TX termination can be enabled when RS-422 or RS-485 is selected. Disable (default) or enable 120 Ohm TX Termination.
HSUART #2 Interface	RS-232 RS-422 RS-485	Select among RS232 (default), RS-422 or RS-485 interface. When selecting RS-422 or RS-485, the following menu item will appear
HSUART #2 RX termination	Disabled / Enabled	RX termination can be enabled when RS-422 or RS-485 is selected. Disable (default) or enable 120 Ohm RX Termination.
HSUART #2 TX termination	Disabled / Enabled	TX termination can be enabled when RS-422 or RS-485 is selected. Disable (default) or enable 120 Ohm TX Termination.

4.3.15 LVDS Configuration submenu

Menu Item	Options	Description
LVDS interface	Enabled / Disabled	Enables or Disables the LVDS interface. When enabled all the following parameters will appear
Edid Mode	External / Default / Custom	Select the source (EDID, Extended Display Identification Data) to be used for the internal flat panel. Depending on the setting chosen, only some of the following option or none will appear.
EDID	640x480 / 800x480 / 800x600 / 1024x600 / 1024x768 / 1280x720 / 1280x800 / 1280x1024 / 1366x768 / 1400x900 / 1600x900 / 1680x1050 / 1920x1080	Only available when Edid Mode is set to “default”. Select a software resolution (EDID settings) to be used for the internal flat panel.
Color Mode	VESA 24bpp / JEIDA 24bpp / 18 bpp	Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.
Interface	Single Channel / Dual Channel	Allows configuration of LVDS interface in Single or Dual channel mode
DE Polarity	Active High Active Low	Data Enable Polarity
V-Sync Polarity	Negative / Positive	Vertical Sync Signal Polarity: Default is Negative (Active Low)
H-Sync Polarity	Negative / Positive	Horizontal Sync Signal Polarity: Default is Negative (Active Low)
LVDS Advanced Options	See Submenu	LVDS Advanced Options Configurations
Save to EEPROM	Enabled / Disabled	Save current LVDS configuration to module EEPROM

4.3.15.1 LVDS Advanced options submenu

Menu Item	Options	Description
Spreading Depth	No Spreading / 0.5% / 1.0% / 1.5% / 2.0% / 2.5%	Sets spread-spectrum bandwidth of LVDS clock frequency for EMI reduction
Output Swing	150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV / 450 mV	Sets the LVDS differential output swing level
T3 Timing	0 ÷ 255	Minimum T3 timing of panel power sequence to enforce (expressed in units of 50ms)
T4 Timing	0 ÷ 255	Minimum T4 timing of panel power sequence to enforce (expressed in units of 50ms)
T12 Timing	0 ÷ 255	Minimum T12 timing of panel power sequence to enforce (expressed in units of 50ms.
T2 Delay	Enabled / Disabled	When Enabled, T2 is delayed by 20ms ± 50%

T5 Delay	Enabled / Disabled	When Enabled, T5 is delayed by 20ms ± 50%
P/N Pairs Swapping	Enabled / Disabled	Enable or disable LVDS Differential pairs swapping (Positive ⇔ Negative)
Pairs Order Swapping	Enabled / Disabled	Enable or disable channel differential pairs order swapping (A ⇔ D, B ⇔ CLK, C ⇔ C)
Bus Swapping	Enabled / Disabled	Enable or disable Bus swapping (Odd ⇔ Even)
Firmware PLL	0: +/- 1.56% 1: +/- 3.12% 2: +/- 6.25% 3: +/- 12.5% 4: +/- 25% 5: +/- 50% 6: +/- 100%	Set Firmware PLL range

4.3.16 SMBIOS Information

Display only screen, shows information about the module and the Carrier board.

4.3.17 Embedded Controller submenu

Menu Item	Options	Description
Power Fail Resume Type	Always ON Always Off Last State	Specifies what must happen when power is re-applied after a power failure (G3 state). Always ON: the System will boot directly as soon as the power is applied. Always OFF: the system remains in power off State until power button is pressed
No C-MOS battery handling	Disabled / Enabled	This option is enabled when “Power Fail resume Type” is set to Always OFF or Last State. In system with no C-MOS battery, the chipset always powers on after a power failure: Always OFF Resume Type or Last State when Last State was OFF will therefore require an immediate shutdown
OUT 80 serial redirection port	None 1 2 1+2	Selects which Embedded Controller’s UART(s) will receive OUT 80 (Post Codes)
Hardware Monitor		By selecting this item, an information screen with System parameters will appear
Reset Causes Handling		By selecting this item, an information screen with the handling of latest resets causes will appear
Super IO Configuration	See Submenu	Sets the parameters for Serial Ports
Internal FAN Settings	See Submenu	Sets the parameters for internal (i.e. on module) FAN

Watchdog Configuration	See Submenu	Configures the Embedded Controller's Watchdog Timer
GPIO Configurations	See Submenu	Sets the parameters for GPIOs

4.3.17.1 Super IO Configuration submenu

Menu Item	Options	Description
Serial Port 1	Enabled/Disabled	Enables or disables Serial Port 1
Address	0x3F8 0x3E8 0x2F0 0x2E8 0x2E0 0x2A8 0x2A0 0x288 0x280	Serial Port IO Base Address
IRQ	3 / 4 / 5 / 6 / 7 / 10 / 11 / 14 / 15	Serial Port IRQ line to assign to Serial Port #1, if enabled.
Serial Port 2	Enabled/Disabled	Enables or disables Serial Port 2
Address	0x3F8 0x3E8 0x2F0 0x2E8 0x2E0 0x2A8 0x2A0 0x288 0x280	Serial Port IO Base Address
IRQ	3 / 4 / 5 / 6 / 7 / 10 / 11 / 14 / 15	Select the IRQ line to assign to Serial Port #2, if enabled.

4.3.17.2 Internal FAN Settings submenu

Menu Item	Options	Description
Enhanced 3 wire RPM measurement	Enabled / Disabled	Enabled: on each measurement phase Duty Cycle will be raised to 100% for 100mS then restored to original value to allow a more precise measure avoiding unwanted ripple on tachometer. Disabled: periodic fan speed up will not occur, but RPM measurement will not be accurate

Automatic Temperature FAN Control	Enabled / Disabled	Disable / Enable Thermal Feed-back FAN Control
AC0 Temperature (°C)	70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when “Automatic Temperature FAN Control”is Enabled AC0: above this temperature the FAN runs at full speed
AC1 Temperature (°C)	5 / 10 / 15 / 20 /25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when “Automatic Temperature FAN Control” is Enabled. AC1: below this temperature the FAN is OFF; between AC1 and AC0 the FAN runs at low speed: this never happens if AC1 is not below AC0.
Temperature Hysteresis	0 .. 10	Only available when “Automatic Temperature FAN Control” is Enabled. Value added (when temperature is growing) to the ACx thresholds or subtracted from them (when temperature is decreasing) to avoid oscillations.
Linear Speed change	Enabled / Disabled	Only available when “Automatic Temperature FAN Control” is Enabled. Linear FAN Duty Cycle growth between AC1 and AC0
FAN Duty Cycle (%) Above AC1	0 .. 100	Only available when “Automatic Temperature FAN Control” is Enabled and “Linear Speed change” is Disabled Fan Duty Cycle (%) between AC1 and AC0 (low speed)
Speed Change Duration	0 .. 50	Only available when “Automatic Temperature FAN Control” is Enabled and “Linear Speed change” is Disabled Duration in seconds of linear FAN Speed Change. Allowed range: from 0 to 50.
FAN PWM Frequency	1 .. 60000	Only available when “Automatic Temperature FAN Control” is Disabled. Sets the frequency of the FAN_PWMOUT signal. Typical values are 100 for a 3-wire device and 20000 for a 4-wire one. Allowed range is 1-60000.
FAN Duty Cycle	0 .. 100	Only available when “Automatic Temperature FAN Control” is Disabled. Default FAN Duty Cycle (%).

4.3.17.3 Watchdog Configuration submenu

Menu Item	Options	Description
Watchdog Status	Disabled / Enabled	Enables or disables the Watchdog Timer. When enabled, the following parameters will appear.
Event action	Raise WDT Signals Power Button Pulse	Action executed at the expiring of the Event time-out.
Reset action	System Reset Power Button Override Raise WDT Signal	Action executed at the expiring of the reset time-out.
Watchdog Delay	0 .. 60	Minutes before watchdog normal operations starts. During delay time-out, a refresh operation will immediately trigger normal operation.

Event time-out	0 .. 60	Time-out minutes that can pass without refresh before triggering the Event Action. A refresh will restart the time-out.
Reset time-out	1 .. 60	Time-out minutes that can pass without refresh before triggering the Reset Action, this timer will start counting when event time-out is expired.

4.3.17.4 GPIO Configurations submenu

Menu Item	Options	Description
GPO0 GPO1 GPO2 GPO3 GPO4 GPO5 GPO6 GPO7	Input Output Low Output High Output Last	Configure pin as input or output with a fixed starting value. Last means no changes with respect to the last boot.

4.3.18 M.2 peripheral management submenu

Menu Item	Options	Description
WiFi on M.2	Disabled / Enabled	Enable Wifi capabilities from a WiFi M.2 Key E Card
Bluetooth on M.2	Disabled / Enabled	Enable Bluetooth capabilities from a BT M.2 Key E Card
WWAN on M.2	Disabled / Enabled	Enable WWAN capabilities from a WWAN M.2 Key B Card

4.3.19 ACPI Devices Configuration submenu

Menu Item	Options	Description
I2C Device Configuration	See submenu	Install I2C devices on ACPI aware OS

4.3.19.1 I2C Device Configuration submenu

Menu Item	Options	Description
Device type	Disabled / 7bits / 10bits	Select I2C device address format for I2C Bus #4 Device #17
Device type	Disabled / 7bits / 10bits	Select I2C device address format for I2C Bus #4 Device #18
Device type	Disabled / 7bits / 10bits	Select I2C device address format for I2C Bus #4 Device #19
Device type	Disabled / 7bits / 10bits	Select I2C device address format for I2C Bus #4 Device #20

4.4 Chipset menu

Menu Item	Options	Description
South Bridge	See submenu	South Bridge Parameters
Uncore Configuration	See submenu	Uncore Configuration Parameters
South Cluster Configuration	See submenu	South Cluster Configuration Parameters

4.4.1 South Bridge submenu

Menu Item	Options	Description
Serial IRQ Mode	Quiet Mode Continuous Mode	Select Serial IRQ Mode. In continuous mode, the host will continually check for device interrupts. In Quiet Mode, Host will wait for a SERIRQ slave to generate a request by driving the SERIRQ line low.
OS Selection	Windows / Android / Win7 / Intel Linux	Select the Target OS

4.4.2 Uncore Configuration submenu

Menu Item	Options	Description
GOP Brightness Level	20/40/60/80/100/120/140/160/180/200/220/240/255	Set Graphics Output Protocol (GOP) Brightness Level
GOP Brightness Minimum value	0 .. 100	Set GOP Brightness minimum level in %
GOP Brightness PWM Frequency	200 .. 40000	Set GOP Brightness PWM Frequency
DDI0 DDC Pull Type	Pull Up 1K Pull Up 2K Pull Up 5K	Sets DDI #0 Pull-up values
DDI1 DDC Pull Type	Pull Up 1K Pull Up 2K Pull Up 5K	Sets DDI #1 Pull-up values
Integrated Graphics Device	Enabled / Disabled	Enable the Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor, or always disable it.
Primary Display	IGD / PCIe / HG	Select which of IGD / PCIe /HG graphics device should be the Primary Display
HG Delay After Power Enable	[0..1000]	Only available when “Primary Display” is set to HG. Delay in milliseconds after power enable
HG Delay After Hold Reset	[0..1000]	Only available when “Primary Display” is set to HG. Delay in milliseconds after hold reset
RC6 (Render Standby)	Enabled / Disabled	Permits to enable the render standby features, which allows the on-board graphics entering in standby mode to decrease power consumption
GTT Size	2 MB / 4 MB / 8 MB	Select the GTT (Graphics Translation Table) Size
Aperture Size	256 MB	Use this item to set the total size of Memory that must be left to the GFX Engine
DVMT Pre-Allocated	64M / 96M / 128M / 160M / 192M / 224M / 256M / 288M / 320M / 352M / 384M / 416M / 448M / 480M / 512M	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphic Device
DVMT Total Gfx Mem	128M / 256M / MAX	Select the size of DVMT (Dynamic Video Memory) 5.0 that the Internal Graphics Device will use
Cd Clock Frequency	144 MHz / 288 MHz / 384 MHz / 576 MHz / 624 MHz	Select the highest CD Clock frequency supported by the platform

GT PM Support	Enabled / Disabled	Enable / Disable GT Power Management Support
PAVP Enable	Enabled / Disabled	Enable / Disable Protected Audio Video Playback (PAVP)
Memory Scrambler	Enabled / Disabled	Enable / Disable the Memory Scrambler Support

4.4.3 South Cluster Configuration submenu

Menu Item	Options	Description
HD Audio Configuration	See submenu	HD Audio Configuration Settings
LPSS Configuration	See submenu	Low Power Sub System Configuration Settings
PCI Express Configuration	See submenu	PCI Express Configuration Settings
SATA Drives	See submenu	SATA Devices Configuration Setup options
SCC Configuration	See submenu	Storage Control Cluster Configuration Settings
USB Configuration	See submenu	USB configuration Settings
Miscellaneous Configuration	See submenu	Miscellaneous Settings

4.4.3.1 HD Audio Configuration submenu

Menu Item	Options	Description
HD Audio Support	Enabled / Disabled	Enable / Disable HD Audio Support
HD Audio DSP	Enabled / Disabled	Enable / Disable HD Audio DSP

4.4.3.2 LPSS Configuration submenu

Menu Item	Options	Description
I2C #0 (D22:F0)	Disable PCI Mode ACPI Mode	Enable/Disable LPSS I2C #0 Support. This I2C line is not connected to anything, but must be enabled if I2C #4 is required
Set LPSS I2C #0 Speed	Standard Mode Fast Mode Fast Plus Mode	Only available when LPSS I2C #0 is not disabled. Select LPSS I2C #0 Speed
I2C #4 (D23:F0) – Touch screen I2C	Disable PCI Mode	Enable/Disable LPSS I2C #4 Support.

	ACPI Mode	
Set LPSS I2C #4 Speed	Standard Mode Fast Mode Fast Plus Mode	Only available when LPSS I2C #4 is not disabled. Select LPSS I2C #4 Speed

4.4.3.3 PCI Express Configuration submenu

Menu Item	Options	Description
Compliance Mode	Enabled / Disabled	Compliance Mode Enable/Disable
PCIE Root Port 3 - M.2 TYPE 2230 (CN15) PCIE Root Port 4 – Internal LAN 0 (CN20) PCIE Root Port 5 – Internal LAN 1 (CN21)	See submenus	Sets the parameters for each single PCI-e Root Port

4.4.3.3.1 PCIE Root Port #x submenus

Menu Item	Options	Description
PCIE Root Port 3 - M.2 TYPE 2230 PCIE Root Port 4 – Internal LAN 0 PCIE Root Port 5 – Internal LAN 1	Auto Enabled Disabled	Controls the PCI Express Root Port. Auto: disable unused root port automatically for the most optimised power saving. Enable: Always enable the PCIe root port. Disable: Always disable the PCIe root port *(all the following items will disappear)*
ASPM	Disable / L0s	PCI Express Active State Power Management Settings
PCIe Speed	Auto Gen1 Gen2	Configure PCIe Speed
PCIe Selectable De-Emphasis	Enabled / Disabled	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b -3.5dB 0b -6dB

4.4.3.4 SATA Drives Configuration submenu

Menu Item	Options	Description
SATA Controller	Enabled / Disabled	Enable / Disable Chipset SATA controller, which supports the 2 black internal SATA ports (up to 3GB/s supported per port).

SATA Test Mode	Enabled / Disabled	Enable / Disable SATA Test Modes
SATA Speed	Gen1 Gen2 Gen3	Select SATA Speed
Port 0 Port 1	Enabled / Disabled	Enable / Disable SATA Port #x

4.4.3.5 SCC Configuration submenu

Menu Item	Options	Description
SCC SD Card Support	Enabled / Disabled	Enable / Disable SCC SD Card Support
SCC eMMC Support	Enabled / Disabled	Enable / Disable SCC eMMC Card Support

4.4.3.6 USB Configuration submenu

Menu Item	Options	Description
xHCI Pre-Boot Driver	Enable / Disable	Enable / Disable the support for XHCI Pre-boot driver.
xHCI Mode	Enable / Disable	Once Disabled, the xHCI Controller function will be disabled, none of the USB devices will be detectable and usable during the boot and in the OS. Do not disable xHCI unless is for debug purposes.
USB Port Disable Override	Enable / Disable	Allows enabling or disabling selectively each single USB port from reporting a device connection to the controller.
USB Port #0 USB Port #1 USB Port #2 USB Port #3 USB Port #4 USB Port #5 USB 3 Port #0 USB 3 Port #1 USB 3 Port #2	Enable / Disable	Only available when “USB Port Disable Override” is Enabled. Allows enabling or disabling the single USB Port #x. Once disabled, any USB device connected to the corresponding port will not be detected by the BIOS neither by the OS
XDCI Support	Disable / PCI Mode	Enable / Disable XDCI (USB dual role functionality)
XDCI Disable Compliance Mode	FALSE / TRUE	Options to disable XHCI Link Compliance Mode. Default is FALSE to not disable Compliance Mode. Set TRUE to disable Compliance Mode

4.4.3.7 Miscellaneous Configuration submenu

Menu Item	Options	Description
Wake On Lan	Enabled / Disabled	Enable or disable the Wake On LAN Feature
BIOS Lock	Enabled / Disabled	Enables or disables the SC BIOS Lock enable feature. It is required that it is enabled to ensure SMM protection of flash
Flash Protection Range Registers	Enabled / Disabled	Enable Flash Protection Range registers
Reset Power Cycle Duration	1-2 seconds 2-3 seconds 3-4 seconds 4-5 seconds	The value in this register determines the minimum time a platform will stay in reset during a host partition reset with power cycle or a global reset

4.5 Security menu

Menu Item	Options	Description
Setup Administrator Password		Set Setup Administrator Password
User Password		Set User Password
Secure Boot	See Submenu	Customizable Secure Boot Settings

4.5.1 Secure Boot submenu

Menu Item	Options	Description
Secure Boot	Enabled / Disabled	Secure Boot is activated when the Platform Key (PK) is enrolled, System Mode is User/Deployed and CSM function is disabled.
Secure Boot Customization	Standard / Custom	Set UEFI Secure Boot Mode to STANDARD Mode or CUSTOM mode. This change will be effective after save. And after reset, the mode will return to Standard
Restore Factory Keys		Active only when “Secure Boot Customization” is set to Custom. Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys
Key management	See submenu	Enable expert users to modify Secure Boot Policy variables without full authentication

4.5.1.1 Key Management submenu

Menu Item	Options	Description
Factory Keys Provision	Enabled / Disabled	Provision factory default keys on next re-boot only when System in Setup Mode
Restore Factory Keys		Force System to User Mode. Configure NVRAM to contain OEM- defined factory default Secure Boot keys
Enroll Efi Image	*File System Image*	Run selected image in Secure Boot mode. Enrol SHA256 Hash Certificates of image into Authorized Signature Database
Restore DB defaults		Restore DB variable to factory defaults
Platform key (PK) Key Exchange Keys Authorized Signatures Forbidden Signatures Authorized Timestamps OS Recovery Signatures	Set New Var Append Key	Enrol factory Defaults or load certificates from a file: 1. Public Key Certificate in: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER encoded) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHA256,384,512 2. Authenticated UEFI variables 3. EFI PE/COFF Image (SHA256), Key Source: Factory, External, Mixed

4.6 Boot menu

Menu Item	Options	Description
Setup Prompt Timeout	0 .. 65535	Number of seconds to wait for setup activation key. 655535 means indefinite waiting.
Bootup NumLock State	On / Off	Select the Keyboard NumLock State at boot
Quiet Boot	Enabled / Disabled	Enables or Disables Quiet Boot options
New Boot Option Policy	Default Place First Place Last	Controls the placement of newly detected UEFI boot options
Boot Mode Select	LEGACY UEFI	Select the boot mode between Legacy and UEFI
Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4 Boot Option #5 Boot Option #6 Boot Option #7 Boot Option #8	Hard Disk0 Hard Disk1 eMMC CD/DVD SD USB Device Network Other Device Disabled	Select the system boot order
UEFI Other Drive BBS Priorities	See submenu	Specifies the Boot Device Priority sequence from available UEFI Drives

4.6.1.1 UEFI Other Drive BBS Priorities submenu

Menu Item	Options	Description
Boot Option #1	Windows Boot Manager Disable	Sets the system boot manager order

4.7 Save & Exit menu

Menu Item	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Changes and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset the system without saving any changes.
Save Changes		Save the changes done so far to any of the setup options.
Discard Changes		Discard the changes done so far to any of the setup options.
Restore Defaults		Restore/Load Default values for all the setup options
Save as User Defaults		Save the changes done so far as User Defaults
Restore User Defaults		Restore the User Defaults to all the setup options
List of EFI boot managers available		Boot override to selected boot manager
Launch EFI Shell from filesystem device		Attempt to Launch the EFI Shell application (Shell.efi) from one of the available filesystem devices

Chapter 5.
APPENDICES

- Thermal Design
- Accessories

5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like ADLER board, offer to the user very good performances in minimal spaces, therefore allowing the system's minimization. On the counterpart, the miniaturizing of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

The board can be used along with specific heatspreaders, but please remember that they will act only as thermal coupling device between the board itself and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimize the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

When using ADLER boards, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilization.

Until the board is used on a laboratory shelf, on free air, just for software development and system tuning, then a heatsink with integrated fan could be sufficient for board's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all SOCs versions.

Therefore, it is always necessary that the customer studies and develops accurately the cooling solution for his system, by evaluating processor's workload, utilization scenarios, the enclosures of the system, the air flow and so on.

SECO can provide ADLER specific passive heatspreaders and active heatsinks with fan, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
SC41-DISS-1-C	ADLER Heat Spreader (PASSIVE) for Celeron/Pentium Nxxxx CPU
SC41-DISS-1-I	ADLER Heat Spreader (PASSIVE) for Atom E39xx CPUs
SC41-DISS-3-C	ADLER Heat Sink (ACTIVE) for Celeron/Pentium Nxxxx CPUs
SC41-DISS-3-I	ADLER Heat Sink (ACTIVE) for Atom E39xx CPUs

5.2 Accessories

SECO can offer various accessories in completion of ADLER functionalities

5.2.1 Accessories kit CABKITC41

This accessories kit includes the following items

- *Dual USB 2.0 Type A adapter with standard PC mounting plate*. Can be used to carry out the signals of internal USB ports #4-#5 (connector CN18) to standard USB 2.0 Type A receptacles
- *Front Panel I/O board* V995, which allows the integration on a panel of an optional enclosure of two Audio jacks (Earphone and Mic in), Reset Button, Power button and two LED (for SATA activity and Power Status of the board itself).

For fixing of the front panel I/O board to the external enclosure's panel, the module is equipped with two brackets and screws for the fixing of the brackets to the module.

- Cables for connection of the Front Panel I/O board to ADLER board.

Connection cable CV-836/30 is needed for audio functionalities; it has to be connected to ADLER board's connector CN7 and to V995 module's connector CN2.

Connection cable CV-837/30 is needed for connection of power and reset pushbuttons and SATA / power LEDs; it must be connected to ADLER board's connector CN12 and to V995 module's connector CN1.

- Serial adapter cable CV-904/20. It can be used to carry out the signals of RS-232/RS-422/RS-485 signals available on the connector CN19 to two standard DB-9 male connectors.
- SATA power cable, for connection of power rails of external SATA disks / SSDs to internal SATA power connector CN10.

5.2.2 USB-to-Serial port converter modules

This optional module can be used to convert one of the internal USB ports available on connector CN18 into a serial port, which can be of RS-232, RS-422 or RS-485 type (fixed configuration).

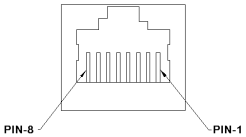
Depending on the type of serial port needed, different module configurations are available; moreover, the output of the module can be available on standard DB-9 male connector or on RJ-45 sockets.

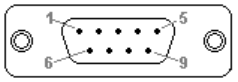
All modules type mounts an FTDI FT232R USB-to-Serial UART interface IC; RS-232 converter module then mounts a Serial Port RS-232 Transceiver with 15kV ESD protection. Instead, the other converters mount and RS-485/RS-422 transceiver.

Modules with DB-9 connector				Modules with RJ-45 socket			
Pin	Signal RS-232 converter	Signal RS-422 converter	Signal RS-485 converter	Pin	Signal RS-232 converter	Signal RS-422 converter	Signal RS-485 converter
1	DCD#	N.C.	N.C.	1	DTR#	N.C.	N.C.
2	RX	RX-	N.C.	2	CTS#	RX+	N.C.
3	TX	TX-	RX- / TX-	3	N.C.	N.C.	N.C.
4	DTR#	N.C.	N.C.	4	RX	RX-	N.C.
5	GND	GND	GND	5	N.C.	N.C.	N.C.
6	DSR#	N.C.	N.C.	6	TX	TX-	RX- / TX-
7	RTS#	TX+	RX+ / TX+	7	GND	GND	GND
8	CTS#	RX+	N.C.	8	RTS#	TX+	RX+ / TX+
9	RI#	N.C	N.C.				

In the table on the left are shown the pinout of DB-9 connector and of RJ-45 socket for all kind of modules.

120Ω termination resistors on differential pairs are available both on RS-422 and on RS-485 modules.





Ordering Code	Description
VA13-0000-1100-C0	USB to RS232 serial port converter with DB9 connector
VA13-0000-1200-C0	USB to RS422 serial port converter with DB9 connector
VA13-0000-1300-C0	USB to RS485 serial port converter with DB9 connector
VA13-0000-2100-C0	USB to RS232 serial port converter with RJ-45 connector
VA13-0000-2200-C0	USB to RS422 serial port converter with RJ-45 connector
VA13-0000-2300-C0	USB to RS485 serial port converter with RJ-45 connector

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